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Analog Electronics

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Table of Contents :

Features of Book

- Use of clear, plain and lucid language making the understanding very easy.
- **Use of informative, self explanatory diagrams, plots and graphs.**
- **Excellent theory well supported with the practical examples and illustrations.**
- **Important concepts are highlighted using Key Points throughout the book.**
- **Large number of solved examples.**
- **Approach of the book resembles classroom teaching.**
- **Book provides detailed insight into the subject.**
- **Stepwise explanation to mathematical derivations for easier understanding.**

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Preface

The importance of **Analog Electronics** is well known in various engineering fields. Overwhelming response to our books on various subjects inspired us to write this book. The book is structured to cover the key aspects of the subject **Analog Electronics**.

The book uses plain, lucid language to explain fundamentals of this subject. The book provides logical method of explaining various complicated concepts and stepwise methods to explain the important topics. Each chapter is well supported with necessary illustrations, practical examples and solved problems. All the chapters in the book are arranged in a proper sequence that permits each topic to build upon earlier studies. All care has been taken to make students comfortable in understanding the basic concepts of the subject.

The book not only covers the entire scope of the subject but explains the philosophy of the subject. This makes the understanding of this subject more clear and makes it more interesting. The book will be very useful not only to the students but also to the subject teachers. The students have to omit nothing and possibly have to cover nothing more.

We wish to express our profound thanks to all those who helped in making this book a reality. Much needed moral support and encouragement is provided on numerous occasions by our whole family. We wish to thank the **Publisher** and the entire team of **Technical Publications** who have taken immense pain to get this book in time with quality printing.

Any suggestion for the improvement of the book will be acknowledged and well appreciated.

Authors

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Dedicated to Gururaj, Neha and Ruturaj

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1 Feedback Amplifiers

1.1 Introduction

Feedback plays an important role in almost all electronic circuits. It is almost invariably used in the amplifier to improve its performance and to make it more ideal. In the process of feedback, a part of output is sampled and fed back to the input of the amplifier. Therefore, at input we have two signals : Input signal, and part of the output which is fed back to the input. Both these signals may be in phase or out of phase. When input signal and part of output signal are in phase, the feedback is called **positive feedback**. On the other hand, when they are in out of phase, the feedback is called **negative feedback**. Use of positive feedback results in oscillations and hence not used in amplifiers.

In this chapter, we introduce the concept of feedback and show how to modify the characteristics of an amplifier by combining a portion or part of the output signal with the input signal. We also study the analysis of various feedback amplifiers.

1.2 Classification of Amplifiers

Before proceeding with the concepts of feedback, it is useful to understand the classification of amplifiers based on the magnitudes of the input and output impedances of an amplifier relative to the source and load impedances, respectively. The amplifiers can be classified into four broad categories : voltage, current, transconductance and transresistance amplifiers.

1.2.1 Voltage Amplifier

Fig. 1.1 shows a Thevenin's equivalent circuit of an amplifier.

If the amplifier input resistance R_i is large compared with the source resistance R_s then $V_i \approx V_s$. If the external load resistance R_L is large compared with the output resistance R_o of the amplifier, then $V_o \approx A_v V_i \approx A_v V_s$. Such amplifier circuit provides a voltage output proportional to the voltage input, and the proportionality factor does not depend on the magnitudes of the source and load resistances. Hence, this amplifier is called **voltage amplifier**. An ideal voltage amplifier must have infinite input resistance R_i and

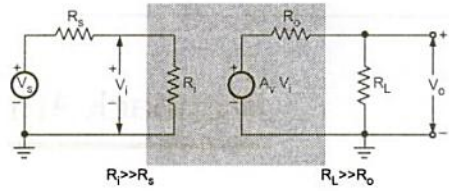


Fig. 1.1 Thevenin's equivalent circuits of a voltage amplifier

zero output resistance R_o. For practical voltage amplifier we must have $R_i >> R_s$ and $R_L >> R_o$.

1.2.2 Current Amplifier

Fig. 1.2 shows Norton's equivalent circuit of a current amplifier. If amplifier input resistance $R_i \to 0$, then $I_i = I_s$. If amplifier output resistance $R_o \to \infty$, then $I_L = A_i I_i$. Such amplifier provides a current output proportional to the signal current, and the proportionality factor is independent of source and load resistances. This amplifier is called **current amplifier**. An ideal current amplifier must have zero input resistance R_i and infinite output resistance R_o. For practical current amplifier we must have $R_i << R_s$ and $R_o >> R_L$.

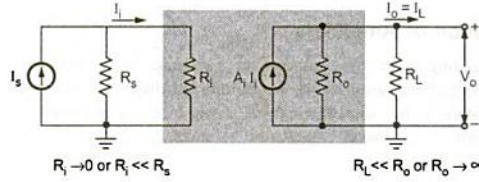


Fig. 1.2 Norton's equivalent circuits of a current amplifier

1.2.3 Transconductance Amplifier

Fig. 1.3 shows a transconductance amplifier with a Thevenin's equivalent in its input circuit and Norton's equivalent in its output circuit. In this amplifier, an output current is proportional to the input signal voltage and the proportionality factor is independent of the magnitudes of the source and load resistances. Ideally, this amplifier must have an infinite input resistance R_i and infinite output resistance R_o. For practical transconductance amplifier we must have $R_i >> R_s$ and $R_o >> R_L$.

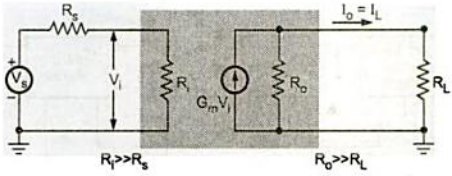


Fig. 1.3 Transconductance amplifier

1.2.4 Transresistance Amplifier

Fig. 1.4 shows a transresistance amplifier with a Norton's equivalent in its input circuit and a Thevenin's equivalent in its output circuit. In this amplifier an output voltage is proportional to the input signal current and the proportionality factor is independent on the source and load resistances. Ideally, this amplifier must have zero input resistance R_i and zero output resistance R_o. For practical transresistance amplifier we must have $R_i << R_s$ and $R_o << R_L$.

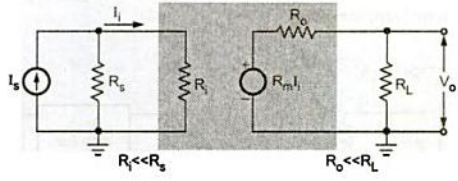


Fig. 1.4

1.3 Block Diagram

In the previous section we have seen four basic amplifier types and their ideal characteristics. In each one of these circuits we can sample the output voltage or current by means of a suitable sampling network and apply this signal to the input through a feedback two port network, as shown in the Fig. 1.5. At the input the feedback signal is combined with the input signal through a mixer network and is fed into the amplifier.

As shown in the Fig. 1.5 feedback connection has three networks :

- Sampling Network
- Feedback Network
- Mixer Network

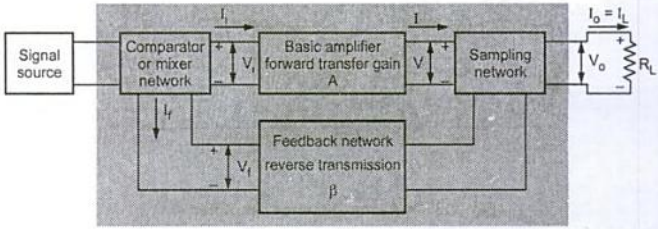
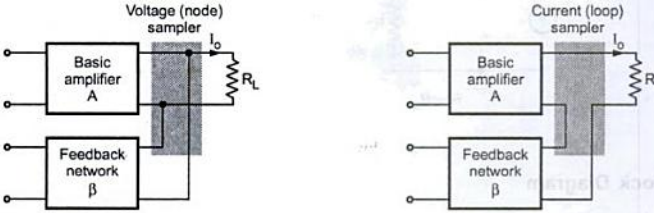


Fig. 1.5 Block diagram of amplifier with feedback

1.3.1 Sampling Network

There are two ways to sample the output, according to the sampling parameter, either voltage or current. The output voltage is sampled by connecting the feedback network in shunt across the output, as shown in the Fig. 1.6 (a). This type of connection is referred to as voltage, or node, sampling. The output current is sampled by connecting the feedback network in series with the output as shown in the Fig. 1.6 (b). This type of connection is referred to as current, or loop, sampling.



(a) Voltage or node sampling **(b) Current or loop sampling**

Fig. 1.6

1.3.2 Feedback Network

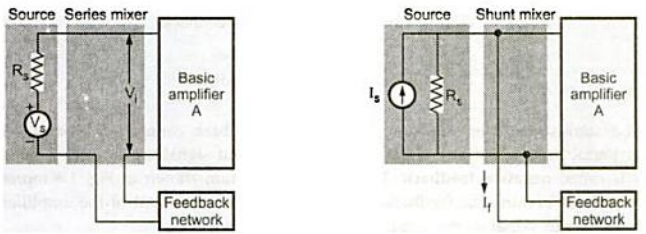
It may consists of resistors, capacitors, and inductors. Most often it is simply a resistive configuration. It provides reduced portion of the output as feedback signal to the input mixer network. It is given as

$$V_f = \beta V_o$$

Where β is a **feedback factor** or **feedback ratio**. The symbol β used in feedback circuits represents feedback factor which always lies between 0 and 1. It is totally different from β symbol used to represent current gain in common emitter amplifier, which is greater than 1.

1.3.3 Mixer Network

Like sampling, there are two ways of mixing feedback signal with the input signal. These are : series input connection and shunt input connection. The Fig. 1.7 (a) and (b) show the simple and very common **series (loop)** input and **shunt (node)** input connections, respectively.



(a) Series mixing **(b) Shunt mixing**

Fig. 1.7

1.3.4 Transfer Ratio or Gain

In Fig. 1.5, the ratio of the output signal to the input signal of the basic amplifier is represented by the symbol A. The suffix of A given next, represents the different transfer ratios.

$$\frac{V}{V_i} = A_v = \text{Voltage gain} \quad \ldots (1)$$

$$\frac{I}{I_i} = A_i = \text{Current gain} \quad \ldots (2)$$

$$\frac{I}{V_i} = G_m = \text{Transconductance} \quad \ldots (3)$$

$$\frac{V}{I_i} = R_m = \text{Transresistance} \quad \ldots (4)$$

The four quantities A_v, A_i, G_m and R_m are referred to as a transfer gain of the basic amplifier without feedback and use of only symbol A represent any one of these quantities.

The transfer gain with feedback is represented by the symbol A_f. It is defined as the ratio of the output signal to the input signal of the amplifier configuration shown in Fig. 1.5. Hence A_f is used to represent any one of the following four ratios :

$$\frac{V_o}{V_s} = A_{Vf} = \text{Voltage gain with feedback} \quad \ldots (5)$$

$$\frac{I_o}{I_s} = A_{If} = \text{Current gain with feedback} \quad \ldots (6)$$

$$\frac{I_o}{V_s} = G_{Mf} = \text{Transconductance with feedback} \quad \ldots (7)$$

$$\frac{V_o}{I_s} = R_{Mf} = \text{Transresistance with feedback} \quad \ldots (8)$$

Fig. 1.8 shows the schematic representation of a feedback connection around a basic amplifier. Recall that, when part of output signal and input signal are in out of phase the feedback is called **negative feedback**. The schematic diagram shown in Fig. 1.8 represents negative feedback because the feedback signal is fed back to the input of the amplifier out of phase with input signal of the amplifier.

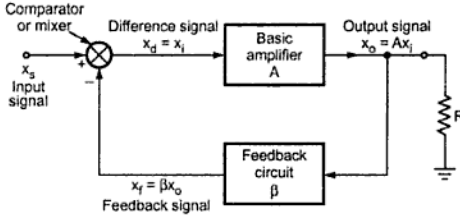


Fig. 1.8 Schematic representation of negative feedback amplifier

1.4 Advantages and Disadvantages of Negative Feedback

1.4.1 Advantages

It is possible to improve important characteristics of four basic amplifier types discussed in section 1.2 by the proper use of negative feedback.

1. **Increased Input Impedance :** Normally high input resistance of a voltage amplifier can be made higher by a factor $(1 + A\beta)$
2. **Reduced Output Impedance :** Normally low output resistance of a voltage amplifier can be lowered by a factor $(1 + A\beta)$

3. **Gain Stability :** The transfer gain A_f of the amplifier with feedback can be stabilized against variations of the h or hybrid-π parameters of the transistor or the parameters of the other active devices used in the amplifier.
4. **Increased Bandwidth :** The proper use of negative feedback improves frequency response of the amplifier by a factor $(1 + A\beta)$.
5. **Reduced Non-linear Distortion :** There is a significant improvement in the linearity of operation of the feedback amplifier compared with that of the amplifier without feedback.
6. **Reduced Noise :** Noise voltage is reduced by factor $(1 + A\beta)$.

1.4.2 Disadvantages

1. All the advantages mentioned above are obtained at the expense of the gain A_f with feedback, which is lowered in comparison with the transfer gain A of an amplifier without feedback by a factor $(1 + A\beta)$.
2. A negative feedback amplifier designed for a particular frequency range may break out into oscillation at some high or low frequency.

1.5 The Four Basic Feedback Topologies

The basic amplifier shown in Fig. 1.8 may be a voltage, current, transconductance, or transresistance amplifier. These can be connected in a feedback configuration as shown in the Fig. 1.9.

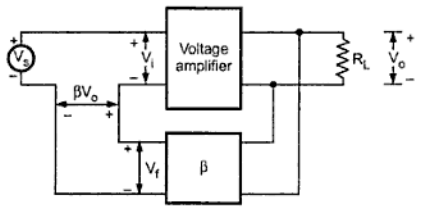


Fig. 1.9 (a) Voltage amplifier with voltage series feedback

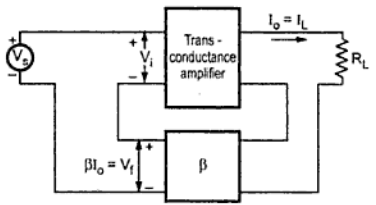


Fig. 1.9 (b) Transconductance amplifier with current series feedback

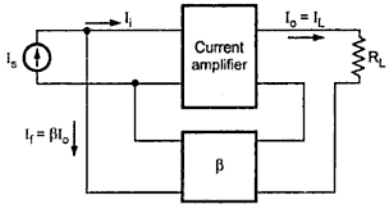


Fig. 1.9 (c) Current amplifier with current-shunt feedback

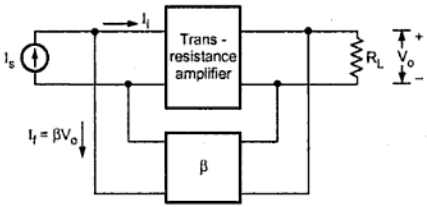


Fig. 1.9 (d) Transresistance amplifier with voltage shunt feedback

1.6 Gain with Feedback

We have seen, the symbol A is used to represent transfer gain of the basic amplifier without feedback and symbol A_f is used to represent transfer gain of the basic amplifier with feedback. These are given as

$$A = \frac{X_o}{X_i} \text{ and } A_f = \frac{X_o}{X_s}$$

Where

X_o = Output voltage or output current

X_i = Input voltage or input current

X_s = Source voltage or source current

As it is a negative feedback the relation between X_i and X_s is given as

$$X_i = X_s + (- X_f)$$

Where

X_f = Feedback voltage or feedback current

$$\therefore \quad A_f = \frac{X_o}{X_s} = \frac{X_o}{X_i + X_f}$$

Dividing by X_i to numerator and denominator we get,

$$A_f = \frac{X_o / X_i}{(X_i + X_f)/X_i} = \frac{A}{1 + X_f / X_i} \quad \because A = \frac{X_o}{X_i}$$

$$= \frac{A}{1 + (X_f / X_o)(X_o / X_i)}$$

$$\therefore \quad A_f = \frac{A}{1 + \beta A} \quad \because \beta = \frac{X_f}{X_o} \qquad \ldots (1)$$

Where β is a feedback factor.

Looking at equation we can say that gain without feedback (A) is always greater than gain with feedback $(A/(1 + \beta A))$ and it decreases with increase in β i.e. increase in feedback factor.

For voltage amplifier, gain with negative feedback is given as

$$\boxed{A_{vf} = \frac{A_v}{1 + A_v \beta}} \equiv \boxed{A_f = \frac{A}{1 + A\beta}} \qquad \ldots (2)$$

Where $A = A_v$ = Open loop gain i.e. gain without feedback

β = Feedback factor

If $|A_f| < |A|$, the feedback is negative, or degenerative. If $|A_f| > |A|$, the feedback is termed positive or regenerative.

1.6.1 Loop Gain

The difference signal, X_d in Fig. 1.8 is multiplied by A in passing through the amplifier, is multiplied by β in transmission through the feedback network, and is multiplied by – 1 in the mixing or difference network. A path of a signal from input terminals through basic amplifier, through the feedback network and back to the input terminals forms a loop. The gain of this loop is the product $-A\beta$. This gain is known as **loop gain** or **return ratio.**

The difference between unity and the loop gain is called **return difference** $D = 1 + A\beta$. The amount of feedback introduced into an amplifier can be expressed in decibels. It is given by

$$N = \text{dB of feedback} = 20 \log \left| \frac{A_f}{A} \right| = 20 \log \left| \frac{1}{1 + A\beta} \right|$$

For negative feedback, N will be negative.

1.6.2 Desensitivity of Gain

The transfer gain of the amplifier is not constant as it depends on the factors such as operating point, temperature, etc. This lack of stability in amplifiers can be reduced by introducing negative feedback.

We know that,

$$A_f = \frac{A}{1+\beta A}$$

Differentiating both sides with respect to A we get,

$$\frac{dA_f}{dA} = \frac{(1+\beta A)1-\beta A}{(1+\beta A)^2}$$

$$= \frac{1}{(1+\beta A)^2}$$

$$\therefore \quad dA_f = \frac{dA}{(1+\beta A)^2}$$

Dividing both sides by A_f we get,

$$\frac{dA_f}{A_f} = \frac{dA}{(1+\beta A)^2} \times \frac{1}{A_f}$$

$$= \frac{dA}{(1+\beta A)^2} \times \frac{(1+\beta A)}{A_f} \qquad \text{since } A_f = \frac{A}{1+\beta A}$$

$$\left|\frac{dA_f}{A_f}\right| = \left|\frac{dA}{A}\right| \frac{1}{|(1+\beta A)|} \qquad \ldots (3)$$

Where

$\frac{dA_f}{A_f}$ = Fractional change in amplification with feedback

$\frac{dA}{A}$ = Fractional change in amplification without feedback

Looking at equation (3) we can say that change in the gain with feedback is less than the change in gain without feedback by factor $(1+\beta A)$. The fractional change in amplification with feedback divided by the fractional change without feedback is called the **sensitivity of the transfer gain.** Hence the sensitivity is $\frac{1}{(1+\beta A)}$. The reciprocal of the sensitivity is called the **desensitivity D.** It is given as

$$D = 1 + \beta A$$

Therefore, stability of the amplifier increases with increase in desensitivity.

If $\beta A >> 1$, then

$$A_f = \frac{A}{1+\beta A} = \frac{A}{\beta A} = \frac{1}{\beta} \qquad \ldots (4)$$

and the gain is dependent only on the feedback network.

Since A represents either A_v, G_M, A_I or R_M and A_f represents the corresponding transfer gains with feedback either A_{vf}, G_{Mf}, A_{If} or R_{Mf} the equation signifies that :

- For voltage series feedback

$$A_{vf} = \frac{1}{\beta} \quad \text{Voltage gain is stabilized} \qquad \ldots (5)$$

- For current series feedback

$$G_{Mf} = \frac{1}{\beta} \quad \text{Transconductance gain is stabilized} \qquad \ldots (6)$$

- For voltage shunt feedback

$$R_{Mf} = \frac{1}{\beta} \quad \text{Transresistance gain is stabilized} \qquad \ldots (7)$$

- For current shunt feedback

$$A_{If} = \frac{1}{\beta} \quad \text{Current gain is stabilized} \qquad \ldots (8)$$

1.7 Cut-off Frequencies with Feedback

We know that,

$$A_f = \frac{A}{1+\beta A}$$

Using this equation we can write,

$$A_{f\,mid} = \frac{A_{mid}}{1+\beta A_{mid}} \qquad \ldots (1)$$

$$A_{f\,low} = \frac{A_{low}}{1+\beta A_{low}} \qquad \ldots (2)$$

and

$$A_{f\,high} = \frac{A_{high}}{1+\beta A_{high}} \qquad \ldots (3)$$

Now we analyse the effect of negative feedback on lower cut-off and upper cut-off frequency of the amplifier.

Lower cut-off frequency

We know that, the relation between gain at low frequency and gain at mid frequency, is given as,

$$\frac{A_{low}}{A_{mid}} = \frac{1}{1-j\left(\frac{f_L}{f}\right)} \quad \therefore A_{low} = \frac{A_{mid}}{1-j\left(\frac{f_L}{f}\right)} \qquad \ldots (4)$$

Substituting value of A_{low} in equation (1) we get,

$$A_{f\,low} = \frac{\dfrac{A_{mid}}{1-j\left(\dfrac{f_L}{f}\right)}}{1+\beta\left(\dfrac{A_{mid}}{1-j\left(\dfrac{f_L}{f}\right)}\right)}$$

$$= \frac{A_{mid}}{1-j\left(\dfrac{f_L}{f}\right)+A_{mid}\,\beta}$$

$$= \frac{A_{mid}}{(1+A_{mid}\beta)-j\left(\dfrac{f_L}{f}\right)}$$

Dividing numerator and denominator by $(1 + A_{mid}\,\beta)$ we get,

$$A_{f\,low} = \frac{\dfrac{A_{mid}}{1+A_{mid}\beta}}{1-j\left[\dfrac{f_L}{\dfrac{1+A_{mid}\beta}{f}}\right]}$$

$$= \frac{A_{f\,mid}}{1-j\left[\left(\dfrac{f_L}{\dfrac{1+A_{mid}\,\beta}{f}}\right)\right]} \quad \because A_f\ mid = \frac{A_{mid}}{1+A_{mid}\,\beta}$$

$$\therefore \quad \frac{A_{f\,low}}{A_{f\,mid}} = \frac{1}{1-j\left(\dfrac{f_{Lf}}{f}\right)} \qquad \ldots(5)$$

where

$$\text{Lower cut-off frequency with feedback} = f_{Lf} = \frac{f_L}{1+A_{mid}\,\beta} \qquad \ldots (6)$$

From equation (6), we can say that lower cut-off frequency with feedback is less than lower cut-off frequency without feedback by factor $(1 + A_{mid}\,\beta)$. Therefore, by introducing negative feedback low frequency response of the amplifier is improved.

Upper Cut-off Frequency

We know that, the relation between gain at high frequency and gain at mid frequency is given as,

$$\frac{A_{high}}{A_{mid}} = \frac{1}{1-j\left(\frac{f}{f_H}\right)}$$

$$\therefore \quad A_{high} = \frac{A_{mid}}{1-j\left(\frac{f}{f_H}\right)} \qquad \ldots (7)$$

Substituting value of A_{high} in equation (11) we get,

$$A_f \text{ high} = \frac{\frac{A_{mid}}{1-j\left(\frac{f}{f_H}\right)}}{1+\beta\left(\frac{A_{mid}}{1-j\left(\frac{f}{f_H}\right)}\right)} = \frac{A_{mid}}{1-j\left(\frac{f}{f_H}\right)+A_{mid}\beta}$$

Dividing numerator and denominator by $(1 + A_{mid}\,\beta)$ we get,

$$A_{f\,high} = \frac{\frac{A_{mid}}{1+A_{mid}\,\beta}}{1-j\left[\frac{f}{(1+A_{mid}\beta)\,f_H}\right]}$$

$$A_{f\,high} = \frac{A_{f\,mid}}{1-j\left[\frac{f}{(1+A_{mid}\beta)\,f_H}\right]} \quad \because A_{f\,mid} = \frac{A_{mid}}{1+A_{mid}\beta}$$

$$= \frac{A_{f\,mid}}{1-j\left(\frac{f}{f_{Hf}}\right)}$$

Where upper cut-off frequency with feedback is given as

$$\boxed{f_{Hf} = (1+A_{mid}\,\beta)\,f_H} \qquad \ldots (8)$$

From equation (8), we can say that upper cut-off frequency with feedback is greater than upper cut-off frequency without feedback by factor $(1 + A_{mid}\,\beta)$. Therefore, by introducing negative feedback high frequency response of the amplifier is improved.

Bandwidth

The bandwidth of the amplifier is given as

$$BW = \text{Upper cut-off frequency} - \text{Lower cut-off frequency}$$

$\therefore$ Bandwidth of the amplifier with feedback is given as

$$BW_f = f_{Hf} - f_{Lf} = (1 + A_{mid}\,\beta)\, f_H - \frac{f_L}{(1 + A_{mid}\,\beta)} \quad \ldots (9)$$

It is very clear that $(f_{Hf} - f_{Lf}) > (f_H - f_L)$ and hence bandwidth of amplifier with feedback is greater than bandwidth of amplifier without feedback, as shown in Fig. 1.10.

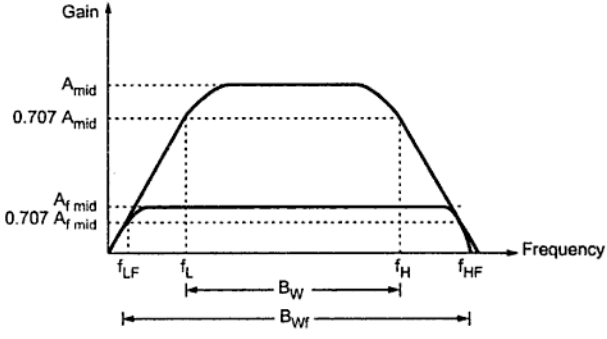


Fig. 1.10 Effect of negative feedback on gain and bandwidth

Key Point : *Since bandwidth with negative feedback increases by factor (1 + Aβ) and gain decreases by same factor, the gain bandwidth product of an amplifier does not altered, when negative feedback is introduced.*

1.8 Distortion with Feedback

1.8.1 Frequency Distortion

From equation (8) of previous section 1.7 we can say that if the feedback network does not contain reactive elements, the overall gain is not a function of frequency. Under such conditions frequency and phase distortion is substantially reduced.

If β is made up of reactive components, the reactances of these components will change with frequency, changing the β. As a result, gain will also change with frequency. This fact is used in tuned amplifiers. In tuned amplifiers, feedback network is designed such that at tuned frequency $\beta \to 0$ and at other frequencies $\beta \to \infty$. As a result, amplifier provides high gain for signal at tuned frequency and relatively reject all other frequencies.

1.8.2 Noise and Nonlinear Distortion

Signal feedback reduces the amount of noise signal and nonlinear distortion. The factor $(1+\beta A)$ reduces both input noise and resulting nonlinear distortion for considerable improvement. Thus, noise and nonlinear distortion also reduced by same factor as the gain.

1.9 Input and Output Resistances

1.9.1 Input Resistance

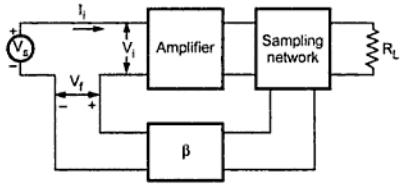


Fig. 1.11

If the feedback signal is added to the input in series with the applied voltage (regardless of whether the feedback is obtained by sampling the output current or voltage), it increases the input resistance. Since the feedback voltage V_f opposes V_s, the input current I_i is less than it would be if V_f were absent, as shown in the Fig. 1.11.

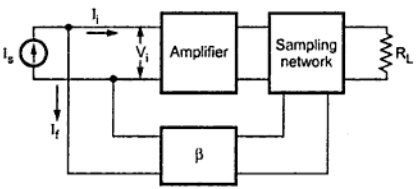


Fig. 1.12

Hence, the input resistance with feedback $R_{if} = \frac{V_s}{I_i}$ is greater than the input resistance without feedback, for the circuit shown in Fig. 1.11.

On the other hand, if the feedback signal is added to the input in shunt with the applied voltage (regardless of whether the feedback is obtained by sampling the output voltage or current), it decreases the input resistance. Since $I_s = I_i + I_f$, the current I_s drawn from the signal source is increased over what it would be if there were no feedback current, as shown in the Fig. 1.12.

Hence, the input resistance with feedback $R_{if} = \frac{V_i}{I_s}$ is decreased for the circuit shown in Fig. 1.12. Now we see the effect of negative feedback on input resistance in different topologies (ways) of introducing negative feedback and obtain R_{if} quantitatively.

Voltage series feedback

The voltage series feedback topology shown in Fig. 1.13 with amplifier is replaced by Thevenin's model. Here, A_v represents the open circuit voltage gain taking R_s into

account. since throughout the discussion of feedback amplifiers we will consider R_s to be part of the amplifier and we will drop the subscript on the transfer gain and input resistance (A_v instead of A_{vs} and R_{if} instead of R_{ifs}).

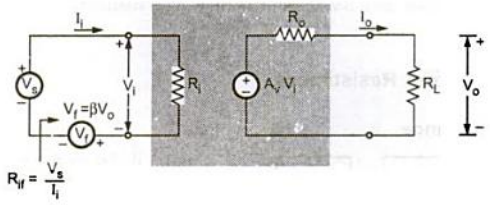


Fig. 1.13

Look at Fig. 1.13 the input resistance with feedback is given as

$$R_{if} = \frac{V_s}{I_i} \quad \ldots (1)$$

Applying KVL to the input side we get,

$$V_s - I_i R_i - V_f = 0$$

$$\therefore \quad V_s = I_i R_i + V_f$$

$$= I_i R_i + \beta V_o \quad \ldots (2)$$

The output voltage V_o is given as

$$V_o = \frac{A_v V_i R_L}{R_o + R_L}$$

$$= A_v I_i R_i = A_V V_i \quad \ldots (3)$$

Where

$$A_V = \frac{V_o}{V_i}$$

$$= \frac{A_v R_L}{R_o + R_L}$$

Key Point : *A_v represents the open circuit voltage gain without feedback and A_V is the voltage gain without feedback taking the load R_L into account.*

Substituting value of V_o from equation (3) in equation (2) we get,

$$V_s = I_i R_i + \beta A_V I_i R_i$$

$$\therefore \quad \frac{V_s}{I_i} = R_i + \beta A_V R_i$$

$$\therefore \quad \boxed{R_{if} = R_i (1 + \beta A_V)} \quad \ldots (4)$$

Current series feedback

The current series feedback topology is shown in Fig. 1.14 with amplifier input circuit is represented by Thevenin's equivalent circuit and output circuit by Norton's equivalent circuit.

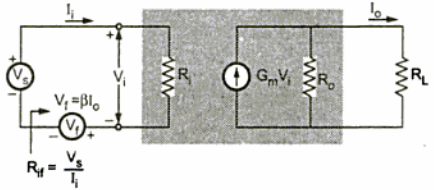


Fig. 1.14

Looking at Fig. 1.14 the input resistance with feedback is given as

$$R_{if} = \frac{V_s}{I_i}$$

Applying KVL to the input side we get,

$$V_s - I_i R_i - V_f = 0$$

$$\therefore \quad V_s = I_i R_i + V_f$$

$$= I_i R_i + \beta I_o \qquad \ldots (5)$$

The output current I_o is given as

$$I_o = \frac{G_m V_i R_o}{R_o + R_L} = G_M V_i \qquad \ldots (6)$$

Where

$$G_M = \frac{G_m R_o}{R_o + R_L}$$

Key Point : *G_m represents the open circuit transconductance without feedback and G_M is the transconductance without feedback taking the load R_L into account.*

Substituting value of I_o from equation (6) into equation (5) we get,

$$V_s = I_i R_i + \beta G_M V_i$$

$$= I_i R_i + \beta G_M I_i R_i \quad \because V_i = I_i R_i$$

$$\therefore \quad \frac{V_s}{I_i} = R_i\,(1+\beta G_M)$$

$$\therefore \quad \boxed{R_{if} = \frac{V_s}{I_i} = R_i\,(1+\beta G_M)} \qquad \ldots (7)$$

Current shunt feedback

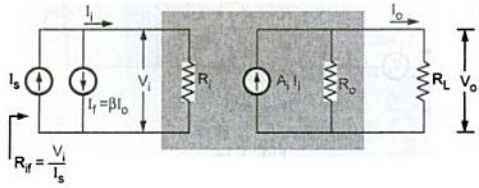


Fig. 1.15

The current shunt feedback topology is shown in Fig. 1.15 with amplifier input and output circuit replaced by Norton's equivalent circuit

Applying KCL to the input node we get

$$I_s = I_i + I_f$$

$$= I_i + \beta I_o \qquad \ldots (8)$$

The output current I_o is given as

$$I_o = \frac{A_i\, I_i R_o}{R_o + R_L}$$

$$= A_I\, I_i \qquad \ldots (9)$$

Where $$A_I = \frac{A_i R_o}{R_o + R_L}$$

Key Point : A_i *represents the open circuit current gain without feedback and* A_I *is the current gain without feedback taking the load* R_L *into account.*

Substituting value of I_o from equation (9) into equation (8) we get,

$$I_s = I_i + \beta A_I I_i$$

$$= I_i\,(1+\beta A_I)$$

The input resistance with feedback is given as

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i\,(1+\beta\ A_I)}$$

$$\therefore \quad \boxed{R_{if} = \frac{R_i}{(1+\beta A_I)} \quad \because R_i = \frac{V_i}{I_i}} \qquad \ldots (10)$$

Voltage shunt feedback

The voltage shunt feedback topology is shown in Fig. 1.16 with amplifier input circuit is represented by Norton's equivalent circuit and output circuit represented by Thevenin's equivalent.

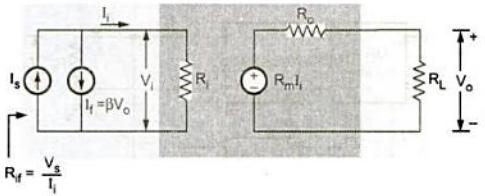


Fig. 1.16

Applying KCL at input node we get,

$$\begin{aligned} I_s &= I_i + I_f \\ &= I_i + \beta V_o \end{aligned} \qquad \ldots (11)$$

The output voltage V_o is given as

$$\begin{aligned} V_o &= \frac{R_m I_i R_o}{R_o + R_L} \\ &= R_M I_i \end{aligned} \qquad \ldots (12)$$

Where $$R_M = \frac{R_m R_o}{R_o + R_L}$$

Key Point : *R_m represents the open circuit transresistance without feedback and R_M is the transresistance without feedback taking the load R_L into account*

Substituting value of V_o from equation (12) into equation (11) we get,

$$\begin{aligned} I_s &= I_i + \beta R_M I_i \\ &= I_i (1 + \beta R_M) \end{aligned}$$

The input resistance with feedback R_{if} is given as

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i (1 + \beta R_M)}$$

$$\therefore \quad \boxed{R_{if} = \frac{R_i}{(1+\beta R_M)}} \qquad \because R_i = \frac{V_i}{I_i} \qquad \ldots (13)$$

1.9.2 Output Resistance

The negative feedback which samples the output voltage, regardless of how this output signal is returned to the input, tends to decrease the output resistance, as shown in the Fig. 1.17.

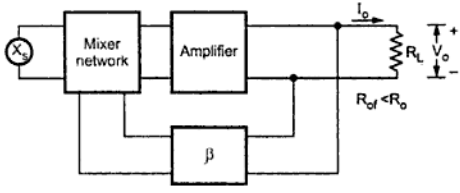


Fig. 1.17

On the other hand, the negative feedback which samples the output current, regardless of how this output signal is returned to the input, tends to increase the output resistance, as shown in the Fig. 1.18.

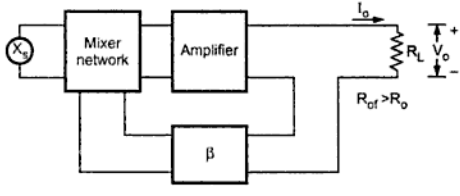


Fig. 1.18

Now, we see the effect of negative feedback on output resistance in different topologies (ways) of introducing negative feedback and obtain R_{of} quantitatively.

Voltage series feedback

In this topology, the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 1.19.

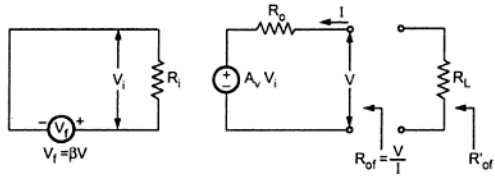


Fig. 1.19

Applying KVL to the output side we get,

$$A_v V_i + IR_o - V = 0$$

$$\therefore \quad I = \frac{V - A_v V_i}{R_o} \qquad \ldots (14)$$

The input voltage is given as

$$V_i = -V_f = -\beta V \quad \because V_s = 0 \qquad \ldots (15)$$

Substituting the V_i from equation (32) in equation (31) we get,

$$I = \frac{V + A_v \beta V}{R_o} = \frac{V(1 + \beta A_v)}{R_o}$$

$$\therefore \quad R_{of} = \frac{V}{I}$$

$$\therefore \quad \boxed{R_{of} = \frac{R_o}{(1 + \beta A_v)}} \qquad \ldots (16)$$

Key Point : *Here A_v is the open loop voltage gain without taking R_L in account,*

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \times R_L}{R_{of} + R_L} = \frac{\left(\frac{R_o}{1 + \beta A_v}\right) \times R_L}{\frac{R_o}{(1 + \beta A_v)} + R_L}$$

$$= \frac{R_o R_L}{R_o + R_L(1 + \beta A_v)} = \frac{R_o R_L}{R_o + R_L + \beta A_v R_L}$$

Dividing numerator and denominator by $(R_o + R_L)$ we get

$$R'_{of} = \frac{\frac{R_o R_L}{R_o + R_L}}{1 + \frac{\beta A_v R_L}{R_o + R_L}}$$

$$\therefore \quad \boxed{R'_{of} = \frac{R'_L}{1 + \beta A_v}} \qquad \because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } A_v = \frac{A_v R_L}{R_o + R_L} \qquad \ldots (17)$$

Key Point : *Here A_v is the open loop voltage gain taking R_L into account.*

Voltage shunt feedback

In this topology, the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 1.20.

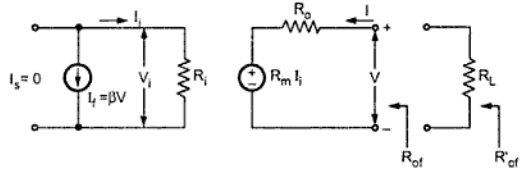


Fig. 1.20

Applying KVL to the output side we get,

$$R_m I_i + I R_o - V = 0$$

$$\therefore \quad I = \frac{V - R_m I_i}{R_o} \qquad \ldots (18)$$

The input current is given as

$$I_i = -I_f = -\beta V. \qquad \ldots (19)$$

Substituting I_i from equation (19) in equation (18) we get,

$$I = \frac{V + R_m \beta V}{R_o} = \frac{V(1 + R_m \beta)}{R_o}$$

$$\therefore \quad R_{of} = \frac{V}{I}$$

$$\therefore \quad \boxed{R_{of} = \frac{R_o}{1 + R_m \beta}} \qquad \ldots [20\ (a)]$$

Key Point : *Here, R_m is the open loop transresistance without taking R_L in account.*

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{\frac{R_o \times R_L}{1 + R_m \beta}}{\frac{R_o}{1 + R_m \beta} + R_L} = \frac{R_o R_L}{R_o + R_L (1 + R_m \beta)}$$

Dividing numerator and denominator by $R_o + R_L$ we get,

$$R'_{of} = \frac{\frac{R_o R_L}{R_o + R_L}}{1 + \frac{\beta R_m R_L}{R_o + R_L}}$$

$$\boxed{R'_{of} = \frac{R'_o}{1+\beta R_m}} \quad \ldots (38)$$

Key Point: *Here,* R_m *is the open loop transresistance taking* R_L *in account.*

Current shunt feedback

In this topology, the output resistance can be measured by open circuiting the input source $I_s = 0$ and looking into the output terminals, with R_L disconnected, as shown in the Fig. 1.21.

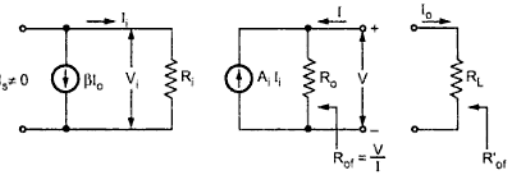


Fig. 1.21

Applying the KCL to the output node we get,

$$I = \frac{V}{R_o} - A_i I_i \quad \ldots (21)$$

The input current is given as

$$I_i = -I_f = -\beta I_o \quad \because I_s = 0$$

$$= \beta I \quad \because I = -I_o \quad \ldots (22)$$

Substituting value of I_i from equation (22) in equation (21) we get,

$$I = \frac{V}{R_o} - A_i \beta I$$

$$\therefore \quad I(1 + A_i \beta) = \frac{V}{R_o}$$

$$\therefore \quad \boxed{R_{of} = \frac{V}{I} = R_o (1 + \beta A_i)} \quad \ldots (23)$$

Key Point : *Here,* A_i *is the open loop current gain without taking* R_L *in account.*

$$R'_{of} = R_{of} \,||\, R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{R_o (1+\beta A_i) R_L}{R_o (1+\beta A_i) + R_L} = \frac{R_o R_L (1+\beta A_i)}{R_o + R_L + \beta A_i R_o}$$

Dividing numerator and denominator by $R_o + R_L$ we get,

$$R'_{of} = \frac{\frac{R_o R_L (1+\beta A_i)}{R_o + R_L}}{1+\frac{\beta A_i R_o}{R_o + R_L}}$$

$$\therefore \quad \boxed{R'_{of} = \frac{R'_o (1+\beta A_i)}{(1+\beta A_i)}}$$

$$\because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } A_i = \frac{A_i R_o}{R_o + R_L} \qquad ...(24)$$

Key Point: *Here, A_i is the open loop current gain taking R_L in account.*

Current series feedback

In this topology the output resistance can be measured by shorting the input source $V_s = 0$ and looking into the output terminals with R_L disconnected, as shown in the Fig. 1.22.

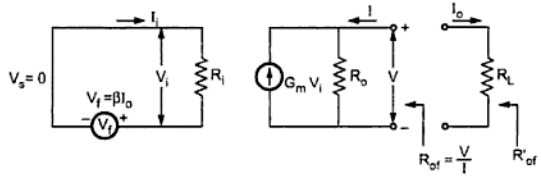


Fig. 1.22

Applying KCL to the output node we get,

$$I = \frac{V}{R_o} - G_m V_i \qquad ... (25)$$

The input voltage is given as $V_i = -V_f = -\beta I_o$

$$= \beta I \qquad \because I_o = -I \qquad ... (26)$$

Substituting value of V_i from equation (26) in equation (25) we get,

$$I = \frac{V}{R_o} - G_m \beta I$$

$$\therefore \quad I(1 + G_m \beta) = \frac{V}{R_o}$$

$$\therefore \quad \boxed{R_{of} = \frac{V}{I} = R_o (1 + G_m \beta)} \qquad ... (27)$$

Key Point : *Here, G_m is the open loop transconductance without taking R_L in account.*

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \times R_L}{R_{of} + R_L}$$

$$= \frac{R_o (1+\beta G_m) R_L}{R_o (1+\beta G_m) + R_L} = \frac{R_o R_L (1+\beta G_m)}{R_o + R_L + \beta G_m R_o}$$

Dividing numerator and denominator by $R_o + R_L$

We get

$$R'_{of} = \frac{\frac{R_L R_o (1+\beta G_m)}{R_o + R_L}}{1 + \frac{\beta G_m R_o}{R_o + R_L}}$$

$$\boxed{R'_{of} = \frac{R'_o (1+\beta G_m)}{1+\beta G_M}} \quad \because R'_o = \frac{R_o R_L}{R_o + R_L} \text{ and } G_M = \frac{G_m R_o}{R_o + R_L} \quad \ldots (28)$$

Key Point : *Note that here, G_M is the open loop current gain taking R_L in account.*

1.10 Summary of Effect of Negative Feedback on Amplifier

Table 1.1 summarizes the effect of negative feedback on amplifier.

Parameter	Voltage series	Current series	Current shunt	Voltage shunt
Gain with feedback	$A_{vf} = \frac{A_v}{1+\beta A_v}$ decreases	$G_{mf} = \frac{G_m}{1+\beta G_m}$ decreases	$A_{if} = \frac{A_i}{1+\beta A_i}$ decreases	$R_{mf} = \frac{R_m}{1+\beta R_{mf}}$ decreases
Stability	Improves	Improves	Improves	Improves
Frequency response	Improves	Improves	Improves	Improves
Frequency distortion	Reduces	Reduces	Reduces	Reduces
Noise and Non linear distortion	Reduces	Reduces	Reduces	Reduces
Input resistance	$R_{if} = R_i(1+\beta A_V)$ increases	$R_{if} = R_i(1+\beta G_M)$ increases	$R_{if} = \frac{R_i}{1+\beta A_I}$ decreases	$R_{if} = \frac{R_i}{1+\beta R_M}$ decreases
Output resistance	$R_{of} = \frac{R_o}{1+\beta A_v}$ decreases	$R_{of} = R_o(1+\beta G_M)$ increases	$R_{of} = R_o(1+\beta A_i)$ increases	$R_{of} = \frac{R_o}{1+\beta R_m}$ decreases

Table 1.1

1.11 Method of Identifying Feedback Topology and Analysis of a Feedback Amplifier

To analyse the feedback amplifier it is necessary to go through the following steps.

Step 1 : Identify Topology (Type of feedback)

a) To find the type of sampling network

1. By shorting the output i.e. $V_o = 0$, if feedback signal (x_f) becomes zero then we can say that it is "Voltage Sampling".
2. By opening the output loop i.e. $I_o = 0$, if feedback signal (x_f) becomes zero then we can say that it is "Current Sampling".

b) To find the type of mixing network

1. If the feedback signal is subtracted from the externally applied signal as a voltage in the input loop, we can say that it is "series mixing".
2. If the feedback signal is subtracted from the externally applied signal as a current in the input loop, we can say that it is "shunt mixing".

Thus by determining type of sampling network and mixing network, type of feedback amplifier can be determine. For example, if amplifier uses a voltage sampling and series mixing then we can say that it is a voltage series amplifier.

Step 2 : Find the input circuit

1. For voltage sampling make $V_o = 0$ by shorting the output
2. For current sampling make $I_o = 0$ by opening the output loop.

Step 3 : Find the output circuit.

1. For series mixing make $I_i = 0$ by opening the input loop.
2. For shunt mixing make $V_i = 0$ by shorting the input

Step 2 and step 3 ensure that the feedback is reduced to zero without altering the loading on the basic amplifier.

Step 4 : Optional. Replace each active device by its h-parameter model at low frequency.

Step 5 : Find the open loop gain (gain without feedback), A of the amplifier.

Step 6 : Indicate X_f and X_o on the circuit and evaluate $\beta = X_f X_o$.

Step 7 : From A and β, find D, A_f, R_{if}, R_{of}, and R'_{of}.

Characteristics	Topology			
	Voltage series	Current series	Current shunt	Voltage shunt
Sampling signal X_o	Voltage	Voltage	Current	Current
Mixing signal	Voltage	Current	Current	Voltage
To find input loop, set	$V_o = 0$	$I_o = 0$	$I_o = 0$	$V_o = 0$
To find output loop, set	$I_i = 0$	$I_i = 0$	$V_i = 0$	$V_i = 0$
Single source	Thevenin	Thevenin	Norton	Norton
$\beta = X_f / X_o$	V_f / V_o	V_f / I_o	I_f / I_o	I_f / V_o
$A = X_o / X_s$	$A_V = V_o / V_i$	$G_M = I_o / V_i$	$A_I = I_o / I_i$	$R_M = V_o / I_i$
$D = 1 + \beta A$	$1 + \beta A_V$	$1 + \beta G_M$	$1 + \beta A_I$	$1 + \beta R_M$
A_f	A_V/D	G_M/D	A_I/D	R_M/D
R_{if}	$R_i D$	$R_i D$	R_i/D	R_i/D
R_{of}	$\frac{R_o}{1+\beta A_v}$	$R_o (1 + \beta G_m)$	$R_o (1 + \beta A_i)$	$\frac{R_o}{1+\beta R_m}$
$R'_{of} = R_{cf} \parallel R_L$	$\frac{R'_o}{1+\beta A_v}$	$\frac{R'_o(1+\beta G_m)}{1+\beta G_M}$	$\frac{R'_o(1+\beta A_i)}{1+\beta A_i}$	$\frac{R'_o}{1+\beta R_M}$

Table 1.2

1.12 Analysis of Feedback Amplifiers

1.12.1 Voltage Series Feedback

In this section, we will see two examples of the voltage series amplifier, First we will analyse transistor emitter follower circuit and then source follower using FET.

1.12.1.1 Transistor Emitter Follower

Fig. 1.23 shows the transistor emitter follower circuit. Here feedback voltage is the voltage across R_o and sampled signal is V_o across R_e.

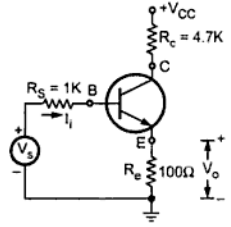


Fig. 1.23

Analysis

Step 1 : Identify Topology

By shorting output voltage ($V_o = 0$), feedback signal becomes zero and hence it is voltage sampling. Looking at Fig. 1.23 we can see that feedback signal V_f is subtracted from the externally applied signal V_s and hence it is a series mixing. Combining two conclusions we can say that it is a voltage series feedback amplifier.

Step 2 and Step 3 : Find input and output circuit

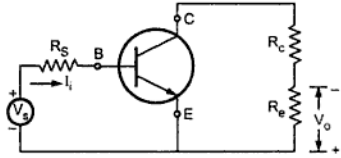


Fig. 1.24

To find the input circuit, set $V_o = 0$, and hence V_s in series with R_s appears between B and E. To find the output circuit, set $I_i = I_b = 0$, and hence R_e appears only in the output loop. With these connections we obtain the circuit as shown in the Fig. 1.24.

Step 4 : Replace transistor by its h-parameter equivalent circuit

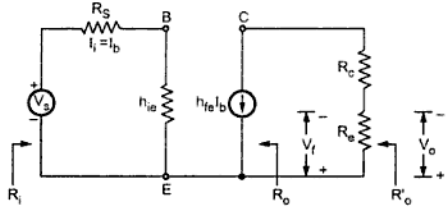


Fig. 1.25 Transistor replaced by its approximate h-parameter equivalent circuit

Step 5 : Find open loop voltage gain

$$A_V = \frac{V_o}{V_s} = \frac{h_{fe} I_b R_e}{V_s}$$

Applying KVL to input loop we get

$$V_s = I_b (R_s + h_{ie})$$

Substituting value of V_s we get

$$A_V = \frac{h_{fe} R_e}{R_s + h_{ie}} = \frac{50 \times 100}{1\,K + 1.1\,K} = \mathbf{2.38}$$

Step 6 : Indicate V_o and V_f and calculate β

We have $\beta = \frac{V_f}{V_o} = 1$ $\because$ both voltage present across R_e

Step 7 : Calculate D, A_{vf} , R_{if} , R_{of} and R'_{of}

$$D = 1 + \beta A_V$$

$$= 1 + 1 \times 2.38$$

$$= \mathbf{2.38}$$

$$A_{Vf} = \frac{A_V}{1 + \beta A_V} = \frac{A_V}{D} = \frac{2.38}{3.38}$$

$$= \mathbf{0.7}$$

$$R_i = R_s + h_{ie}$$

$$= 1\,K + 1.1\,K = \mathbf{2.1\,K}$$

$$R_{if} = R_i\, D$$

$$= 2.1\,K \times 3.38$$

$$= \mathbf{7.098\,K}$$

$$R_o = \infty$$

$$R_{of} = \infty$$

$$R'_{of} = \frac{R'_o}{D} \qquad \text{Where } R'_o = R_e$$

$\therefore$

$$R'_{of} = \frac{R_e}{D} = \frac{100}{3.38}$$

$$= \mathbf{29.58\,\Omega}$$

1.12.1.2 FET Source Follower

Fig. 1.26 shows the FET source follower circuit. Here feedback voltage is the voltage across R_s and sampled signal is V_o across R_e.

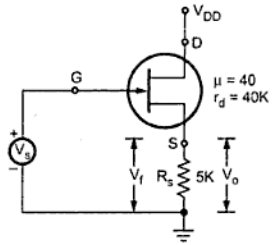


Fig. 1.26

Analysis :

Step 1 : Identify Topology

By shorting output voltage $V_o = 0$, feedback signal becomes zero and hence it is voltage sampling. Looking at Fig. 1.26 we can see that feedback signal V_f is subtracted from the externally applied signal V_s and hence it is a series mixing. Combining two conclusions we can say that it is a voltage series feedback amplifier.

Step 2 and Step 3 : Find input and output circuit

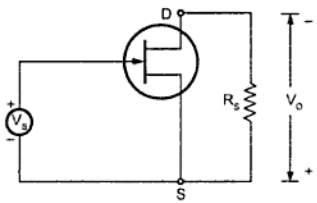


Fig. 1.27

To find the input circuit, set $V_s = 0$, and hence V_s appears between G and S. To find the output circuit, set $I_i = I_G = 0$, and hence R_s appears in the output loop. With these connections we obtain the circuit as shown in the Fig. 1.27.

Step 4 : Replace FET by its equivalent circuit

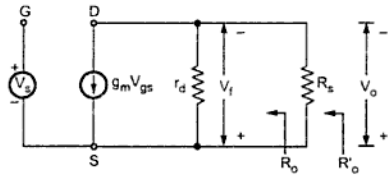


Fig. 1.28

Step 5 : Find open loop voltage gain

$$A_V = \frac{V_o}{V_s} = \frac{g_m V_{gs} r_d R_s}{(r_d + R_s) V_s}$$

$$= \frac{g_m r_d R_s}{r_d + R_s} \quad \because V_{gs} = V_s \qquad \ldots (1)$$

$$= \frac{\mu R_s}{r_d + R_s} \quad \because \mu = g_m r_d \qquad \ldots (2)$$

$$= \frac{40 \times 5\,K}{40\,K + 5\,K} = \mathbf{4.44}$$

Step 6 : Indicate V_o and V_f and calculate β

$$\beta = \frac{V_f}{V_o} = 1 \qquad \because \text{ both voltages present across } R_S$$

Step 7 : Calculate D, A_{vf}, R_{if}, R_{of} and R'_{of}

$$D = 1 + \beta A_v = 1 + 1 \times 4.44$$

$$= \mathbf{5.44} \qquad \ldots (3)$$

$$A_{vf} = \frac{A_v}{1 + \beta A_v} = \frac{A_v}{D}$$

$$= \frac{4.44}{5.44} = \mathbf{0.816}$$

$$R_i = \infty \text{ and hence } R_{if} = R_i\,D = \infty \qquad \ldots (4)$$

$$R_o = r_d = \mathbf{40\ k\Omega} \qquad \ldots (5)$$

$$R_{of} = \frac{R_o}{D} = \frac{40\,K}{5.44} = \mathbf{7.35\ K} \qquad \ldots (6)$$

$$R'_{of} = \frac{R'_o}{D}$$

Where

$$R'_o = R_s \,||\, r_d$$

$$= \frac{R_s r_d}{R_s + r_d} = \frac{5\,K \,||\, 40\,K}{5\,K \,||\, 40\,K} = \mathbf{4.44\ K}$$

$\therefore$

$$R'_{of} = \frac{4.44\,K}{5.44} = \mathbf{816.2\ \Omega} \qquad \ldots (7)$$

1.12.1.3 Voltage Series Feedback Pair

Fig. 1.29 shows two cascaded stages. The output of second stage is connected through feedback network to the input of first stage in opposition to the input signal V_s.

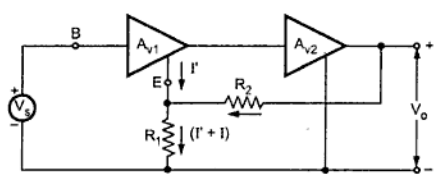


Fig. 1.29 Voltage series feedback pair

Analysis :

Step 1 : Identify topology

By shorting output voltage $V_o = 0$, feedback signal becomes zero and hence it is voltage sampling. Looking at Fig. 1.29 we can see that feedback signal V_f is subtracted from the externally applied signal V_s and hence it is a series mixing. Combining two conclusions we can say that it is a voltage series feedback amplifier.

Step 2 and Step 3 : Find input and output circuit

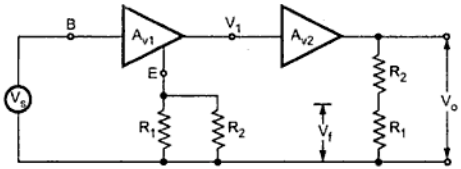


Fig. 1.30

To find input circuit, set $V_o = 0$, and hence R_2 appears in parallel with R_1 at first emitter. To find the output circuit, set $I_i = 0$ and hence R_1 appears in series with R_2 across output. The resulting circuit is shown in Fig. 1.30.

For this circuit, feedback factor β can be calculated as

$$\beta = \frac{V_f}{V_o} = \frac{R_1}{R_1 + R_2} \quad \ldots (8)$$

Example 1.1 : *Transistors in the feedback amplifier shown in Fig. 1.31 are identical and their 'h' parameters are h_{ie} = 1100 Ω, h_{fe} = 100, $h_{re} = h_{oe}$ = 0 Neglect capacitances of all capacitors.*

i) State topology with justification.
ii) Calculate β, A_v, A_{Vf}, R_{if}, R_{of} and R'_{of}.

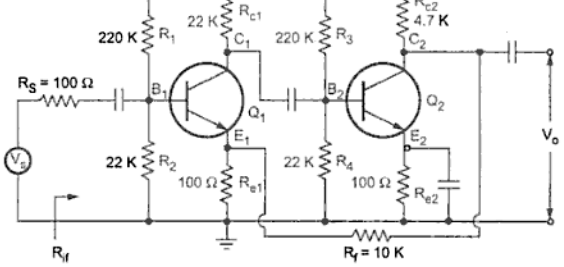


Fig. 1.31

Solution : Step 1 : Identify topology

The feedback voltage is applied across the resistance R_{e1} and it is in series with input signal. Hence feedback is voltage series feedback.

Step 2 and Step 3 : Find input and output circuit

To find input circuit, set $V_o = 0$ (connecting C_2 to ground), which gives parallel combination of R_e with R_f at E_1. To find output circuit, set $I_i = 0$ (opening the input node E_1 at emitter of Q_1), which gives series combination of R_f and R_{e1} across the output. The resultant circuit is shown in Fig. 1.32.

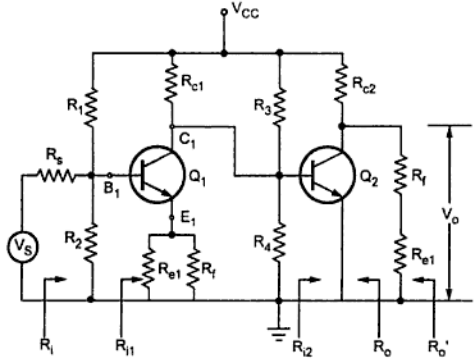


Fig. 1.32

Step 4 : Find open loop voltage gain (A_v)

$$R_{L2} = 4.7\ K \parallel (100 + 10\ K)$$

$$= \mathbf{3.21\ k\Omega}$$

$$A_{i2} = -h_{fe} = \mathbf{-100}$$

$$R_{i2} = h_{ie} = \mathbf{1100\ \Omega}$$

$$A_{v2} = \frac{A_{i2} R_{L2}}{R_{i2}} = \frac{-100 \times 3.21\ K}{1100\ \Omega}$$

$$= \mathbf{-291.82}$$

$$A_{i1} = -h_{fe} = -100$$

$$R_{L1} = R_{C1} \parallel R_1 \parallel R_2 \parallel R_{i2} = 22\ K \parallel 220\ K \parallel 22\ K \parallel 1100$$

$$= \mathbf{995\ \Omega}$$

$$R_{i1} = h_{ie} + (1 + h_{fe}) R_e$$

$$= 1100 + (1 + 100)\ (100\ \Omega \parallel 10\ K)$$

$$= \mathbf{11.099\ k\Omega}$$

$$\therefore \quad A_{vl} = \frac{A_{il} R_{L1}}{R_{il}} = \frac{-100 \times 995}{11.099 \times 10^3}$$

$$= \mathbf{-\ 8.96}$$

The overall gain without feedback is given as

$$A_v = A_{v1} \times A_{v2} = -291.82 \times -8.96$$

$$= \mathbf{2614.7}$$

The overall gain taking R_s in account is given as

$$A_v = \frac{V_o}{V_s} = \frac{A_v R_{il}}{R_{il} + R_s} = \frac{2614.7 \times 11.099 \times 10^3}{11.099 \times 10^3 + 100}$$

$$= \mathbf{2591.35}$$

Step 5 : Calculate β

Looking at Fig. 1.33

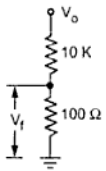


Fig. 1.33

$$\beta = \frac{V_f}{V_o} = \frac{100}{100 + 10 \times 10^3}$$

$$= \mathbf{0.0099}$$

$$D = 1 + \beta A_V = 1 + 0.0099 \times 2591.35$$

$$= \mathbf{26.65}$$

$$\therefore \quad A_{Vf} = \frac{A_V}{D} = \frac{2591.35}{26.65}$$

$$= \mathbf{97.23}$$

$$R_{if} = R_{il}\ D = 11.099 \times 10^3 \times 26.65$$

$$= \mathbf{295.788\ k\Omega}$$

$$R'_{if} = R_{if} \parallel R_1 \parallel R_2 = 295.788\ K \parallel 220\ K \parallel 22\ K$$

$$= \mathbf{18.73\ k\Omega}$$

$$R_{of} = \frac{R_o}{D} = \frac{\infty}{D} = \infty$$

$$\therefore \quad R'_{of} = \frac{R'_o}{D} \quad \text{where } R'_o = R_{L2}$$

$$\therefore \quad R'_{of} = \frac{3.21 \times 10^3}{26.65} = \mathbf{120.45\ \Omega}$$

1.12.2 Current Series Feedback

In this section, we will see two examples of the current series feedback amplifier. First we will analyse transistor common emitter circuit with unbypassed emitter resistance and then common source with unbypassed source resistance.

1.12.2.1 Common Emitter Configuration with Unbypassed R_e

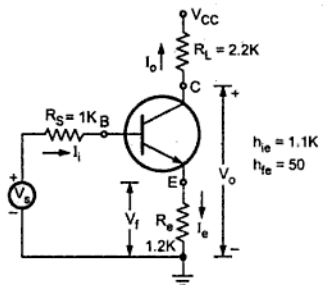


Fig. 1.34

Fig. 1.34 shows the common emitter circuit with unbypassed R_e. The common emitter circuit with unbypassed R_e is an example of current series feedback. In this configuration resistor R_e is common to base to emitter input circuit as well as collector to emitter output circuit and input current I_b as well as output current I_c both flow through it. The voltage drop across R_e, $V_f = (I_b + I_c) = I_e R_e = I_c R_e = - I_o R_e$. This voltage drop shows that the output current I_o is being sampled and it is converted to voltage by feedback network. At input side voltage V_f is subtracted from V_s to produce V_i. Therefore, the feedback applied in series.

Analysis

Step 1 : Identify topology

By opening the output loop, (output current, $I_o = 0$), feedback signal becomes zero and hence it is current sampling. Looking at Fig. 1.34 we can see that feedback signal V_f is subtracted from the externally applied signal V_s and hence it is a series mixing. Combining two conclusions we can say that it is a current series feedback amplifier.

Step 2 and Step 3 : Find input and output circuit

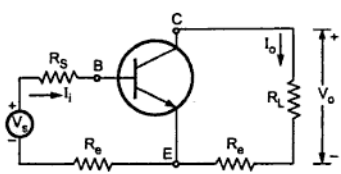


Fig. 1.35

To find input circuit set $I_o = 0$, then R_e appears at the input side. To find output circuit set $I_i = 0$, then R_e appears in the output circuit. The resulting circuit is shown in the Fig. 1.35.

Step 4 : Replace transistor with its approximate h-parameter equivalent circuit

Fig. 1.36 shows the approximate h-parameter equivalent circuit

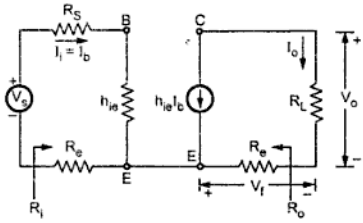


Fig. 1.36 Approximate h-parameter equivalent circuit

Step 5 : Find open loop transfer gain

$$G_M = \frac{I_o}{V_i} = \frac{-h_{fe}I_b}{V_s} \quad \ldots (9)$$

$$= \frac{-h_{fe}I_b}{I_b(R_s + h_{ie} + R_e)}$$

$$= \frac{-h_{fe}}{R_s + h_{ie} + R_e} = \frac{50}{1\,K + 1.1\,K + 1.2\,K}$$

$$= \mathbf{-0.015}$$

Step 6 : Indicate I_o and V_f and calculate β

$$\beta = \frac{V_f}{I_o} = \frac{I_e R_e}{I_o} \quad \ldots (10)$$

$$= \frac{-I_o R_e}{I_o} = -R_e \qquad \because I_e = -I_o$$

$$= \mathbf{-1.2\ K}$$

Step 7 : Calculate D, G_{Mf} , A_{Vf} , R_{if} , R_{of} and R'_{of}

$$D = 1 + \beta G_M = 1 + (-1.2\,K) \times (-0.015) \quad \ldots (11)$$

$$= \mathbf{19.18}$$

$$G_{Mf} = \frac{G_M}{D} = \frac{-0.015}{19.18} \quad \ldots (12)$$

$$= \mathbf{-0.782 \times 10^{-3}}$$

The voltage gain A_{Vf} is given as

$$A_{Vf} = \frac{V_o}{V_s} = \frac{I_o R_L}{V_s} = G_{Mf} R_L \qquad \because G_{Mf} = \frac{I_o}{V_s} \quad \ldots (13)$$

$$= -0.782 \times 10^{-3} \times 2.2\,K$$

$$= \mathbf{-1.72}$$

Looking at Fig. 1.36 R_i can be given as

$$R_i = R_s + h_{ie} + R_e \quad \ldots (14)$$

$$= 1\,K + 1.1\,K + 1.2\,K = \mathbf{3.3\ K}$$

$$R_{if} = R_i\ D = 3.3K \times 19.18 \quad \ldots (15)$$

$$= \mathbf{63.294\ K}$$

Looking at Fig. 1.36 R_o is given as

$$R_o = \infty \quad \ldots (16)$$

$\therefore$ $$R_{of} = R_o\ D = \infty \quad \ldots (17)$$

$$R'_{of} = R_{of} \parallel R_L \quad \ldots (18)$$

$$= R_L \qquad \because R_{of} = \infty$$

$$= \mathbf{2.2\ K}$$

1.12.2.2 Common Source Configuration with R_s Unbypassed

Fig. 1.37 shows the common source circuit with unbypassed R_s. Here, the feedback signal is a voltage across R_s and the sampled signal is the load current I_o.

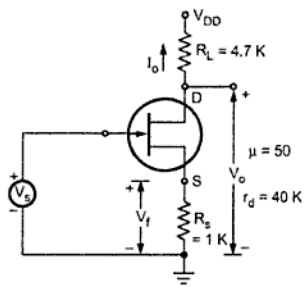


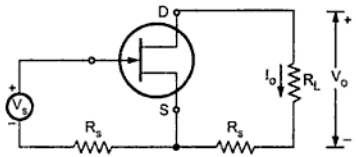
Fig. 1.37

Analysis

Step 1 : Identify topology

By setting $V_o = 0$, drain current does not become zero therefore feedback does not become zero. Hence this is not voltage sampling. On the other hand, by setting $I_o = 0$, we have $V_f = 0$. Hence this is current sampling. The feedback voltage V_f is mixed in series with the input source. Hence the topology used is a current series feedback.

Step 2 and step 3 : Find input and output circuit



To find input circuit set $I_o = 0$, then R_s appears at the input side. To find output circuit set $I_i = 0$, then R_s appears in the output circuit. The resulting circuit is shown in the Fig. 1.38.

Fig. 1.38

Step 4 : Replace FET with its equivalent circuit

Fig. 1.39 shows the equivalent circuit

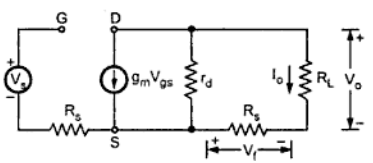


Fig. 1.39 FET replaced by its equivalent circuit

Step 5 : Find the open loop transconductance

$$G_M = \frac{I_o}{V_s} = \frac{-g_m V_{gs} r_d}{\frac{r_d + R_L + R_s}{V_s}}$$

$$= \frac{-g_m r_d}{r_d + R_L + R_s} \quad \because V_s = V_{gs} \qquad \ldots (19)$$

$$= \frac{-\mu}{r_d + R_L + R_s} \quad \because \mu = g_m r_d \qquad \ldots (20)$$

$$= \frac{-50}{40\,K + 4.7\,K + 1\,K} = -1.09 \times 10^{-3}$$

Step 6 : Calculate β

$$\beta = \frac{V_f}{I_o} = \frac{-I_o R_s}{I_o} \qquad \ldots (21)$$

$$= -R_s = -1\ K$$

Step 7 : Calculate D, G_{Mf} , A_{vf} , R_{if} , R_{of} and R'_{of}

$$D = 1+\beta G_M \quad \ldots (22)$$

$$= 1 + (-1\text{ K})(-1.09\times10^{-3})$$

$$= 2.09$$

$$G_{Mf} = \frac{G_M}{D} = \frac{-1.09\times10^{-3}}{2.09} \quad \ldots (23)$$

$$= -0.5215\times10^{-3}$$

$$A_{Vf} = \frac{V_o}{V_s} = \frac{I_o R_L}{V_s}$$

$$= G_{Mf}\, R_L \qquad \because G_{Mf} = \frac{I_o}{V_s} \quad \ldots (24)$$

$$= (-0.5215\times10^{-3})\times(4.7\text{ K})$$

$$= \mathbf{-2.45}$$

Looking at Fig. 1.39 R_i can be given as

$$R_i = \infty \quad \ldots (25)$$

$$\therefore \quad R_i = R_i\, D = \infty \quad \ldots (26)$$

Looking at Fig. 1.39 R_o can be given as

$$R_o = r_d + R_s = 40\text{ K} + 1\text{ K} = \mathbf{41\ K} \quad \ldots (27)$$

$$R_{of} = R_o\,(1+\beta G_m) \text{ where } G_m = \lim_{R_L \to 0} G_M \quad \ldots (28)$$

$$\therefore \quad 1+\beta G_m = \frac{r_d + (1+\mu) R_s}{r_d + R_s}$$

$$\therefore \quad R_{of} = (r_d + R_s) \times \frac{r_d + (1+\mu) R_s}{r_d + R_s}$$

$$= r_d + (1+\mu) R_s \quad \ldots (29)$$

$$= 40\text{ K} + (1+50)\times 1\text{ K} = \mathbf{91\ K}$$

$$R'_{of} = R_L \parallel R_{of} \quad \ldots (30)$$

$$= 4.7\text{ K} \parallel 91\text{ K} = \mathbf{4.47\ K}$$

We have seen that the R'_{of} is most easily calculated as $R_L \parallel R_{of}$. The same result may be obtained from the expression in Table 1.2 with $R'_o = R_o \parallel R_L$. Thus

$$R'_{of} = R'_o \frac{1+\beta G_m}{D}$$

where $R'_o = R_o \parallel R_L$

$$= (r_d + R_s) \parallel R_L = \frac{(r_d + R_s)R_L}{r_d + R_s + R_L}$$

and $D = 1 + \beta GM$

$$= 1 + (-R_s)\frac{-\mu}{r_d + R_L + R_s}$$

$$= 1 + \frac{\mu R_s}{r_d + R_L + R_s}$$

$$= \frac{r_d + R_L + (\mu + 1)R_s}{r_d + R_L + R_s}$$

Substituting the values of R'_o and D we have

$$R'_{of} = \frac{(r_d + R_s)R_L}{r_d + R_s + R_L} \cdot \frac{r_d + (\mu + 1)R_s}{r_d + R_s} \cdot \frac{r_d + R_L + R_s}{r_d + R_L + (\mu + 1)R_s}$$

$$= \frac{R_L[r_d + (\mu + 1)R_s]}{r_d + R_L + (\mu + 1)R_s}$$

$$= \frac{4.7\text{ K}\,[40\text{ K} + (1 + 50) \times 1\text{ K}]}{40\text{ K} + 4.7\text{ K} + (1 + 50) \times 1\text{ K}}$$

$$= \mathbf{4.47\ K}$$

1.12.3 Current Shunt Feedback

Fig. 1.40 shows two transistors in cascade connection with feedback from second emitter to first base through resistor R'. Here, the feedback network formed by R' and R_{e2} divides the current I_e. Since $I_e = -I_o$, the feedback network gives current feedback. At input side, we see that $I_i = I_s - I_f$, i.e. I_f is shunt subtracted from I_s to get I_i. Therefore, this configuration is a current shunt feedback.

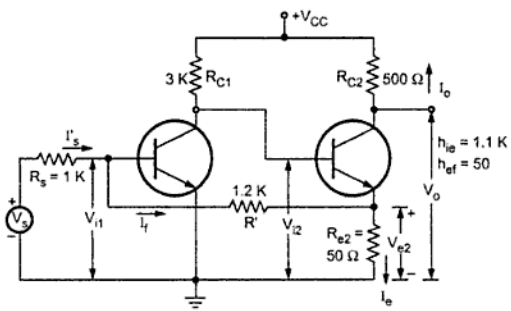


Fig. 1.40

Step 1 : Identify topology

By shorting output voltage ($V_o = 0$), feedback signal does not become zero and hence it is not voltage sampling. By opening the output loop ($I_o = 0$), feedback signal becomes zero and hence it is a current feedback. The feedback signal appears in shunt with input ($I_i = I_s - I_f$), hence the topology is current shunt feedback amplifier.

Step 2 and Step 3 : Find input and output circuit

The input circuit of the amplifier without feedback is obtained by opening the output loop at the emitter of Q_2 ($I_o = 0$). This places R′ in series with R_e from base to emitter of Q_1. The output circuit is found by shorting the input node (the base of Q_1), i.e. making $V_i = 0$. This places R′ in parallel with R_e. The resultant equivalent circuit is shown in Fig. 1.41.

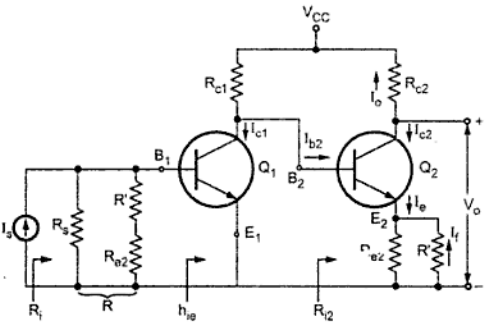


Fig. 1.41

Step 4 : Find open circuit transfer gain

$$A_I = \frac{-I_{c2}}{I_s} = \frac{-I_{c2}}{I_{b2}} \cdot \frac{I_{b2}}{I_{c1}} \cdot \frac{I_{c1}}{I_{b1}} \cdot \frac{I_{b1}}{I_s} \quad \ldots (31)$$

We know that,

$$\frac{-I_{c2}}{I_{b2}} = A_{i2} = -h_{fe} = -50 \text{ and} \quad \ldots (32)$$

$$\frac{-I_{c1}}{I_{b1}} = A_{i1} = -h_{fe} = -50$$

$$\therefore \quad \frac{I_{c1}}{I_{b1}} = 50 \quad \ldots (33)$$

Looking at Fig. 1.41 we can write

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{c1}}{R_{c1}+R_{i2}} \quad \ldots (34)$$

Where $R_{i2} = h_{ie} + (1 + h_{fe})\,(R_{e2} \parallel R')$

$$= 1.1 + (51)\left(\frac{50\times 1.2\ K}{50+1.2\ K}\right)$$

$$= \mathbf{3.55\ K}$$

$$\therefore \quad \frac{I_{b2}}{I_{c1}} = \frac{-3\ K}{3\ K+3.55\ K} = -0.457$$

Looking at Fig. 1.41 we can write

$$\frac{I_{b1}}{I_s} = \frac{R}{R+h_{ie}} \quad \ldots (35)$$

Where $R = R_s \parallel (R' + R_e) = \dfrac{1.2\ K\times 1.25\ K}{1.2\ K+1.25\ K}$

$$= \mathbf{0.612\ K}$$

$$\therefore \quad \frac{I_{b1}}{I_s} = \frac{0.612\ K}{0.612+1.1\ K} = 0.358$$

Substituting the numerial values obtained from equations (32), (33), (34) and (35) in equation (31) we get,

$$A_I = (-50)\times(-0.457)\times(50)\times(0.358)$$

$$= \mathbf{406}$$

Step 5 : Calculate β

Looking at Fig. 1.41 we can write,

$$I_f = \frac{-I_e R_{e2}}{R_e + R'}$$

$$= \frac{-I_c R_{e2}}{R_e + R'} \qquad \because I_e \equiv I_c$$

$$= \frac{I_o R_{e2}}{R_{e2} + R'} \qquad \because I_o = -I_c$$

$$\therefore \quad \beta = \frac{I_f}{I_o} = \frac{R_{e2}}{R_{e2}+R'} = \frac{50}{50+1.2\ K}$$

$$= \mathbf{0.04}$$

Step 6 : Calculate D, R_i, R_{if}, A_{If}, A_{vf}, R_o, R_{of}

$$D = 1 + \beta A_I = 1 + (0.04) \times 406$$

$$= \mathbf{17.2}$$

$$A_{If} = \frac{A_I}{D} = \frac{406}{17.2}$$

$$= \mathbf{23.6}$$

$$A_{vf} = \frac{V_o}{V_s} = \frac{-I_{c2} R_{c2}}{I_s R_s}$$

$$= \frac{A_{If} R_{c2}}{R_s} \qquad \because \frac{-I_{c2}}{I_s} = A_{If}$$

$$= \frac{(23.6)(500)}{1.2\,K}$$

$$= \mathbf{9.83}$$

$$R_i = R \parallel h_{ie} = \frac{0.612\,K \times 1.1\,K}{0.612\,K + 1.1\,K}$$

$$= \mathbf{0.394\ K}$$

$$R_{if} = \frac{R_i}{D} = \frac{0.394\,K}{17.2}$$

$$= \mathbf{23\ \Omega}$$

$$R_o = \infty \qquad \because h_{oe} = 0$$

$$\therefore \quad R_{of} = R_o\, D = \infty$$

$$R'_o = R_o \parallel R_{c2} = \infty \parallel 500 = \mathbf{500\ \Omega}$$

From calculation for A_I we note that A_I is independent of the load $R_L = R_{c2}$. Hence $A_i = \lim_{R_{c2} \to 0} = A_I$

$$\therefore \quad R'_{of} = R'_o \frac{1+\beta A_i}{1+\beta A_I} = R'_o = R_{c2}$$

$$= \mathbf{500\ \Omega}$$

1.12.4 Voltage Shunt Feedback

Fig. 1.42 shows a common emitter amplifier with a resistor R′ connected from the output to the input.

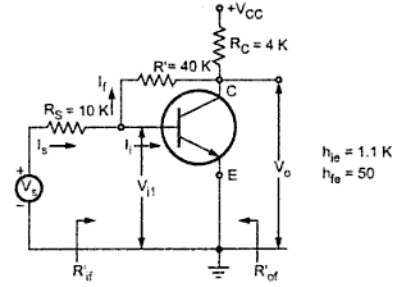


Fig. 1.42

Step 1 : Identify topology

The feedback current I_f is given as

$$I_f = \frac{V_i - V_o}{R'} \qquad \text{But } V_o > \beta V_i$$

$$\therefore \quad I_f = \frac{-V_o}{R'}$$

By shorting output voltage ($V_o = 0$), feedback reduces to zero and hence it is a voltage sampling. As $I_i = I_s - I_f$, the mixing is shunt type and topology is voltage shunt feedback amplifier.

Step 2 and Step 3 : Find input and output circuit.

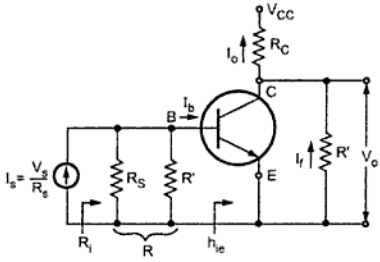


Fig. 1.43

To find input circuit, set $V_o = 0$, this places R′ between base and ground. To find output circuit, set $V_i = 0$, this places R′ between collector and ground.

The resultant circuit is shown in Fig. 1.43.

The feedback signal is the current I_f in the resistor R′ which is in the output circuit as shown in the Fig. 1.43.

We have seen that

$$I_f = \frac{V_i - V_o}{R'} = \frac{-V_o}{R'} \qquad \because V_o > V_i$$

$$\therefore \quad \frac{I_f}{V_o} = \beta = \frac{-1}{R'}$$

$$R_{Mf} = \frac{R_M}{1 + \beta R_M} = \frac{1}{\beta} \qquad \because \beta R_M >> 1$$

$$= -R'$$

$$\therefore \quad A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s}$$

$$\approx \frac{1}{\beta R_s} = \frac{-R'}{R_s}$$

Step 4 : Find the open circuit transresistance

$$R_M = \frac{V_o}{I_s} = \frac{I_o R'_c}{I_s} = \frac{-I_c R'_c}{I_s} \qquad \ldots (36)$$

Where $R'_c = R_c \parallel R' = 4\ K \parallel 40\ K$

$$= \mathbf{3.636\ K}$$

and $$\frac{-I_c}{I_s} = \frac{-I_c}{I_b}\frac{I_b}{I_s}$$

$$\frac{-I_c}{I_b} = A_i = -h_{fe} = -50 \text{ and} \qquad \ldots (37)$$

$$\frac{I_b}{I_s} = \frac{R}{R + h_{ie}} \qquad \text{Where } R = R_S \parallel R' = 10\ K \parallel 40\ K = 8\ K$$

$$\therefore \quad \frac{I_b}{I_s} = \frac{8\ K}{8\ K + 1.1\ K}$$

$$= \mathbf{0.879} \qquad \ldots (38)$$

Substituting values of equation (37) and (38) in equation (36) we have

$$R_M = \frac{-I_c R'_c}{I_s} = \frac{-I_c}{I_b}\frac{I_b}{I_s} \times R'_c$$

$$= (-50) \times (0.879) \times 3.636\ K$$

$$= \mathbf{-159.8\ K}$$

Step 5 : Calculate β

$$\beta = \frac{-1}{R'} = \frac{-1}{40\,K}$$

$$= -2.5\times10^{-5}$$

Step 6 : Calculate D, R_{MF}, A_{VF}, R_{if}, R_{of} and R'_{of}

$$D = 1 + \beta R_M$$

$$= 1 + (-2.5\times10^{-5})\,(-159.8\times10^{3})$$

$$= \mathbf{4.995}$$

$$R_{MF} = \frac{R_M}{D} = \frac{-159.8\,K}{4.995}$$

$$= \mathbf{-32\ K}$$

$$A_{VF} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s} = \frac{R_{Mf}}{R_s}$$

$$= \frac{-32\,K}{10\,K} = \mathbf{-3.2}$$

Looking at Fig. 1.43 we can write

$$R_i = R \parallel h_{ie} = \frac{R\,h_{ie}}{R + h_{ie}}$$

$$= \frac{8\,K\times1.1\,K}{8\,K + 1.1\,K} = 0.967\ K$$

$$R_{if} = \frac{R_i}{D} = \frac{0.967\,K}{4.995}$$

$$= \mathbf{193.59\ \Omega}$$

$$R_o = \infty \qquad \because h_{oe} = 0$$

$\therefore$ $$R_{of} = \frac{\infty}{D} = \infty$$

$$R'_o = R_o \parallel R'_c = \infty \parallel 3.636\ K$$

$$= \mathbf{3.636\ K}$$

$$R'_{of} = \frac{R'_o}{D} = \frac{3.636\,K}{4.995}$$

$$= \mathbf{728\ \Omega}$$

1.13 Nyquist Criterion for Stability of Feedback Amplifiers

A negative feedback amplifier designed for a particular frequency range may break out into oscillation at some high or low frequency. This stability problem arises in feedback amplifiers when the loop gain has more than two real poles. The existence of pole with a positive real part result in a disturbance increasing exponentially with time. When such transient disturbance persists indefinitely or increases, the system becomes unstable.

Hence, the condition which must be satisfied, if a system is to be stable, is that the poles of the transfer function must all lie in the left-hand half of the complex-frequency plane. If the system without feedback is stable, the poles of A do lie in the left-hand half plane. Therefore, from equation $A_f = A/1 + A\beta$ we can say that the stability condition requires that the zeroes of $1 + A\beta$ all lie in the left-hand half of the complex-frequency plane.

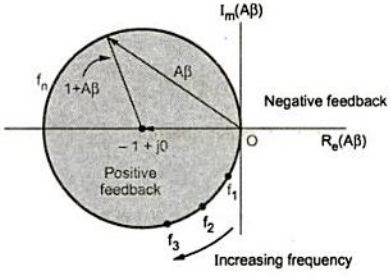


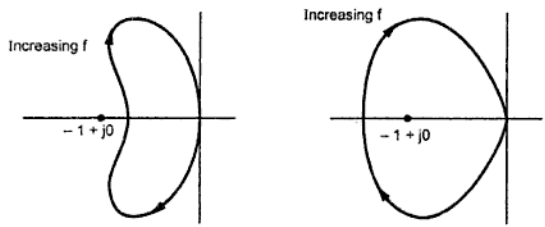
Fig. 1.44 Locus of $|1 + A\beta| = 1$

The Nyquist criterion forms the basis of a steady-state method of determining whether or not an amplifier is stable. The Nyquist criteria express condition for stability in terms of the steady-state, or frequency response, characteristics. Let us see the Nyquist criterion.

Since the product $A\beta$ is a complex number, it may be represented as a point in the complex plane where the real component being plotted along the X axis and the j component along the Y axis. We know that, the $A\beta$ is a function of frequency. Consequently, points in the complex plane are obtained for the values of $A\beta$ corresponding to all values of f from $-\infty$ to $+\infty$. The locus of all these points forms a closed curve. The criterion of Nyquist is that **the amplifier is unstable if this curve encloses the point $-1 + j0$, and the amplifier is stable if the curve does not enclose this point.** (See Fig. 1.44).

The Fig. 1.44 shows the locus of $|1 + A\beta| = 1$. It is a circle of unit radius, with its center at $-1 + j0$. If for any frequency, $A\beta$ extends outside this circle, the feedback is negative since $|1 + A\beta| > 1$. If, however, $A\beta$ lies within this circle, then $|1 + A\beta| < 1$, and the feedback is positive.

An example of the Nyquist criterion is illustrated in Fig. 1.45. The locus in Fig. 1.45 (a) is stable since it does not enclose the $-1 + j0$ point, whereas the locus shown in Fig. 1.45 (b) is unstable since the curve does enclose the $-1 + j0$ point.



(a) Stable (b) Unstable

Fig. 1.45 Stability condition using Nyquist criterion

Examples with Solutions

Example 1.2 : *A feedback amplifier has an open loop gain of 600 and feedback factor $\beta = 0.01$. Find the closed loop gain with negative feedback.*

Solution :

$$A_{vf} = \frac{A}{1+A\beta} = \frac{600}{1+600\times 0.01}$$

$$= \mathbf{85.714}$$

Example 1.3 : *The distortion in an amplifier is found to be 3 %, when the feedback ratio of negative feedback amplifier is 0.04. When the feedback is removed, the distortion becomes 15 %. Find the open and closed loop gain.*

Solution : Given : $\beta = 0.04$ Distortion with feedback = 3 %, Distortion without feedback = 15 %

$$\therefore \quad D = \frac{15}{3} = 5 \quad \text{Where } D = 1 + A\beta = 5$$

$$\therefore \quad 5 = 1 + A\beta = 1 + A \times 0.04$$

$$\therefore \quad A = 100$$

Example 1.4 : *An amplifier has mid-band voltage gain ($A_{v\,mid}$) of 1000 with $f_L = 50$ Hz and $f_H = 50$ kHz, if 5 % feedback is applied then calculate gain f_L, and f_H with feedback.*

Solution : Given $\beta = \frac{5}{100} = 0.05$, $f_L = 50$, $f_H = 50$ kHz and $A_{v\,mid} = 1000$

a) Gain with feedback

$$A_{v\,mid\,f} = \frac{A_{v\,mid}}{1+\beta A_{v\,mid}} = \frac{1000}{1+0.05\times 1000}$$

$$= \mathbf{19.6}$$

b) $$f_{Lf} = \frac{f_L}{1+\beta A_{v\,mid}} = \frac{50}{1+0.05\times 1000}$$

$$= \mathbf{0.98\ Hz}$$

c) $$f_{Hf} = f_H \times (1+\beta A_{v\,mid}) = 50\times 10^3 \times (1+0.05\times 1000)$$

$$= \mathbf{2.55\ MHz}$$

Example 1.5 : *An amplifier with open loop voltage gain of 1000 delivers 10 W of power output at 10 % second harmonic distortion when i/p is 10 mV. If 40 dB negative feedback is applied and output power is to remain at 10 W, determine required input signal V_s and second harmonic distortion with feedback.*

Solution : Given $A_v = 1000$, Output power = 10 W,

a) β : $$-40 = 20 \log\left[\frac{1}{1+\beta A}\right]$$

$\therefore$ $$1+\beta A = 100$$

$\therefore$ $$\beta A = 99$$

$\therefore$ $$\beta = \frac{99}{1000} = \mathbf{0.099}$$

Gain of the amplifier with feedback is given as

$$A_{vf} = \frac{A_v}{1+\beta A_v} = \frac{1000}{100} = \mathbf{10}$$

b) To maintain output power 10 W, we should maintain output voltage constant and to maintain output voltage constant with feedback gain required V_s is

$$V_{sf} = V_s \times 100 = 10\text{mV} \times 100$$

$$= \mathbf{1\ V}$$

c) Second harmonic distortion is reduced by factor $1+\beta A$.

$$\therefore \quad D_{2f} = \frac{D_2}{1+\beta A} = \frac{0.1}{1+\beta A}$$

$$= \frac{0.1}{100} = 0.001$$

$$= \mathbf{0.1\ \%}$$

Example 1.6 : *An amplifier with open loop gain of A = 2000 ± 150 is available. It is necessary to have the amplifier whose voltage gain varies by not more than ± 0.2 %. Calculate β and A_f.*

Solution : a) We know that

$$\frac{dA_f}{A_f} = \frac{1}{1+\beta A} \frac{dA}{A}$$

$$\therefore \quad \frac{0.2}{100} = \frac{1}{1+\beta A} \times \frac{150}{2000}$$

$$\therefore \quad 1+\beta A = 37.5$$

$$\therefore \quad \beta A = 36.5$$

$$\therefore \quad \beta = \frac{36.5}{2000} = 0.01825$$

$$= \mathbf{1.825\ \%}$$

b) A_F :

$$A_F = \frac{A}{1+\beta A} = \frac{2000}{1+0.01825 \times 2000}$$

$$= \mathbf{53.33}$$

Example 1.7 : *If an amplifier has a bandwidth of 300 kHz and voltage gain of 100, what will be the new bandwidth and gain if 10 % negative feed back is introduced? What will be the gain bandwidth product before and after feed back? What should be the amount of feedback if the bandwidth is to be limited to 800 kHz.*

Solution : The voltage gain of the amplifier with feedback is given as

$$A_{vf} = \frac{A}{1+A\beta} \quad \text{Where } \beta = 0.1 \quad \text{and } A = 100$$

$$\therefore \quad A_{vf} = \frac{100}{1+100 \times 0.1}$$

$$= \mathbf{9.09}$$

The bandwidth of an amplifier with feedback is given as

$$B_{wf} = (1+A_{mid}\,\beta)\,f_H - \frac{f_L}{(1+A_{mid}\,\beta)}$$

Assuming $f_H >> f_L$ we have

$$B_w = f_H \text{ and } B_{wf} = (1 + A_{mid}\,\beta)\,B_w$$

$$\therefore \quad B_{wf} = (1+100\times 0.1)\times 300 \text{ kHz}$$

$$= \mathbf{3300\ kHz}$$

The gain bandwidth product before feedback can be given as

Gain bandwidth product = $A_v\,B_w$

$$= 100\times 300 \text{ kHz} = 30\times 10^6$$

Gain bandwidth product after feedback

$$= A_{vf}\times B_{wf}$$

$$= 9.09\times 3300 \text{ kHz}$$

$$= 30\times 10^6$$

If bandwidth is to be limited to 800 kHz we have f_{Hf} = 800 kHz assuming $f_{Hf} >> f_{Lf}$
We know that

$$B_{wf} = (1+A_{vmid}\ \beta)\,f_H$$

$$\therefore \quad 800K = (1+100\beta)\,300\ K$$

$$\therefore \quad \beta = \frac{\frac{800}{300}-1}{100} = \mathbf{0.01667}$$

Example 1.8 : *For the feedback amplifier whose block diagram is shown in Fig. 1.46 compute the changes in ΔA_f when*
i) A_1 changes by an amount ΔA_1 and
ii) A_2 changes by an amount ΔA_2

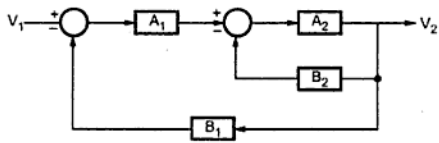


Fig. 1.46

Solution : For above circuit voltage gain with feedback is given as

$$A_f = \frac{A_1\left[\frac{A_2}{1+A_2 B_2}\right]}{1+A_1\left[\frac{A_2}{1+A_2 B_2}\right]B_1}$$

i) $$\Delta A_f = \left| \frac{A_1\left[\frac{A_2}{1+A_2 B_2}\right]}{1+A_1\left[\frac{A_2}{1+A_2 B_2}\right]B_1} - \frac{|A_1-\Delta A_1|\times\left[\frac{A_2}{1+A_2 B_2}\right]}{1+|A_1-\Delta A_1|\times\left[\frac{A_2}{1+A_2 B_2}\right]B_1} \right|$$

ii) $$\Delta A_f = \frac{A_1\left[\frac{A_2}{1+A_2 B_2}\right]}{1+A_1\left[\frac{A_2}{1+A_2 B_2}\right]B_1} - \frac{A_1\left[\frac{|A_2-\Delta A_2|}{1+|A_2-\Delta A_2|\times B_2}\right]}{1+A_1\left[\frac{|A_2-\Delta A_2}{1+|A_2-\Delta A_2|\times B_2}\right]B_1}$$

Example 1.9 : *An amplifier has a voltage gain of 4000. It's input impedance is 2 K and output impedance is 60 K. Calculate the voltage gain, input and output impedance of the circuit is 5 % of the feedback is fed in the form of series negative voltage feedback.*

Solution : The voltage gain with feedback can be given as

$$A_{vf} = \frac{A_v}{1+A_v\beta} = \frac{4000}{1+4000\times 0.05}$$

$$= \mathbf{19.9}$$

In a voltage series feedback input resistance with feedback is given as

$$R_{if} = R_i\,(1+\beta\, A_v)$$

$$= 2\ K(1+0.05\times 4000)$$

$$= \mathbf{402\ k\Omega}$$

In a voltage series feedback output resistance with feedback is given as

$$R_{of} = \frac{R_o}{1+\beta A_v} = \frac{60K}{1+0.05\times 4000}$$

$$= \mathbf{298.5\ \Omega}$$

Example 1.10 : *An amplifier without feedback gives a fundamental output of 36 V with 7 % second harmonic distortion when the input is 0.028 V.*
i) If 1.2 percent of the output is fedback into the input in a negative voltage series feedback circuit, what is the output voltage
ii) If the fundamental output is maintained at 36 V but the second harmonic distortion is reduced to 1 percent what is the input voltage?

Solution : The voltage gain of amplifier can be given as

$$A_v = \frac{V_o}{V_{in}}$$

$$= \frac{36}{0.028}$$

$$= \mathbf{1285.7}$$

i) $\beta = 0.012$

∴ The gain of the amplifier with feedback is given as

$$A_f = \frac{A_v}{1+A_v\beta}$$

$$= \frac{1285.7}{1+1285.7\times 0.012}$$

$$= \mathbf{78.26}$$

The output voltage with feedback is given as

$$V_o = A_f V_{in} = 78.26 \times 0.028$$

$$= \mathbf{2.19\ V}$$

ii) If the output remains constant at 36 V, then the distortion produced within the active devices of the amplifier is unchanged. However, since the distortion at the output is less than in part i) by a factor of 7, it follows that the feedback now increased by 7 and hence, the voltage gain decreased by 7. Thus, the input signal required to produce the same output (as in part i) without feedback must be:

$$V_{in} = 7\ (0.028\ V)$$

$$= \mathbf{0.196\ V}$$

➠ **Example 1.11 :** *An amplifier having a voltage gain of 60 dB uses $1/20^{th}$ of it output in negative feedback. Calculate the gain with feedback, the percentage change in gain without and with feedback consequent on 50 % change in g_m.*

Solution : i) The gain of the amplifier is given as

$$60\ \text{dB} = 20 \log \frac{V_o}{V_s}$$

$$\therefore \quad A_v = \frac{V_o}{V_s} = 1000$$

$$\beta = \frac{1}{20} = \mathbf{0.05}$$

∴ The gain of amplifier with feedback is

$$A_{vf} = \frac{A_v}{1+\beta A_v}$$

$$= \frac{1000}{1+0.05\times 1000}$$

$$= \mathbf{19.6}$$

ii) The gain of the amplifier is directly proportional to the g_m. Therefore, the gain of the amplifier without feedback changes as same amount as g_m changes

$$\therefore \quad A_v = A_v \pm 0.5A_v$$

$$= 1000 \pm 500$$

The gain of the amplifier with feedback is now given as

$$A_{vf} = \frac{1000\pm 500}{1+0.05(1000\pm 500)} = \frac{1000\pm 500}{1+(50\pm 25)}$$

$$= \mathbf{19.23 \text{ or } 19.73}$$

Example 1.12 : *A single stage RC coupled amplifier has a midband gain of 1000 is made into a negative feedback amplifier by feeding 10 % of the output voltage in series with input opposing.*
i) What is the ratio of half power frequencies with feedback to those without feedback?
ii) If f_L = 20 Hz and f_H = 50 kHz for the amplifier without feedback. Find the corresponding values after feedback is incorporated.

Solution : $A_v = 1000$ and $\beta = 0.1$

i) $$\frac{f_{Hf}}{f_H} = 1 + \beta A_v$$

$$= 1 + 0.1 \times 1000$$

$$= \mathbf{101}$$

and $$\frac{f_{Lf}}{f_L} = \frac{1}{1+\beta A_v} = \frac{1}{1+0.1\times 1000}$$

$$= \frac{1}{101}$$

$$= \mathbf{0.0099}$$

ii) With f_L = 20 Hz and f_H = 50 kHz

$$f_{Lf} = 20\times 0.0099$$

$$= 0.198 \text{ Hz and } f_{Hf} = 50 \text{ kHz} \times 101$$

$$= \mathbf{5.05 \text{ MHz}}$$

Example 1.13 : *An amplifier without feedback gives an output of 50 V into 6 % second harmonic distortion when the input is 0.2 V. If the negative feedback is applied to amplifier so that the second harmonic distortion is reduced to 1 %. What value of feedback ratio must be used? What input voltage will be required to produce the same output voltage of 50 V?*

Solution : The voltage gain of the amplifier is given as

$$A_v = \frac{V_o}{V_{in}}$$

$$= \frac{50}{0.2}$$

$$= \mathbf{250}$$

We know that,

$$B_{2f} = \frac{B_2}{1 + A_v \beta}$$

$$\therefore \quad 0.01 = \frac{0.06}{1 + 250\beta}$$

$$\therefore \quad \text{Feedback ratio, } \beta = \frac{\frac{0.06}{0.01} - 1}{250}$$

$$= \mathbf{0.02}$$

ii) $$A_{vf} = \frac{A_V}{1 + A_V \beta}$$

$$= \frac{250}{1 + 250 \times 0.02} = \mathbf{41.66}$$

To produce output voltage of 50 V V_{in} must be

$$V_{in} = \frac{50}{A_{vf}} = \frac{50}{41.66} = \mathbf{1.2\ V}$$

Example 1.14 : *An amplifier with negative feedback has a voltage gain of 120. It is found that without feedback an input signal of 60 mV is required to produce a particular output, whereas with feedback the input signal must be 0.5 V to get the same output. Find A_v and β of the amplifier.*

Solution : Given $A_{vf} = 120$

$$A_v = \frac{V_o}{V_s} = \frac{V_o}{60\ mV}$$

and $$A_{vf} = \frac{V_o}{0.5}$$

$\therefore \quad V_o = 0.5 \times 120 = \mathbf{60\ V}$

with $V_o = 60$ V we have,

$$A_v = \frac{60}{60\text{mV}} = 1000$$

We know that,

$$A_{vf} = \frac{A_v}{1+A_v\beta}$$

$$\therefore \quad 120 = \frac{1000}{1+1000\beta}$$

$$\therefore \quad \beta = \mathbf{0.00733}$$

Example 1.15 : *Identify topology, with justification for the circuit shown in Fig. 1.47 Transistors used are identical and have parameters h_{ie} = 2 K, h_{fe} = 50 and $h_{re} = h_{oe} = 0$. Determine A_{vf}.*

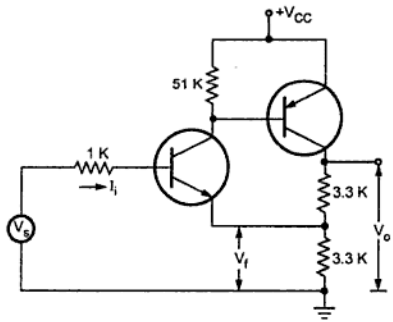


Fig. 1.47

Solution : Step 1 : Identify topology

By shorting output voltage ($V_o = 0$) feedback voltage V_f becomes zero, hence it is a voltage sampling. Since feedback is mixed in series with input the topology is voltage series feedback amplifier.

Step 2 and Step 3 : Find input and output circuit

To find input circuit set $V_o = 0$. This places the parallel combination of 3.3 K and 3.3 K at first emitter. To find output circuit set $I_i = 0$. This places resistors 3.3 K and 3.3 K in series across the output. The resultant circuit is shown in Fig. 1.48.

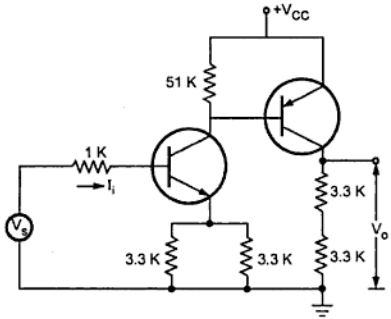


Fig. 1.48

Step 4 : Replace transistors with their h-parameter equivalent circuits

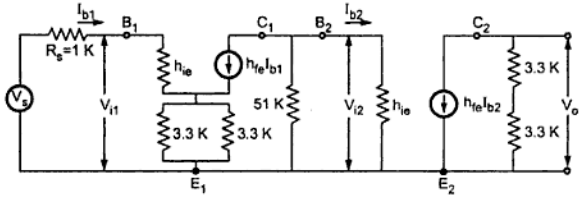


Fig. 1.49 h-parameter equivalent circuit

Step 5 : Find open loop transfer gain

The voltage gain without feedback

$$A_v = A_{v1} A_{v2} = \frac{V_{i2}}{V_{i1}} \times \frac{V_o}{V_{i2}}$$

$$= \frac{V_o}{V_{i2}} = \frac{-h_{fe} R_{L2}}{R_{i2}}$$

Where $R_{L2} = 3.3\ K + 3.3\ K = 6.6\ K$

and $R_{i2} = h_{ie} = 2\ K$

$\therefore$ $$A_{V2} = \frac{V_o}{V_{i2}} = \frac{-50 \times 6.6 \times 10^3}{2 \times 10^3}$$

$$= -165$$

$$\frac{V_{i2}}{V_{i1}} = \frac{-h_{fe}R_{L1}}{R_{i1}}$$

Where $R_{L1} = 51\ K \parallel R_{i2} = 51\ K \parallel 2\ K$

$= \mathbf{1.92\ k\Omega}$

and $R_{i1} = h_{ie} + (1 + h_{fe})\ (3.3\ K \parallel 3.3\ K)$

$= 2 \times 10^3 + (1 + 50)\ (1.65 \times 10^3)$

$= \mathbf{86.15\ k\Omega}$

$\therefore \quad A_{v1} = \frac{V_{i2}}{V_{i1}} = \frac{-50 \times 1.92 \times 10^3}{86.15 \times 10^3} = \mathbf{-1.114}$

$\therefore \quad A_V = -165 \times -1.114 = \mathbf{183.86}$

Step 6 : Calculate β

$$\beta = \frac{V_f}{V_o} = \frac{3.3K}{3.3K + 3.3K} = \mathbf{0.5}$$

We know that, $D = 1 + \beta A_v$

$$A_{vf} = \frac{A_V}{D} = \frac{183.86}{92.93}$$

$= \mathbf{1.978}$

Example 1.16 : *For the circuit shown in Fig. 1.50. Calculate A_{vf}, R_{if} and R'_{of}. Transistors are identical and their parameters are h_{ie} = 1.1 K, h_{fe} = 50. Neglect h_{re} and h_{oe}.*

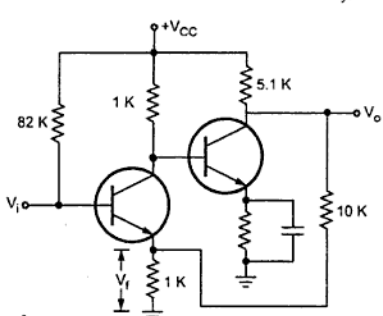


Fig. 1.50

Solution : Step 1 : Identify topology

By shorting output voltage ($V_o = 0$), feedback voltage V_f becomes zero. The feedback voltage is mixed in series feedback.

Step 2 and Step 3 : Find input and output circuit

To find input circuit, set $V_o = 0$. This places the parallel combination of resistors 10 K and 1 K at the first emitter. To find output circuit, set $I_i = 0$. This places resistors 10 K and 1 K is series across the output. The resultant circuit is shown in the Fig. 1.51.

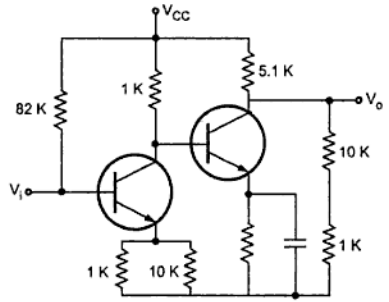


Fig. 1.51

Step 4 : Replace transistors with h-parameter equivalent circuits.

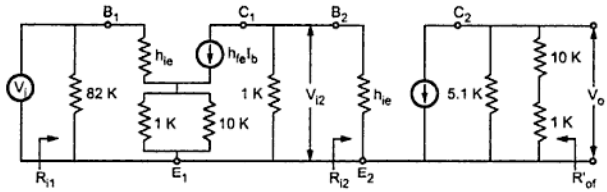


Fig. 1.52 h-parameter equivalent circuit

Step 5 : Find open loop transfer gain

$$A_v = A_{v1} A_{v2}$$

$$= \frac{V_{i2}}{V_{i1}} \times \frac{V_o}{V_{i2}}$$

$$\frac{V_o}{V_{i2}} = \frac{-h_{fe}R_{L2}}{R_{i2}}$$

Where $R_{L2} = 5.1\ K \parallel (10\ K + 1\ K)$

$= \mathbf{3.484\ k\Omega}$

and $R_{i2} = h_{ie} = \mathbf{1.1\ K}$

$\therefore \quad \frac{V_o}{V_{i2}} = \frac{-50 \times 3.484 \times 10^3}{1.1 \times 10^3}$

$= \mathbf{-158.36}$

$$\frac{V_{i2}}{V_{i1}} = \frac{-h_{fe}R_{L1}}{R_{i1}}$$

Where $R_{L1} = R_{i2} \parallel 1\ K = 1.1\ K \parallel 1\ K$

$= \mathbf{523.8\ k\Omega}$

and $R_i = 82\ K \parallel [h_{ie} + (1 + h_{fe})\ (1\ K \parallel 10\ K)]$

$= 82\ K \parallel [1.1\ K + (1 + 50)\ (0.909\ K)]$

$= \mathbf{30\ k\Omega}$

$\therefore \quad \frac{V_{i2}}{V_{i1}} = \frac{-50 \times 523.8}{30 \times 10^3} = -0.888$

$\therefore \quad A_v = -158.36 \times -0.888$

$= \mathbf{140.62}$

Step 6 : Calculate β

$$\beta = \frac{V_f}{V_o} = \frac{1\,K}{10\,K}$$

$= \mathbf{0.1}$

Step 7 : Calculate A_{Vf}, R_{if} and R'_{of}

$D = 1 + \beta A_v = 1 + 0.1 \times (140.62)$

$= \mathbf{15.062}$

$$A_{Vf} = \frac{A}{D} = \frac{140.62}{15.062}$$

$= \mathbf{9.336}$

$R_{if} = R_i \times D = 30 \times 10^3 \times 15.062$

$$= 451.86\ k\Omega$$

$$R'_o = R_{L2} = 3.484\ k\Omega$$

$$R'_{of} = \frac{R'_o}{D} = \frac{3.484 \times 10^3}{15.062}$$

$$= 231.31\Omega$$

Example 1.17 : *The two stage feedback shown in Fig. 1.53 uses FET. The parameters are* $r_d = 10\ K$ *and* $\mu = 40$.

i) Identify the topology of feedback

ii) Calculate D, A_{Vf}, R_{if}, R_{of} *and* R'_{of}.

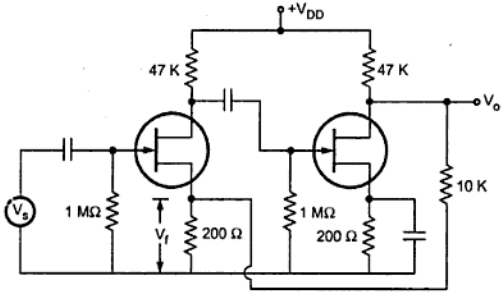


Fig. 1.53

Solution : Step 1 : Identify topology

By shorting output voltage ($V_o = 0$), feedback voltage V_f becomes zero and hence it is voltage sampling. The feedback voltage is applied in series with the input voltage hence the topology is voltage series feedback.

Step 2 and Step 3 : Find input and output circuit.

To find input circuit, set $V_o = 0$. This places the parallel combination of resistors 10 K and 200 Ω at first source. To find output circuit, set $I_i = 0$. This places the resistors 10 K and 200 Ω in series across the output. The resultant circuit is shown in Fig. 1.54.

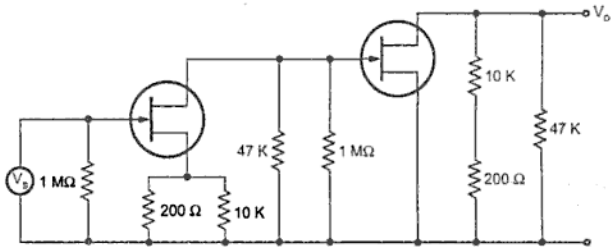


Fig. 1.54

Step 4 : Replace FET with its equivalent circuit

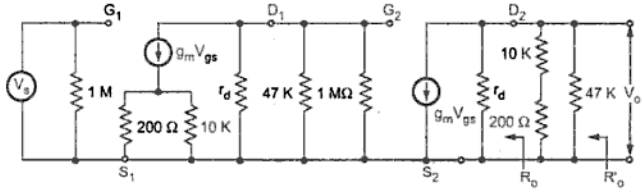


Fig. 1.55

Step 5 : Find open loop transfer gain

$$A_V = \frac{V_o}{V_s} = A_{v1}\, A_{v2}$$

$$A_{v2} = \frac{-\mu\, R_{L2}}{R_{L2} + r_d}$$

Where $R_{L2} = (10\text{ K} + 200\ \Omega) \parallel 47\text{ K}$

$= \mathbf{8.38\ K}$

$\therefore$ $$A_{v2} = \frac{-40 \times 8.38 \times 10^3}{8.38 \times 10^3 + 10 \times 10^3}$$

$= \mathbf{-18.237}$

$$A_{v1} = \frac{\mu\, R_{Deff}}{r_d + R_{Deff} + (1+\mu)\, R_s}$$

Where $R_{Deff} = R_D \parallel R_{G2} = 47\text{ K} \parallel 1\ \text{M}\Omega$

$= \mathbf{44.89\ k\Omega}$

$$A_{v1} = \frac{-40 \times 44.98 \times 10^3}{10 \times 10^3 + 44.89 \times 10^3 + (1+40)(10K \parallel 200)}$$

$$= \mathbf{-28.59}$$

$$\therefore \quad A_v = -28.59 \times -18.237$$

$$= \mathbf{521.39}$$

Step 6 : Calculate β

$$\beta = \frac{V_f}{V_o} = \frac{200}{10 \times 10^3}$$

$$= \mathbf{0.02}$$

Step 7 : Calculate D, A_{Vf}, R_{if}, R'_{of}

$$D = 1 + \beta A_v = 1 + 0.02 \times 521.39$$

$$= \mathbf{11.4278}$$

$$A_{Vf} = \frac{A_V}{D} = \frac{521.39}{11.4278} = \mathbf{45.62}$$

$$R_i = R_G = \mathbf{1\ M\Omega}$$

$$R_{if} = R_i \times D = 1 \times 10^6 \times 11.4278$$

$$= \mathbf{11.4278\ M\Omega}$$

$$R_o = r_d$$

$$= \mathbf{10\ K}$$

$$R_{of} = \frac{R_o}{D} = \frac{10 \times 10^3}{11.4278} = \mathbf{875\ \Omega}$$

$$R'_o = r_d \parallel R_{L2} = 10\ K \parallel 8.38\ K$$

$$= \mathbf{4.559\ k\Omega}$$

$$\therefore \quad R'_{of} = \frac{R'_o}{D} = \frac{4.559 \times 10^3}{11.4278}$$

$$= \mathbf{399\ \Omega}$$

Example 1.18 : *The circuit shows three stage FET amplifier. The identical FETs have following parameters*
$r_d = 8\ k\Omega$, $g_m = 5\ mA/V$, $R_g = 1\ M\Omega$,
$R_g = R_1 + R_2$, $R_1 = 50\ \Omega$, $R_d = 40\ k\Omega$
Calculate voltage gain including feedback.

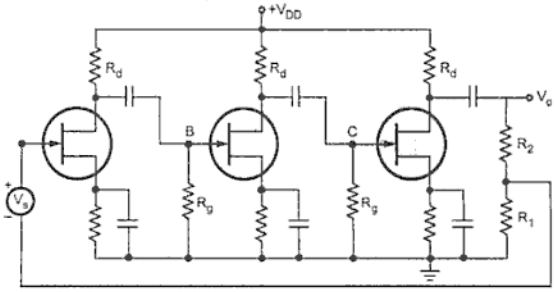


Fig. 1.56

Solution : Here, output voltage is sampled and fed in series with the input signal. Hence the topology is voltage series feedback.

The open loop voltage gain for one stage is given as

$$A_v = -g_m R_{eq}$$

Where $R_{eq} = r_d \parallel R_d \parallel (R_{11} + R_2) = 8\ K \parallel 40\ K \parallel (1\ M\Omega)$

$$= \mathbf{6.62\ k\Omega}$$

$$A_v = -5 \times 10^3 \times 6.62 \times 10^3$$

$$= \mathbf{-33.11}$$

Overall voltage gain $= |A_{v\,mid}|^3 = |-33.11|^3$

$$= -36306$$

$$\beta = \frac{R_1}{R_1 + R_2} = \frac{50}{1 \times 10^6}$$

$$= \mathbf{5 \times 10^{-5}}$$

$\therefore$ $D = 1 + \beta\,|A_v| = 1 + (5 \times 10^{-5}) \times (36306)$

$$= \mathbf{2.8153}$$

$\therefore$ $$|A_{Vf}| = \frac{A_{Vf}}{1 + |A_v|\beta}$$

$$= \frac{36306}{2.8153} = 12.895 \times 10^3$$

$\therefore$ $$A_{Vf} = \mathbf{-12.895 \times 10^3}$$

Example 1.19 : *In the Ex. 1.18, if output is taken between point B and ground, calculate* A_{vf}

Solution : We know that

$$A_V = -33.11$$

Here $$\beta = \frac{V_f}{V_B} = \frac{V_f}{V_o} \times \frac{V_o}{V_C} \times \frac{V_C}{V_B}$$

Where V_B and V_C are voltages at point B and C, respectively

$$\therefore \quad \beta = \frac{V_f}{V_o} \times A_{V3} \times A_{V2} \qquad \because \frac{V_o}{V_C} = A_{V3} \text{ and } \frac{V_C}{V_B} = A_{V2}$$

$$\therefore \quad \beta = 5 \times 10^{-5} \times (-33.11) \times (-33.11)$$

$$= \mathbf{0.0548}$$

$$\therefore \quad |A_{Vf}| = \frac{A_{Vf}}{1+\beta|A_V|} = \frac{33.11}{1+0.0548 \times 33.11} = 11.76$$

$$\therefore \quad A_{Vf} = \mathbf{-11.76}$$

Example 1.20 : *For the circuit shown in Fig. 1.57.*

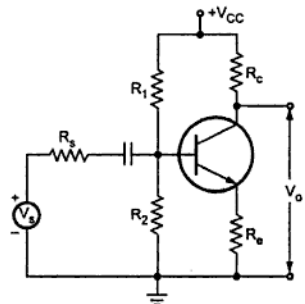


Fig. 1.57

i) Identify topology used in feedback amplifier

ii) Show that voltage gain with feedback

$$A_{Vf} = \frac{V_o}{V_s} = \frac{-h_{fe} R_c \left(\dfrac{1}{1+\dfrac{R_s}{R_b}} \right)}{R'_s + h_{ie} + (1+h_{fe}) R_e}$$

Where $R'_s = R_s \parallel R_1 \parallel R_2$

Solution : Step 1 : Identify topology

By shorting output ($V_o = 0$), feedback voltage does not become zero. By opening the output loop feedback becomes zero and hence it is current sampling. The feedback is applied in series with the input signal, hence topology used is current series feedback.

Step 2 and Step 3 : Find input and output circuit

To find input circuit, set $I_o = 0$. This places R_e in series with input. To find output circuit $I_i = 0$. This places R_e in the output side. The resultant circuit is shown in Fig. 1.58.

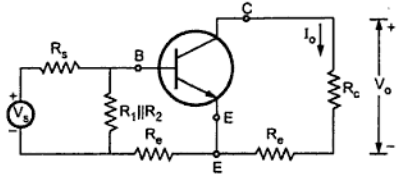


Fig. 1.58

Step 4 : Replace transistor with its h-parameter equivalent

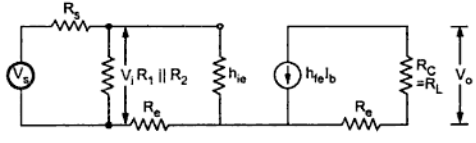


Fig. 1.59

Step 5 : Find open loop transfer gain

From equation (13) of section 1.12 we have

$$A_{Vf} = \frac{I_o R_L}{V_i} = G_{Mf} R_L$$

$$= \frac{-h_{fe} R_L}{R'_s + h_{ie} + (1 + h_{fe}) R_e}$$

Here $$R'_s = R_s \| R_1 \| R_2$$

$$= R_s \| R_b \qquad \because R_b = R_1 \| R_2$$

$\therefore$ $$\frac{V_o}{V_s} = \frac{V_o}{V_i} \times \frac{V_i}{V_s}$$

Where $$\frac{V_i}{V_s} = \frac{R_b}{R_s + R_b}$$

$$\therefore \quad \frac{V_o}{V_s} = \frac{-h_{fe}R_L}{R'_s + h_{ie} + (1+h_{fe})R_e} \times \frac{R_b}{R_s + R_b}$$

Dividing both numerator and denominator by $R_s + R_b$ we get

$$A_{Vf} = \frac{V_o}{V_s} = \frac{-h_{fe}R_c \times \frac{R_b}{R_b + R_s}}{R'_s + h_{ie} + (1+h_{fe})R_e} \quad \because R_L = R_c$$

$$= \frac{-h_{fe}R_C\left(\frac{1}{1+\frac{R_s}{R_b}}\right)}{R'_s + h_{ie} + (1+h_{fe})R_e}$$

Example 1.21 : *Identify the topology of feedback in the circuit of Fig. 1.60 giving justification. Two transistors are identical with h_{ie} = 2 K and h_{fe} = 100, Calculate*

i) R_{if} ii) A_{if} iii) A_{Vf}

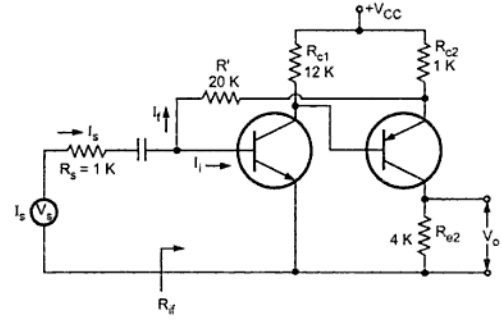


Fig. 1.60

Solution : Step 1 : Identify topology

Making output voltage zero (V_o = 0); feedack does not become zero and hence it is not voltage sampling. By opening the output loop feedback becomes zero and hence it is a current sampling. As $I_i = I_s - I_f$, the feedback current appears in shunt with the input signal and hence the topology is current shunt feedback.

Step 2 and Step 3 : Find input and output circuit

To find input circuit, set I_o = 0. This gives series combination of resistors 20 K and 1 K across of the input of the first transistor. To find output circuit, set V_i = 0. This gives

parallel combination of resistors 20 K and 1 K at emitter of the second transistor. The resultant circuit is shown in Fig. 1.61.

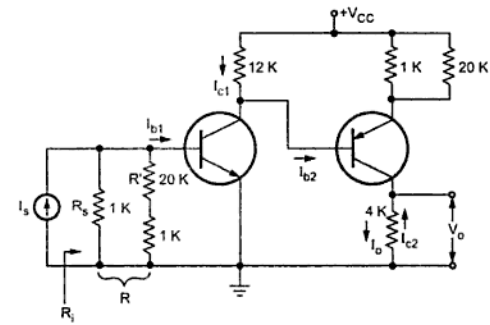


Fig. 1.61

Step 4 : Find open circuit current gain

$$A_I = \frac{I_o}{I_s} = \frac{-I_{c2}}{I_s} = \frac{-I_{c2}}{I_{b2}} \times \frac{I_{b2}}{I_{c1}} \times \frac{I_{c1}}{I_{b1}} \times \frac{I_{b1}}{I_s}$$

$$\frac{-I_{c2}}{I_{b2}} = -h_{fe} = -100$$

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{c1}}{R_{c1} + R_{i2}}$$

Where $R_{i2} = h_{ie} + (1 + h_{fe})\, R_e = 2 \times 10^3 + (1 + 100)\ (1\ K \parallel 20\ K)$

$= 98.19\ K$

$$\therefore \quad \frac{I_{b2}}{I_{c1}} = \frac{-12\ K}{12\ K + 98.19\ K} = -0.109$$

$$\frac{I_{c1}}{I_{b1}} = h_{fe} = 100$$

$$\frac{I_{b1}}{I_s} = \frac{1\ K \parallel (20\ K + 1\ K)}{h_{ie} + 1\ K \parallel (20\ K + 1K)} = 0.323$$

$$\therefore \quad A_I = (-100) \times (-0.109) \times (100) \times (0.323)$$

$$= 352$$

Step 5 : Calculate β

$$\beta = \frac{I_f}{I_o} = \frac{R_{e2}}{R_{e2} + R'} = \frac{4\ K}{4\ K + 20\ K}$$

$$= 0.1667$$

$$\therefore \quad D = 1 + \beta A_I = 1 + (0.1667) \times 352$$

$$= 59.67$$

$$A_{If} = \frac{A_I}{1+\beta A_I} = \frac{A_I}{D} = \frac{352}{59.67}$$

$$= 5.90$$

$$R_i = 1\ K \parallel (1\ K + 20\ K) \parallel R_{i1}$$

$$= 1\ K \parallel 21\ K \parallel 2\ K \qquad \because R_{i1} = h_{ie} = 2K$$

$$= 646\ \Omega$$

$$R_{if} = \frac{R_i}{1+\beta A_I} = \frac{R_i}{D} = \frac{646}{59.67}$$

$$= 10.82\ \Omega$$

$$R_o = \infty \qquad \therefore \ R_{of} = \infty \qquad \because h_{oe} = 0$$

$$R'_o = R_o \parallel R_{c2} = \infty \parallel 4\ K = 4\ K$$

$$R'_{of} = R'_o \frac{(1+\beta A_i)}{(1+\beta A_I)} = R'_o = 4\ K$$

$$A_{Vf} = \frac{A_{If} R_L}{R_s} = \frac{5.9 \times 4K}{1K}$$

$$= 23.6$$

Example 1.22 : *For the circuit shown in Fig. 1.62. Calculate A_{Vf}, R_{if} and R_{of}. Transistor parameters are h_{ie} = 1 K, h_{fe} =100, h_{re} = 0.*

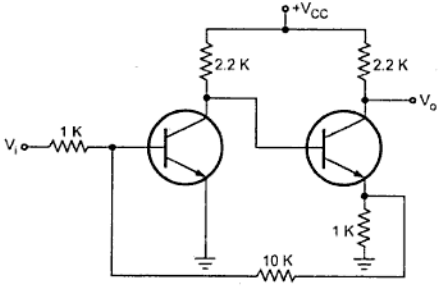


Fig. 1.62

Solution : Step 1 : Identify topology

$V_o = 0$, does not make feedback zero, but $I_o = 0$ makes feedback to become zero and hence it is current sampling. The feedback is fed in shunt with the input signal, hence topology is current shunt feedback.

Step 2 and Step 3 : Find input and output circuit

To find input circuit, set $I_o = 0$. This gives series combination of R_{e2} and 10 K across the input. To find output circuit, set $V_i = 0$. This gives parallel combination of R_{e2} and 10 K at E_2. The resultant circuit is shown in Fig. 1.63.

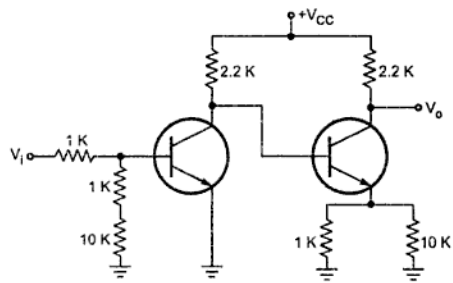


Fig. 1.63

Step 4 : Replace transistor with its h-parameter equivalent

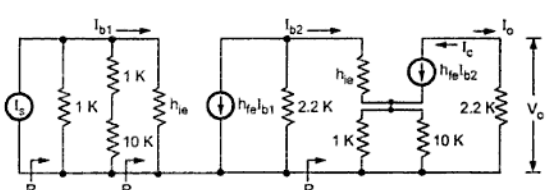


Fig. 1.64 h-parameter equivalent circuit

Step 5 : Find open loop current gain

$$A_I = \frac{I_o}{I_s} = \frac{-I_c}{I_s}$$

$$= \frac{I_o}{I_{b2}} \frac{I_{b2}}{I_{c1}} \frac{I_{c1}}{I_{b1}} \frac{I_{b1}}{I_s}$$

$$\frac{I_o}{I_{b2}} = -h_{fe} = -100$$

$$\frac{I_{c1}}{I_{b1}} \times \frac{I_{b2}}{I_{c1}} = \frac{-h_{fe} R_{c1}}{R_{c1} + R_{i2}} \qquad \because \frac{I_{b2}}{I_{c1}} = \frac{R_{c1}}{R_{c1} + R_{i2}}$$

Where

$$R_{i2} = h_{ie} + (1 + h_{fe})\ (1\ K \parallel 10\ K)$$

$$= 1\ K + (1 + 100)\ (1\ K \parallel 10\ K)$$

$$= \mathbf{92.818\ K}$$

$\therefore$

$$\frac{I_{b2}}{I_{b1}} = \frac{-100 \times 2.2 \times 10^3}{92.818 \times 10^3 + 2.2 \times 10^3}$$

$$= -2.315$$

$$\frac{I_{b1}}{I_s} = \frac{1\ K \parallel (1\ K + 10\ K)}{h_{ie} + 1\ K \parallel (10\ K + 1\ K)}$$

$$= 0.478$$

$$A_I = (-100) \times (-2.315) \times 0.478$$

$$= \mathbf{110.7}$$

Step 6 : Calculate β

$$\beta = \frac{R_{e2}}{R_{e2} + R'} = \frac{1K}{1K + 10K} = \mathbf{0.09}$$

Step 7 : Calculate D, A_{If}, R_{if}, R_{of} and A_{vf}

$$D = 1 + \beta A_I = 1 + (0.09)\ (110.7)$$

$$= \mathbf{11.063}$$

$$A_{If} = \frac{A_I}{1 + \beta A_I} = \frac{A_I}{D} = \frac{110.7}{11.063}$$

$$= \mathbf{10}$$

$$R_i = 1\ K \parallel (10\ K + 1\ K) \parallel R_{i1}$$

$$= 1\ K \parallel (11\ K) \parallel 1\ K \qquad \because R_{i1} = h_{ie} = 1\ K$$

$$= \mathbf{478\ \Omega}$$

$$R_{if} = \frac{R_i}{D} = \frac{478}{11.063} = \mathbf{43.20\ \Omega}$$

$$R_o = \infty$$

$\therefore$ $R_{of} = R_o D = \infty \because h_{oe} = 0$

$R'_o = 2.2\ k\Omega$

$R'_{of} = R'_o \frac{(1+\beta A_i)}{(1+\beta A_I)} = R'_o$

$= 2.2\ k\Omega$

Example 1.23 : *For the circuit shown in Fig. 1.65 has following parameters : $h_{fe} = 100$ $h_{ie} = 1.1$ K, and h_{re} and $h_{oe} = 0$. Determine*

i) $R_{mf} = \frac{V_o}{I_s}$, *ii)* $A_{vf} = \frac{V_o}{V_s}$

iii) R_{if} *and* *iv)* R'_{of}

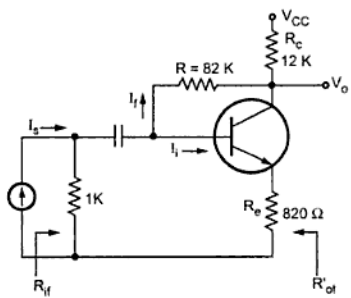


Fig. 1.65

Solution : Step 1 : Identify topology

Here output voltage is sampled and fed in shunt with the input signal, such that, $I_s - I_f = I_i$ hence topology is voltage shunt feedback.

Step 2 : Find input and output circuit

To find input circuit, set $V_o = 0$. This places resistor R across the input. To find output circuit, set $V_i = 0$. This places resistor R across the output. The resultant circuit is shown in Fig. 1.66.

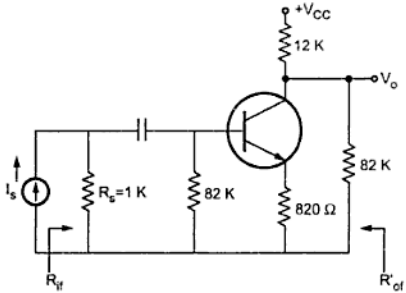


Fig. 1.66 h-parameter equivalent circuit

Step 4 : Replace transistor with its h-parameter equivalent circuit

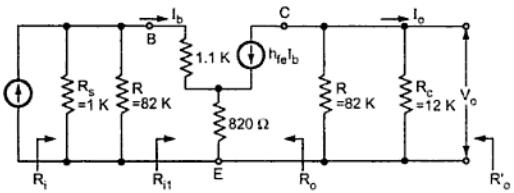


Fig. 1.67

Step 5 : Find the open circuit transresistance

$$R_M = \frac{V_o}{I_s} = \frac{R_c I_o}{I_s} = \frac{-R_c I_c}{I_s}$$

$$= R_c \frac{-I_c}{I_b} \frac{I_b}{I_s}$$

$$\frac{-I_c}{I_b} = \frac{-h_{fe} R}{R + R_c} = \frac{-100 \times 82 \times 10^3}{82 \times 10^3 + 12 \times 10^3}$$

$$= -87.23$$

$$\frac{I_b}{I_s} = \frac{R_s \| R}{R_s \| R + R_{i1}}$$

Where

$$R_{i1} = h_{ie} + (1 + h_{fe}) R_e$$

$$= 1.1 \times 10^3 + (101)\ 820$$

$$= 83.92 \text{ K}$$

$$\therefore \quad \frac{I_b}{I_s} = \frac{(1\times10^3)\,||\,(82\times10^3)}{(1\times10^3)\,||\,(82\times10^3)+83.92\times10^3}$$

$$= 0.0116$$

$$\therefore \quad R_M = \frac{V_o}{I_s} = 12\times10^3\times(-87.23)\times0.0116$$

$$= \mathbf{-12.142\ K}$$

Step 6 : Calculate β

$$\beta = \frac{I_f}{I_o} = \frac{V_i - V_o}{V_o R}$$

$$= \frac{-1}{R} \quad \because V_o > V_i$$

$$\therefore \quad \beta = \frac{-1}{82\,K} = \mathbf{-1.22\times10^{-5}}$$

Step 7 : Calculate D, R_{Mf}, A_{Vf}, R_{if} and R'_{of}

$$D = 1 + \beta R_M$$

$$= 1 + (-1.22\times10^{-5})\,(-12.142\times10^3)$$

$$= \mathbf{1.148}$$

$$R_{Mf} = \frac{R_M}{D} = \frac{-12.142\ K}{1.148} = \mathbf{-10.57\ K}$$

$$A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s}$$

$$= \frac{R_{Mf}}{R_s} = \frac{-10.57\times10^3}{1\times10^3} \quad \because R_{MF} = \frac{V_o}{I_s}$$

$$= \mathbf{-10.57}$$

$$R_i = R_s \,||\, R \,||\, R_{i1} = 1\ K \,||\, 82\ K \,||\, 83.92\ K$$

$$= \mathbf{0.976\ K}$$

$$\therefore \quad R_{if} = \frac{R_i}{D} = \frac{0.976\times10^3}{1.148} = \mathbf{850\ \Omega}$$

$$R_o = \infty \qquad \therefore R_{of} = \frac{\infty}{D} = \infty \quad \because h_{oe} = 0$$

$$R'_o = R_c \,||\, R = 12\ K \,||\, 82\ K$$

$$= 10.468 \text{ K}$$

$$R'_{of} = \frac{R'_o}{D} = \frac{10.468 \times 10^3}{1.148}$$

$$= 9.118 \text{ K}$$

Example 1.24 : *The two stage amplifier shown in the Fig. 1.68 has identical transistors with parameters h_{ie} = 2 K, h_{fe} = 100, and h_{re} = 0. Calculate a) A_{Vf} b) R_{if} c) R'_{of}*

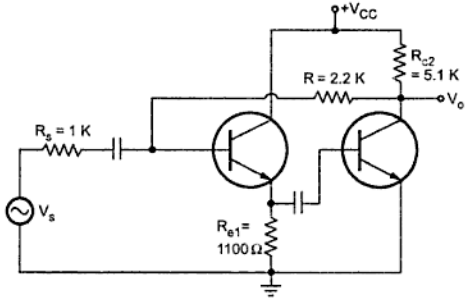


Fig. 1.68

Solution : Step 1 : Identify topology

Here output voltage is sampled and fed in shunt with the input signal such that, $I_s - I_f = I_i$, hence topology is voltage shunt feedback.

Step 2 and Step 3 : Find input and output circuit

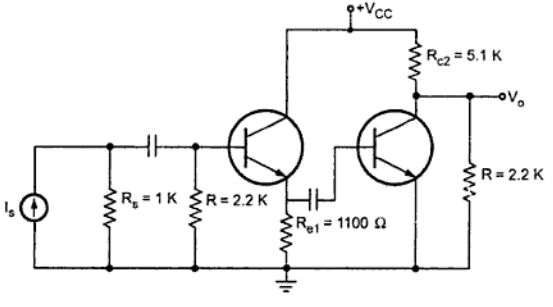


Fig. 1.69

To find input circuit, set $V_o = 0$. This places resistor R across the input. To find output circuit, set $V_i = 0$. This places resistor R across input. The resultant circuit is as shown in the Fig. 1.69. The circuit shows voltage source replaced by current source.

Step 4 : Replace transistors with their h-parameter equivalent circuits.

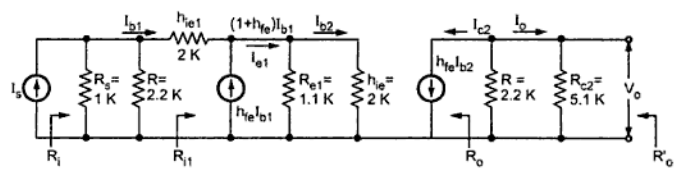


Fig. 1.70 h-parameter equivalent circuit

Step 5 : Find open loop transfer gain

$$R_M = \frac{V_o}{I_s} = \frac{R_{c2}I_o}{I_s}$$

$$= R_{c2} \cdot \frac{I_o}{I_{b2}} \frac{I_{b2}}{I_{e1}} \frac{I_{e1}}{I_{b1}} \frac{I_{b1}}{I_s}$$

$$\frac{I_o}{I_{b2}} = \frac{-h_{fe}R}{R+R_{c2}} = \frac{-100\times 2.2\times 10^3}{2.2\times 10^3 + 5.1\times 10^3}$$

$$= -30.137$$

$$\frac{I_{b2}}{I_{e1}} \times \frac{I_{e1}}{I_{b1}} = \frac{(1+h_{fe})R_{e1}}{R_{e1}+h_{ie}} = \frac{101\times 1.1\times 10^3}{1.1\times 10^3 + 2\times 10^3}$$

$$= 35.84$$

$$\frac{I_{b1}}{I_s} = \frac{R_s \| R}{(R_s \| R) + R_{i1}}$$

Where $$R_{i1} = h_{ie} + (1 + h_{fe})\, R_e$$

$$= 2\times 10^3 + (101) \times 1.1 \times 10^3$$

$$= \mathbf{113.1\ k\Omega}$$

$$\frac{I_{b1}}{I_s} = \frac{1\times 10^3 \| 2.2\times 10^3}{1\times 10^3 \| 2.2\times 10^3 + 113.1\times 10^3}$$

$$= 6.04 \times 10^{-3}$$

$\therefore$ $$R_M = 5.1 \times 10^3 \times (-30.137) \times 35.84 \times 6.04 \times 10^{-3}$$

$$= \mathbf{-33.539\ K}$$

Step 6 : Calculate β

$$\beta = \frac{I_f}{I_o} = \frac{V_i - V_o}{V_o R}$$

$$= \frac{-1}{R} \qquad \because V_o > V_i$$

$$= -\frac{1}{2.2 \times 10^3}$$

$$= \mathbf{-4.545 \times 10^{-4}}$$

Step 7 : Calculate D, R_{Mf}, A_{Vf}, R_{if} and R'_{of}

$$D = 1 + \beta R_M$$

$$= 1 + (-4.545 \times 10^{-4})(-33.539 \times 10^3)$$

$$= \mathbf{16.245}$$

$$R_{Mf} = \frac{R_M}{D} = \frac{-33.539 \times 10^3}{16.245}$$

$$= \mathbf{-2.065\ K}$$

$$A_{Vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s}$$

$$= \frac{R_{Mf}}{R_s} = \frac{-2.065 \times 10^3}{1 \times 10^3}$$

$$= \mathbf{-2.065}$$

$$R_i = R_s \parallel R \parallel R_{i1} = 1\ K \parallel 2.2\ K \parallel 113.1\ K$$

$$= \mathbf{638\ \Omega}$$

$\therefore$

$$R_{if} = \frac{R_i}{D} = \frac{683}{16.245}$$

$$= \mathbf{42\ \Omega}$$

$$R_o = \infty \qquad \therefore R_{of} = \frac{\infty}{D} = \infty$$

$$R'_o = R \parallel R_{c2} = 2.2 \times 10^3 \parallel 5.1 \times 10^3$$

$$= \mathbf{1.537\ k\Omega}$$

$$R'_{of} = \frac{R'_o}{D} = \frac{1.537 \times 10^3}{16.245}$$

$$= \mathbf{94.61\ \Omega}$$

Example 1.25 : *In the FET amplifier shown in Fig. 1.71 has the following parameters* $r_d = 40\ k\Omega$, $g_m = 2.5\ mA/V$. *Assume all capacitors to be arbitrarily large. Calculate D.* R_{Mf}, A_{Vf}, R_{if}, R_{of} *and* R'_{of}.

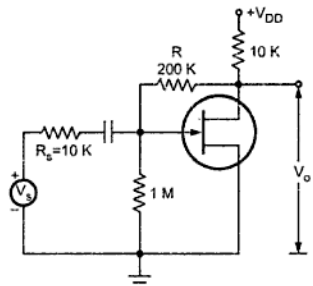


Fig. 1.71

Solution : Step 1 : Identify topology

By making $V_o = 0$, feedback current becomes zero. Hence it is a voltage sampling. The feedback is fed in shunt with the input signal and thus the topology is voltage shunt feedback.

Step 2 and Step 3 : Find input and output circuit.

To find input circuit, set $V_o = 0$. This places resistor R across the input. To find output circuit, set $V_i = 0$. This places resistor R across output. The resultant circuit is shown in Fig. 1.72.

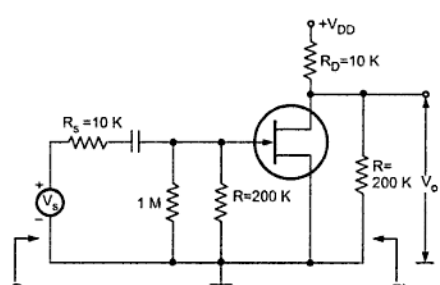


Fig. 1.72

Step 4 : Replace FET with its equivalent circuit

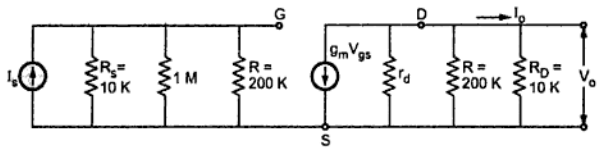


Fig. 1.73

Step 5 : Find open loop transresistance

$$R_M = \frac{V_o}{I_s} = \frac{-g_m V_{gs} R_{eff}}{I_s}$$

Where $R_{eff} = r_d \parallel R \parallel R_D = 40\ K \parallel 200\ K \parallel 10\ K$

$= \mathbf{7.69\ k\Omega}$

and $V_{gs} = I_s R_i = I_s \times R_s \parallel 1M \parallel R$

$= I_s \times 10\ K \parallel 1M \parallel 200\ K$

$= \mathbf{9.43 \times 10^3\ I_s}$

$$R_M = \frac{-g_m \times 9.43 \times 10^3 I_s \times 7.69 \times 10^3}{I_s}$$

$= -2.5 \times 10^{-3} \times 9.43 \times 10^3 \times 7.69 \times 10^3$

$= \mathbf{-181.29\ K}$

Step 6 : Calculate β

$$\beta = \frac{I_f}{I_o} = \frac{V_i - V_o}{V_o R}$$

$$= \frac{-1}{R} \qquad \because (V_o > V_i)$$

$$= -\frac{1}{200 \times 10^3} = \mathbf{-5 \times 10^{-6}}$$

Step 7 : Calculate D, R_{Mf}, A_{Vf}, R_{of} and R'_{of}

$$D = 1 + \beta R_M$$

$= 1 + (-5 \times 10^{-6})(-181.29 \times 10^3)$

$= \mathbf{1.9}$

$$R_{Mf} = \frac{R_M}{D} = \frac{-181.29\ K}{1.9}$$

$$= \mathbf{-\ 95.415\ K}$$

$$A_{Vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s} = \frac{R_{Mf}}{R_s} = \frac{-95.415\times10^3}{10\times10^3}$$

$$= \mathbf{-\ 9.5415}$$

$$R_i = R_s \parallel M \parallel R = 10\ K \parallel 1\ M \parallel 200\ K$$

$$= \mathbf{9.43 \times 10^3}$$

$\therefore$ $$R_{if} = \frac{R_i}{D} = \frac{9.43\times10^3}{1.9}$$

$$= \mathbf{4.963\ \Omega}$$

$$R'_o = R_{eff} = r_d \parallel R \parallel R_D$$

$$= 40\ K \parallel 200\ K \parallel 10\ K$$

$$= \mathbf{7.69\ k\Omega}$$

$\therefore$ $$R_{of} = \frac{R'_o}{D} = \frac{7.69\times10^3}{1.9}$$

$$= \mathbf{4\ k\Omega}$$

Example 1.26 : *For the feedback amplifier shown in Fig. 1.74, calculate A_{vf}, R_{if}, R_{of}. Assume $h_{fe} = 50$ and $h_{ie} = 1.2$ kΩ.*

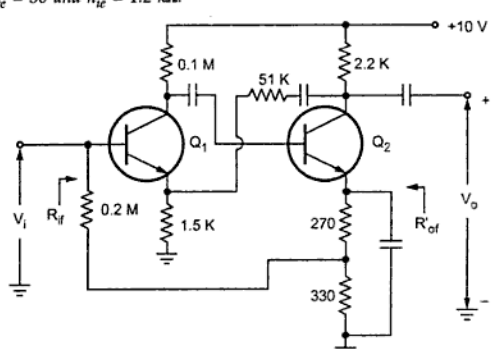


Fig. 1.74

Solution : Step 1 : Identify topology

The feedback voltage is applied across the resistance R_{e1} and it is in series with input signal. Hence feedback is voltage series feedback.

Step 2 and Step 3 : Find input and output circuit

To find input circuit, set $V_o = 0$, which gives parallel combination of R_{e1} with R_f at E_1 as shown in the Fig. 1.75. To find output circuit, set $I_i = 0$ opening the input node E_1 at emitter of Q_1, which gives series combination of R_f and R_{e1} across the output. The resultant circuit is shown in Fig. 1.75.

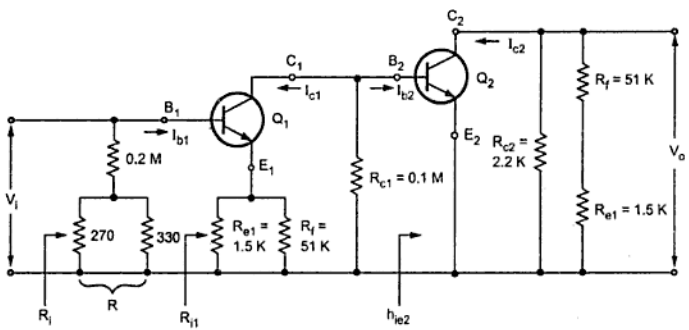


Fig. 1.75

Step 4 : Find open loop voltage gain (A_v)

$$R_{L2} = R_{c2} \parallel (R_f + R_{e1}) = 2.2 \text{ K} \parallel (51 \text{ K} + 1.5 \text{ K})$$

$$= \mathbf{2.11\ K}$$

$$A_{i2} = -h_{fe} = \mathbf{-50}$$

$$R_{i2} = h_{ie} = \mathbf{1.2\ k\Omega}$$

$$\therefore \quad A_{v2} = \frac{A_{i2} R_{L2}}{R_{i2}} = \frac{-50 \times 2.11 \text{ K}}{1.2 \text{ K}}$$

$$= \mathbf{-87.91}$$

$$R_{L1} = R_{C1} \parallel R_{i2} = 0.1 \text{ M} \parallel 1.2 \text{ K}$$

$$= \mathbf{1.185\ K}$$

$$A_{i1} = -h_{fe} = \mathbf{-50}$$

$$R_{i1} = h_{ie} + (1 + h_{fe}) R_e$$
$$= 1.2\ K + (1 + 50)\ (1.5\ K \parallel 51\ K)$$
$$= \mathbf{75.51\ K}$$

$$\therefore \quad A_{v1} = \frac{A_{i1} R_{L1}}{R_{i1}} = \frac{50 \times 1.185\ K}{75.51\ K}$$
$$= \mathbf{-0.784}$$

The overall gain without feedback is given is

$$A_v = A_{v1} \times A_{v2} = (-0.784) \times (-87.91)$$
$$= \mathbf{68.92}$$

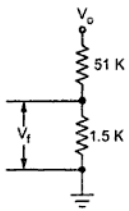


Fig. 1.76

Step 5 : Calculate β

$$\beta = \frac{V_f}{V_o} = \frac{1.5K}{51K + 1.5K}$$
$$= \mathbf{0.0285}$$

Step 6 : Calculate D, A_{vf}, R_{if} and R_{of}

$$D = 1 + \beta A_V$$
$$= 1 + (0.0285) \times 68.92$$
$$= \mathbf{2.964}$$

$$\therefore \quad A_{Vf} = \frac{A_V}{D} = \frac{68.92}{2.964}$$
$$= \mathbf{23.25}$$

$$R_i = R_{i1} \parallel R = 75.51\ K \parallel (0.2\ M + (270 \parallel 330))$$
$$= 75.51\ K \parallel 200.1485\ K$$
$$= \mathbf{54.82\ K}$$

$$\therefore \quad R_{if} = R_i \times D = 54.82\ K \times 2.964$$
$$= \mathbf{162.48\ K}$$

$$R_o = \infty \qquad \because \quad h_{oe} = 0$$
$$R'_o = R_o \parallel R_{c2} \parallel (R_f + R_{e1}) = R_o \parallel R_{L2}$$
$$= \infty \parallel 2.11\ K$$
$$= \mathbf{2.11\ K}$$

$$\therefore \quad R'_{of} = \frac{R'_o}{D} = \frac{2.11\,K}{2.964}$$

$$= 712\,\Omega$$

Example 1.27 : *For the circuit shown in Fig. 1.77.*

a. Identify the topology of feedback with proper reasoning

b. Find A_{If}, A_{vf}, R_{if}, R_{of}, A_I.

The transistor Q_1 and Q_2 have the following h-parameters : h_{ie} = 1.5 K and h_{fe} = 50. Assume C to be large enough to act as short at operating frequency.

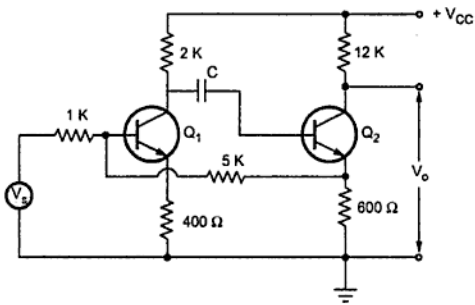


Fig. 1.77

Solution : Step 1 : Identify topology

The feedback is given from emitter of Q_2 to the base of Q_2. If $I_o = 0$ then feedback current through 5 K register is zero, hence it is current sampling. As feedback signal is mixed in shunt with input, the amplifier is current shunt feedback amplifier.

Step 2 and Step 3 : Find input and output circuit

The input circuit of the amplifier without feedback is obtained by opening the output loop at the emitter of Q_2 ($I_o = 0$). This places R' (5 K) in series with R_e from base to emitter of Q_1. The output circuit is found by shorting the input node, i.e. making $V_i = 0$. This places R' (5K) in parallel with R_e. The resultant equivalent circuit is shown in Fig. 1.78.

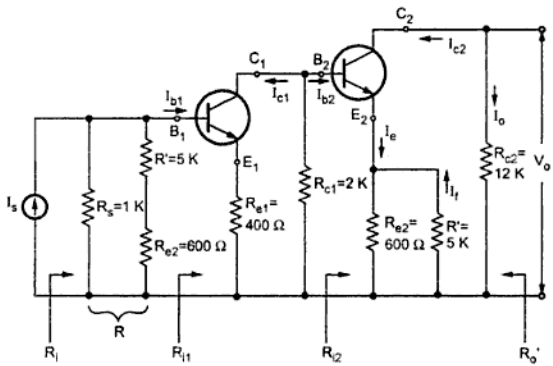


Fig. 1.78

Step 4 : Find open circuit transfer gain

$$A_I = \frac{I_o}{I_s} = \frac{-I_c}{I_s}$$

$$= \frac{-I_{c2}}{I_{b2}} \frac{I_{b2}}{I_{c1}} \frac{I_{c1}}{I_{b1}} \frac{I_{b1}}{I_s}$$

We know that $\frac{-I_{c2}}{I_{b2}} = A_{i2} = -h_{fe} = -50$ and

$$\frac{-I_{c1}}{I_{b1}} = A_{i1} = -h_{fe} = 50$$

$\therefore$ $\frac{I_{c1}}{I_{b1}} = 50$

Looking at Fig. 1.77 we can write

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{c1}}{R_{c1} + R_{i2}}$$

Where $R_{i2} = h_{ie} + (1 + h_{fe})\ (R_{e2} \parallel R')$

$$= 1.5\ K + (1 + 50)\ (600 \parallel 5\ K)$$

$$= \mathbf{28.82\ K}$$

$\therefore$ $\frac{I_{b2}}{I_{c1}} = \frac{-2\ K}{2\ K + 28.82\ K}$

$$= -0.0649$$

Looking at Fig. 1.78 we can write

$$\frac{I_{b1}}{I_s} = \frac{R}{R + R_{i1}}$$

Where $$R = R_3 \parallel (R' + R_e) = \frac{1\,K \times 56\,K}{1\,K + 5.6\,K}$$

$$= \mathbf{848\ \Omega}$$

and $$R_{i1} = h_{ie} + (1 + h_{fe})\, R_{e1}$$

$$= 1.5\ K + (1 + 50) \times 400 = \mathbf{21.9\ K}$$

$\therefore$ $$\frac{I_{b1}}{I_s} = \frac{848}{848 + 21.9\,K}$$

$$= 0.0372$$

Substituting the numerical values obtained in equations of A_I we get,

$$A_I = (-50) \times (-0.0649) \times (50) \times (0.0372)$$

$$= \mathbf{6}$$

Step 5 : Calculate β

$$\beta = \frac{I_f}{I_o} = \frac{R_{e2}}{R_{e2} + R'} = \frac{600}{600 + 5\,K}$$

$$= \mathbf{0.107}$$

Step 6 : Calculate D, A_{If}, A_{Vf}, R_{if}, R_{of}

$$D = 1 + \beta A_I = 1 + (0.107) \times 6$$

$$= \mathbf{1.642}$$

$$A_{If} = \frac{A_I}{D} = \frac{6}{1.642}$$

$$= \mathbf{3.654}$$

$$A_{Vf} = \frac{V_o}{V_s} = \frac{-I_{c2} R_{c2}}{I_s R_s}$$

$$= \frac{A_{If} R_{C2}}{R_S} = \frac{(3.654)(12\,K)}{1\,K}$$

$$= \mathbf{43.848}$$

$$R_i = R \parallel R_{i1} = 848 \parallel 21.9\ K$$

$$= 816.38\ \Omega$$

$$R_{if} = \frac{R_i}{D} = \frac{816.38}{1.642}$$

$$= 497.2\ \Omega$$

$$R_o = \infty \quad \because \quad h_{oe} = 0$$

$$\therefore \quad R_{of} = R_o\, D = \infty$$

$$R'_o = R_o \parallel R_{c2} = \infty \parallel 12\ K$$

$$= 12\ K$$

$$R'_{of} = R'_o \frac{1+\beta A_i}{1+\beta A_1} = R'_o = R_{c2} = 12\ K$$

Example 1.28 : *For feedback amplifier shown in Fig. 1.79, identify the feedback topology with proper justification.*

The transistors used are identical with the following parameters :

$h_{fe} = 200$, $h_{ie} = 2\ k\Omega$, $h_{re} = 10^{-4}$, $h_{oe} = 10^{-6}\ A/V$

Calculate

i) A_{Vf} *ii)* R_{if} *iii)* R_{of}

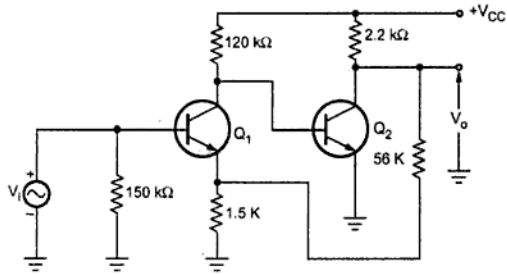


Fig. 1.79

Solution : Step 1 : Identify topology

The feedback voltage is applied across $R_{e1} = 1.5$ K, which is in series with input signal. Hence feedback is voltage series feedback.

Step 2 and Step 3 : Find input and output circuit

To find input circuit, set $V_o = 0$, which gives parallel combination of R_{e1} with R_f at E_1 as shown in the Fig. 1.80. To find output circuit, set $I_i = 0$ by opening the input node, E_1 at emitter of Q_1, which gives the series combination of R_f and R_{e1} across the output. The resultant circuit is shown in Fig. 1.80.

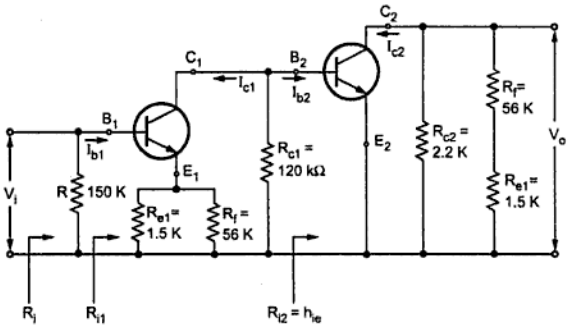


Fig. 1.80

Step 4 : Find the open loop voltage gain (A_V)

$$R_{L2} = R_{C2} \parallel (R_f + R_{e1})$$

$$= 2.2 \text{ K} \parallel (56 \text{ K} + 1.5 \text{ K})$$

$$= \mathbf{2.119\ K}$$

Since $h_{oe}\ R_{L2} = 10^{-6} \times 2.119 \text{ K} = 0.002119$ is less than 0.1 we use approximate analysis

$$A_{i2} = -h_{fe} = \mathbf{-200}$$

$$R_{i2} = h_{ie} = \mathbf{2\ k\Omega}$$

$$\therefore \quad A_{v2} = \frac{A_{i2} R_{L2}}{R_{i2}} = \frac{-200 \times 2.119 \text{ K}}{2 \text{ K}}$$

$$= \mathbf{-211.9}$$

$$R_{L1} = R_{C1} \parallel R_{i2} = 120 \text{ K} \parallel 2 \text{ K}$$

$$= \mathbf{1.967\ K}$$

Since $h_{oe}\ R_{L1} = 10^{-6} \times 1.967 = 0.001967$ is less than 0.1 we use approximate analysis

$$A_{i1} = -h_{fe} = \mathbf{-200}$$

$$R_{i1} = h_{ie} + (1 + h_{fe})\ R_e$$

$$= 2\ K + (1 + 200)\ (1.5\ K \parallel 56\ K)$$

$$= \mathbf{295.63\ K}$$

$$\therefore \quad A_{v1} = \frac{A_{i1} R_{L1}}{R_{i1}} = \frac{-200 \times 1.967\ K}{295\ 63\ K}$$

$$= \mathbf{-1.33}$$

The overall gain without feedback is

$$A_v = A_{v1} \times A_{v2} = (-1.33) \times (-211.9)$$

$$= \mathbf{281.82}$$

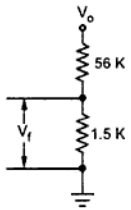


Fig. 1.81

Step 5 : Calculate β

$$\beta = \frac{V_f}{V_o}$$

$$= \frac{1.5\ K}{56\ K + 1.5\ K}$$

$$= \mathbf{0.026}$$

Step 6 : Calculate D, A_{Vf}, R_{if}, R_{of}

$$D = 1 + \beta A_V$$

$$= 1 + (0.026) \times 281.82 = \mathbf{8.327}$$

$$\therefore \quad A_{Vf} = \frac{A_V}{D} = \frac{281.82}{8.327}$$

$$= \mathbf{33.84}$$

$$R_i = R_{i1} \parallel R = 295.63\ K \parallel 150\ K$$

$$= \mathbf{99.5\ K}$$

$$\therefore \quad R_{if} = R_i \times D = 99.5 \times 8.327$$

$$= \mathbf{828.53\ K}$$

$$R_o = \frac{1}{h_{oe}} = \frac{1}{10^{-6}}$$

$$= \mathbf{1\ M\Omega}$$

$$R_{of} = \frac{R_o}{D} = \frac{1M}{8.327}$$

$$= \mathbf{120\ K}$$

$$R'_o = R_o \parallel R_{C2} \parallel (R_f + R_{e1}) = R_o \parallel R_{L2}$$

$$= 1\ M \parallel 2.119\ K$$

$$= \mathbf{2.1145\ K}$$

$$R'_{of} = \frac{R'_o}{D} = \frac{2.1145\,K}{8.327}$$

$$= \mathbf{254\ \Omega}$$

Example 1.29 : *For the circuit shown in Fig. 1.82, calculate : i) A_{vf} ii) R_{if} iii) R_{of} where these parameters have their usual meaning. The transistor parameters are : $h_{ie} = 1\ K$, $h_{re} = 0$, $h_{fe} = 100$ and $h_{oe} = 0$.*

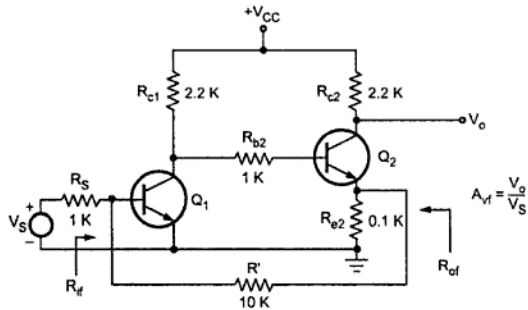


Fig. 1.82

Solution : This is a current shunt feedback amplifier open circuit transfer gain.

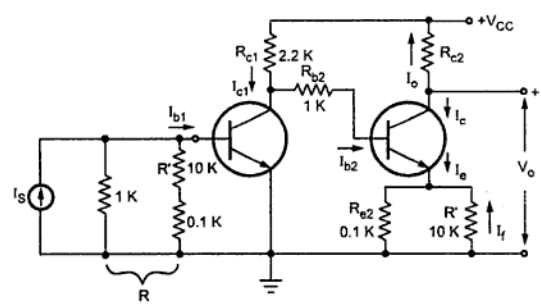


Fig. 1.83

$$A_I = -\frac{I_{c2}}{I_s} = -\frac{I_{c2}}{I_{b2}} \frac{I_{b2}}{I_{c1}} \frac{I_{c1}}{I_{b1}} \frac{I_{b1}}{I_s}$$

$$-\frac{I_{c2}}{I_{b2}} = A_{i2} = -h_{fe} = -100$$

$$-\frac{I_{c1}}{I_{b1}} = 100$$

$$R_{i2} = h_{ie} + (1 + h_{fe})(R_{e2} \parallel R') = 1\,K + (101)(0.1\,K \parallel 10\,K)$$

$$= 11\,K$$

$$\frac{I_{b2}}{I_{c1}} = \frac{-R_{c1}}{R_{c1} + (R_{i2} + R_{b2})}$$

$$= \frac{-2.2\,K}{2.2\,K + (11\,K + 1\,K)}$$

$$\frac{I_{b2}}{I_{c1}} = -0.155$$

$$\frac{I_{b1}}{I_s} = \frac{R}{R + h_{ie}}$$

$$R = R_s \parallel (R' + R_e) = 1\,K \parallel (10\,K + 0.1\,K)$$

$$= \mathbf{909.9\ \Omega}$$

$$\therefore \quad \frac{I'_b}{I_s} = \frac{909.9}{909.9 + 1\,K}$$

$$= 0.476$$

$$\therefore \quad A_I = (-100) \times (0.155) \times (100) \times (0.476) = \mathbf{737.8}$$

Calculation of β :

$$I_f = -\frac{I_o R_{e2}}{R_{e2} + R'} = -\frac{I_c R_{e2}}{R_{e2} + R'}$$

$$= \frac{I_o R_{e2}}{R_{e2} + R'}$$

$$\beta = \frac{I_f}{I_o} = \frac{R_{e2}}{R_{e2} + R'} = \frac{100}{100 + 10\,K}$$

$$D = 1 + \beta A_I = 1 + \left(9.9 \times 10^{-3}\right) \times 737.8$$

$$D = \mathbf{8.3}$$

$$A_{if} = \frac{A_I}{D} = 88.89$$

$$A_{vf} = \frac{V_o}{V_s} = -\frac{I_{c2} R_{c2}}{I_s R_s} = \frac{A_{if} R_{c2}}{R_s}$$

$$= \frac{88.89 \times 2.2\ K}{1\ K}$$

$$A_{vf} = \mathbf{195.558}$$

$$R_{it} = R \parallel h_{ie} = 909.9 \parallel 1000 = \mathbf{476\ \Omega}$$

$$R_{if} = \frac{R_i}{D} = \frac{476}{8.3} = \mathbf{57.35\ \Omega}$$

$$R_{of} = R_{c2} = \mathbf{2.2\ k\Omega}$$

Example 1.30 : *In a negative feedback amplifier A = 100, β = 0.02 and input signal volatge is 40 mV. Determine :*

i) Voltage gain with feedback

ii) Feedback voltage

iii) Output voltage

Solution : Given :

$A = 100, \beta = 0.02, V_i = 40 \times 10^{-3}$ V

i) Voltage gain with feedback $A_f = \frac{A_v}{D}$

Where, $D = 1 + \beta A_v = 1 + 0.02 \times 100 = \mathbf{3}$

$\therefore$ $A_{vi} = \frac{100}{3} = \mathbf{33.33}$

ii) Feedback voltage $V_f = \beta \cdot V_o = \beta \times A_{vf} \times V_i$

$= 0.02 \times 33.33 \times 40 \times 10^{-3}$

$= \mathbf{26.66\ mV}$

iii) Output voltage $V_o = A_{Vi} \times V_i = 33.33 \times 40 \times 10^{-3}$

$= \mathbf{1.333\ V}$

Example 1.31 : *Determine the voltage gain, input and output impedance with feedback for voltage series feedback having A = – 100, R_i = 10 k Ω, R_o = 20 k Ω for feedback of (a) β = – 0.1 and (b) β = – 0.5.*

Solution : For β = – 0.1, D = 1 + β Av = 1 + (– 0.1) (–100) = 11

i) Voltage gain $A_{vf} = \frac{A_v}{D}$

$\therefore$ $A_{vf} = \frac{-100}{11} = \mathbf{-9.09}$

ii) Input impedance $R_{if} = R_i D = 10 \times 11 = \mathbf{110\ k\Omega}$

iii) Output impedance $R_{of} = \frac{R_o}{D} = \frac{20K}{11}$

$= \mathbf{1.81\ k\Omega}$

For β = – 0.5, D = 1 + β A_v = 1 + (– 0.5) (– 100) = 51

i) Voltage gain $= \frac{A_v}{D} = \frac{-100}{51}$

$= \mathbf{-1.96}$

ii) Input impedance $R_{if} = R_i D = 10 \times 51 = \mathbf{510\ k\Omega}$

iii) Ouput impedance $R_{of} = \frac{R_o}{D} = \frac{20K}{51} = \mathbf{0.392\ k\Omega}$

Example 1.32 : *Which is the most commonly used feedback arrangement in cascaded amplifiers and why ?*

Solution : Voltage series feedback is the most commonly used feedback arrangement in cascaded amplifiers. Voltage series feedback increases input resistance and decreases output resistance. Increase in input resistance reduces the loading effect of previous stage and the decrease in output resistance reduces the loading effect of amplifier itself for driving the next stage.

Example 1.33 : *Voltage gain of an amplifier without feedback is 60 dB. It decreases to 40 dB with feedback. Calculate the feeback factor.*

Solution : Given A_v = 60 dB and A_{vf} = 40 dB

We know that,

$$A_{vf} = \frac{A_v}{1+\beta A_v}$$

$\therefore$ $A_{vf} + \beta A_v A_{vf} = A_v$

$$\therefore \quad \beta = \frac{A_v - A_{vf}}{A_v A_{vf}} = \frac{60-40}{60\times 40}$$

$$= 8.33 \times 10^{-3}$$

Example 1.34 : *An R-C coupled amplifier has a mid frequency gain of 400 and lower and upper 3 dB frequencies of 100 Hz and 15 kHz. A negative feedback with β = 0.01 is incorporated into amplifier circuit. Calculate :*

(i) Gain with feedback (ii) New bandwidth

Solution : Given : $A_v = 400$, $F_L = 100$ Hz, $f_H = 15$ kHz

$$\beta = 0.01$$

i) $$A_{vf} = \frac{A_v}{1+\beta A_v} = \frac{400}{1+(0.01\times 400)} = \mathbf{80}$$

ii) $$f_{Lf} = \frac{f_L}{1+\beta A_v} = \frac{100}{1+(0.01\times 400)} = \mathbf{20\ Hz}$$

iii) $$f_{Hf} = f_H \times (1+\beta A_v)$$

$$= 15 \times 10^3 \times [1+(0.01\times 400)]$$

$$= \mathbf{75\ kHz}$$

iv) New Bandwidth $= f_{Hf} - f_{Lf} = 75$ kHz $- 20$ Hz

$$= \mathbf{74.980\ kHz}$$

Review Questions

1. *What do you mean by voltage amplifier and current amplifier ? Give their equivalent circuit.*
2. *Draw the equivalent circuit of a transconductance amplifier.*
3. *Explain the sampling and mixing networks.*
4. *Define the feedback factor β.*
5. *Define negative and positive feedback.*
6. *Give topology for various types of feedback amplifiers.*
7. *Using a block diagram, derive the closed loop form transfer ratio of a feedback system in terms of the open gain.*
8. *Using a block diagram, derive the expression of closed loop forward transfer ratio with positive and negative feedbacks introduced in an amplifier.*
9. *Draw the block schematic of amplifier with negative feedback.*

10. *"The gain bandwidth product of an amplifier is not altered, when negative feedback introduced". Justify the statement.*
11. *What are the effects of negative feedback on distortion and gain of an amplifier ?*
12. *What are the advantages of negative feedback in amplifiers ?*
13. *Explain the consequences of introducing negative feedback in small signal amplifier.*
14. *Define desensitivity D ? For large values of D what is A_f ? What is the significance of this result ?*
15. *Discuss the effects of negative feedback on the frequency response of an amplifier.*
16. *Define 'Desensitivity' of transfer gain.*
17. *Compare the frequency response characteristics of an amplifier with and without negative feedback.*
18. *What are the steps to be carried out for the complete analysis of a feedback amplifier ?*
19. *With typical example compare current series and voltage shunt feedback amplifiers.*
20. *Draw the equivalent circuit of a voltage amplifier.*
21. *A feedback amplifier has an open loop gain of 600 and feedback factor $\beta = 0.01$. Find the closed loop gain with negative feedback.*
22. *The gain and distortion of an amplifier are 100 and 4% respectively. If a negative feedback with $\beta = 0.2$ is applied, find the new distortion in the system.*
23. *List out the steps that are carried out in obtaining the complete analysis of a feedback amplifier.*
24. *Write a note on voltage series feedback circuits.*
25. *Write a note on current series feedback circuits.*
26. *Write a note on current shunt feedback circuits.*
27. *Write a note on voltage shunt feedback circuits.*
28. *The distortion in an amplifier is found to be 3%, when the feedback ratio of negative feedback amplifier is 0.04. When the feedback is removed, the distortion becomes 15%. Find the open loop and closed loop gain.*
29. *Derive using a block diagram the closed loop forward transfer ratio A_f of a feedback system.*
30. *Derive the input impedance R_{if} of a voltage series and current shunt feedback amplifiers.*
31. *For the amplifier circuit given in Fig. 1.84 with $h_{fe} = 50$, $h_{ie} = 1.1$ KΩ, $h_{re} = h_{oe} = 0$.*
    i) Identify the type of negative feedback present.
    ii) Obtain the basic amplifier circuit.
    iii) Calculate the voltage gain, input resistance and output resistance of the given amplifier.

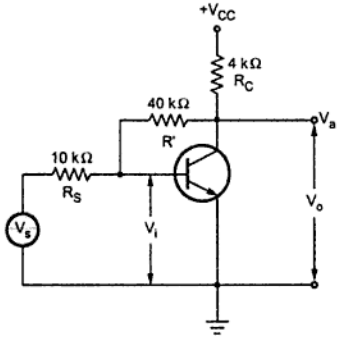


Fig. 1.84

32. *The circuit given in Fig. 1.85 has the following parameers R_C = 4 k Ω, R_S = 10 k Ω, h_{ie} = 1.1 K, h_{fe} = 50 and $h_{re} = h_{oe} = 0$. Find A_{vf}, R_{if} and R_{of}*

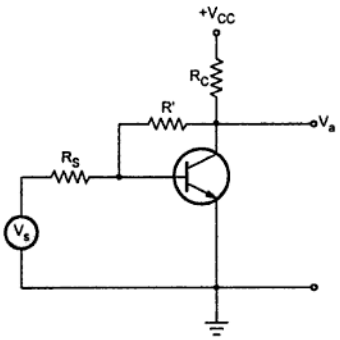


Fig. 1.85

33. *What is Nyquist criterion for stability of feedback amplifier ?*

Exercise Problems on Feedback Amplifiers

1. *Determine A_{Vf} for a feedback amplifier shown in Fig. 1.86 in which transistors used are identical and h_{ie} = 2 K, h_{fe} = 50, h_{re} and h_{oe} negligible.*

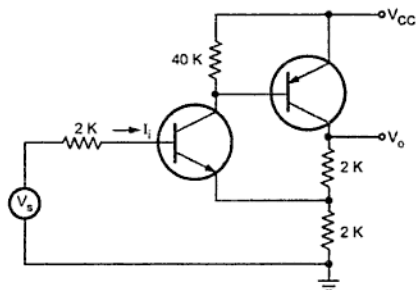


Fig. 1.86

(Ans. : A_{vf} = 1.977)

2. *Calculate β, A_V , A_{Vf} , R_{if} , R_{of} , R'_{of} for the feedback amplifier shown in Fig. 1.87.*
Given : h_{ie} = 1100 Ω, h_{fe} = 50, $h_{re} = 2.5 \times 10^{-4}$, $h_{oe} = 25 \times 10^{-6}$ *A/V.*

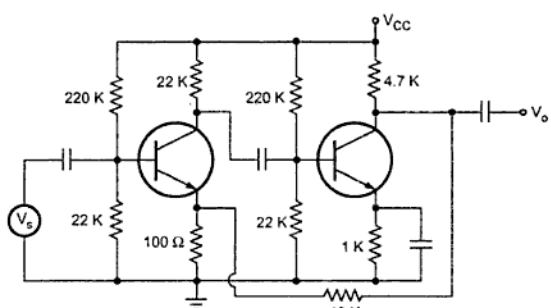


Fig. 1.87

(Ans. : i) β = 0.0099, ii) A_v = 1177, iii) A_{vf} = 93.04, iv) R_{if} = 77.8 K, v) R_{of} = ∞ , vi) R'_{of} = 253 Ω)

3. *For the feedback amplifier shown in Fig. 1.88,* $R_s = 0$, $h_{fe} = 50$, $h_{ie} = 1.1$ *K,* $h_{re} = h_{oe} = 0$ *and transistors are identical. Calculate* A_{vf}, R_{of}, R_{if}.

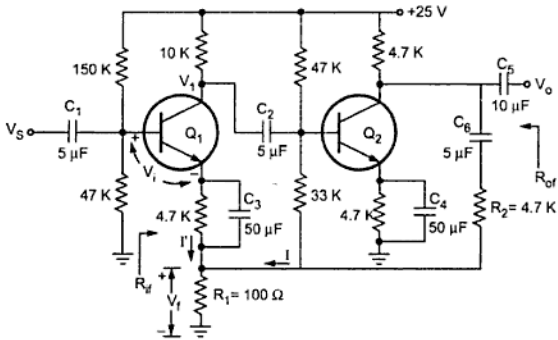


Fig. 1.88

(Ans. : i) $A_{Vf} = 47.5$, **ii)** $R_{of} = 24.4\ \Omega$, **iii)** $R_{if} = 106$ **K)**

4. *Determine* A_{Vf} , R_{if} *and* R'_{of} *for the circuit shown in Fig. 1.89.*
Given : $h_{ie} = 1$ *K,* $h_{fe} = 50$, h_{re} *and* h_{oe} *negligible.*

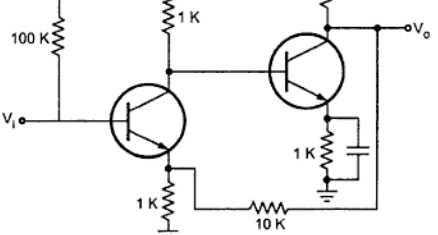


Fig. 1.89

(Ans. : i) $A_{Vf} = 9.9$, **ii)** $R_{if} = 294$ **K,** **iii)** $R_{of} = 374\ \Omega$)

5. *For the circuit shown in Fig. 1.90* $R_{c1} = 3$ *K.* $R_{c2} = 500\ \Omega$, $R_{e2} = 50\ \Omega$, $R' = R_s = 1.2K$, $h_{fe} = 50$, $h_{ie} = 1.1$ *K and* $1/h_{oe} = 40$ *K. Calculate*
i) $A'_v = V_{c2} / V_{i1}$ *ii)* R_{if} *iii) Resistance seen by the source iv)* A_{Vf}

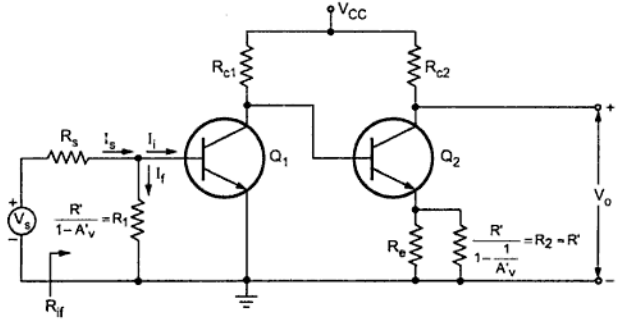


Fig. 1.90

(Ans. : i) $A'_v = -52.5$ **ii)** $R_{if} = 22\ \Omega$
iii) Resistance seen by the source = 1.22 K, iv) $A_{Vf} = 9.3$ **)**

6. *The feedback amplifier is shown in Fig. 1.91 The transistors are identical and* $h_{fe} = 100$, $h_{ie} = 1.5$ *K,* h_{re} *and* h_{oe} *are negligible, reactances of all capacitors are negligible. Calculate :*
i) A_{Vf}, *ii)* R_{if}, *iii)* R_{of}, *iv)* R'_{of}.

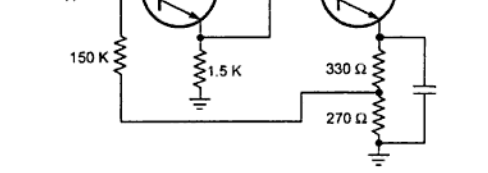


Fig. 1.91

(Ans. : i) $A_{Vf} = 30.14$ **ii)** $R_{if} = 345.43$ **K**
iii) $R_{of} = \infty$ **iv)** $R'_{of} = 456\ \Omega$.**)**

7. *For the voltage shunt negative feedback circuit,* $R_c = 4\ K$, $R_{CB} = 40\ K$, $R_s = 10\ K$, $h_{ie} = 1.1\ K$, $h_{fe} = 50$, $1/h_{oe} = 40\ K$.

Calculate, i) A_V, *ii)* R_{if}, *iii) Resistance seen by* V_s, *iv)* A_{Vf}.

(Ans. : i) $A_v = -166$ **ii)** $R_{if} = 200\ \Omega$

iii) Resistance seen by V_s, **iv)** $A_{Vf} = -3.26$.)

8. *For the circuit shown in Fig. 1.92,* $A = A_v = -1000$, $B = V_f/V_o = 1/100$, $R_s = R_c = R_e = 1 k\Omega$, $h_{ie} = 1\ k\ \Omega$, $h_{fe} = 100$ *and* h_{re}, h_{oe} *are negligible.*

Find i) V_i *as a function of* V_s *and* V_f *(Assume that the inverting amplifier input resistance is infinite.),*

ii) $A_{Vf} = V_o/V_s = A.\ V_i/V_s$.

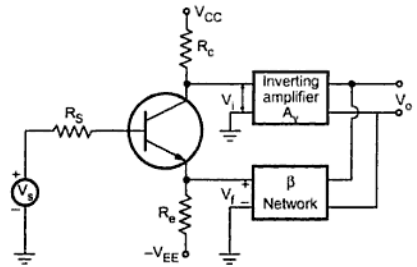


Fig. 1.92

(Ans. : i) $V_i = -50\ (V_s - V_f)$, **ii)** $A_{Vf} = 100$.)

9. *The two-stage amplifier using JFET is shown in Fig. 1.93 Given :* $r_d = 10\ K$, $\mu = 30$. A_{Vf}, R_{if} *and* R'_{of}.

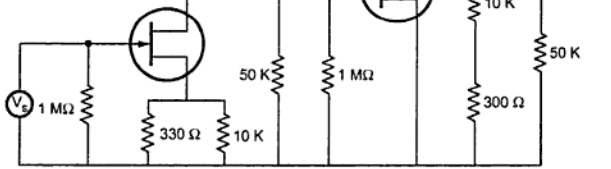


Fig. 1.93

(Ans. : i) $A_{Vf} = 30.65$, **ii)** $R_{if} = 1$ MΩ **iii)** $R'_{of} = 498\ \Omega$.)

10. For the current series feedback amplifier an overall transconductance gain of –1 mA/V, a voltage gain of – 4 (a) desensitivity of 50, R_s = 1 K, h_{fe} = 150. Find R_e, R_L and R_{if}.

(Ans. : i) R_e = 1 K, ii) R_L = –4 K, iii) R_{If} = 150 K.)

11. For the two stage amplifier circuit shown in Fig. 1.94, the transistors are identical,

h_{fe} = 50, h_{ie} = 2 K, h_{re} and h_{oe} negligible.

Find $A_{If} = I_o/I_s$, $R_i = V_i/I_s$,

$A'_{If} = I_o/I_i$ and $A_{Vf} = V_o/V_s$

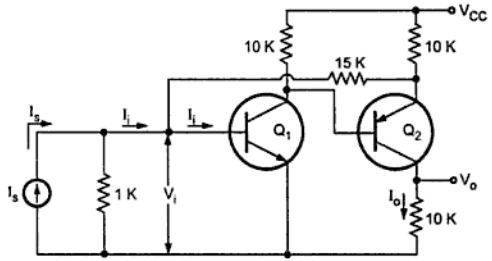


Fig. 1.94

(Ans. : A_I = 15.5, β = 0.4, A_{If} = 2.15, R_i = 650 Ω, R_{if} = 90.27 Ω, A_{vf} = 21.5)

12. For the circuit shown in Fig. 1.95 h_{fe} = 50, h_{ie} = 1.1 K, h_{oe} and h_{re} are negligible. Find A_{Vf}, A_{If}, R_{if}, R_{of} and R'_{of}.

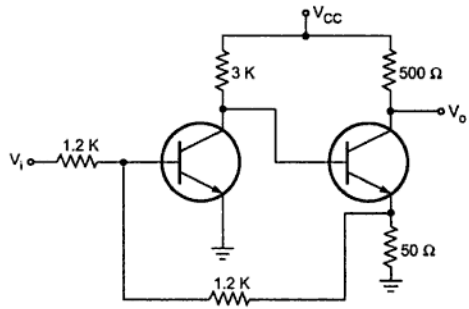


Fig. 1.95

(Ans. : i) A_{Vf} = 9.79, ii) A_{If} = 23.5, iii) R_{if} = 22.6 Ω, iv) R_{of} = ∞ v) R'_{of} = 500 Ω)

13. For the two stage amplifier circuit shown in Fig. 1.96.

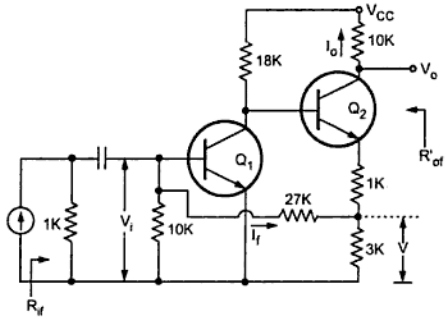


Fig. 1.96

h_{fe} = *50,* h_{ie} = *2 K,* h_{re} *and* h_{oe} *are negligible and transistors are identical.*

Find

i) $A_{If} = \frac{I_o}{I_s}$ *ii)* R_{if} *iii)* $A_{Vf} = \frac{V_o}{V_s}$ *iv)* R'_{of}.

(Ans. : i) A_{If} **= 8.69, ii)** R_{if}**, = 80.2 Ω**

iii) A_{Vf} **= 86.9, iv)** R'_{of} **= 10 K)**

14. For the voltage shunt feedback amplifier circuit shown in Fig. 1.97.

h_{fe} = *100,* h_{ie} = *1 K and* h_{re} *,* h_{oe} *negligible.*

Calculate : i) $R_{mf} = \frac{V_o}{I_s}$ *ii)* $A_{Vf} = \frac{V_o}{V_s}$ *iii)* R_{if} *and iv)* R'_{of}

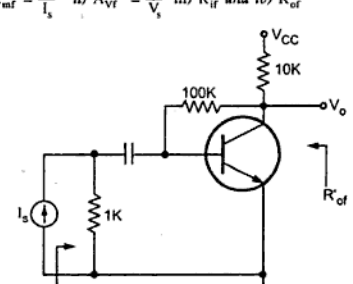


Fig. 1.97

(Ans. : i) R_{Mf} **= – 81.98 K ii)** A_{Vf} **= – 82**

iii) R_{if} **= 90 Ω iv)** R'_{of} **= 1.63 K)**

15. *For the current shunt feedback amplifier shown in Fig. 1.98.*
h_{ie} = *1 K,* h_{fe} = *100,* h_{re} *and* h_{oe} *negligible. Calculate* A_{Vf} , R_{if} *and* R'_{of}.

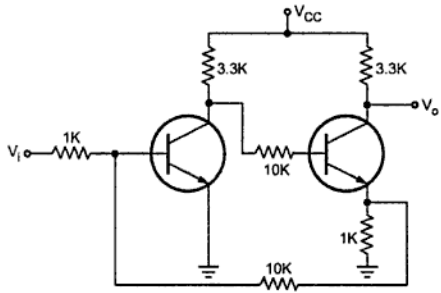


Fig. 1.98

(Ans. : i) A_{vf} **= 34.14 ii)** R_{if} **= 33.28 Ω iii)** $R_{of} = \infty$**)**

16. *For the CE amplifier shown in Fig. 1.99 ,* R_1 = *10 MΩ* R_2 = *1.6 MΩ,* R_3 = *8 K,* V_{CC} = *20 V and* h_{fe} = *100. Calculate* R_{Mf}

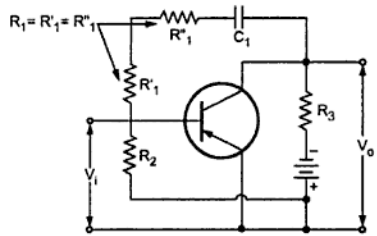


Fig. 1.99

(Ans. : R_{Mf} **= – 733.19 K)**

17. *For the circuit shown in Fig. 1.100 transistors are identical with* h_{fe} = *100,* h_{ie} = *2 K,* h_{re} *and* h_{oe} *negligible. Calculate* A_{Vf} , R_{if} , R'_{of}.

(Ans. : i) A_{Vf} **= –22.9 ii)** R_{if} **= 23.35 Ω iii)** R'_{of} **= 483 Ω)**

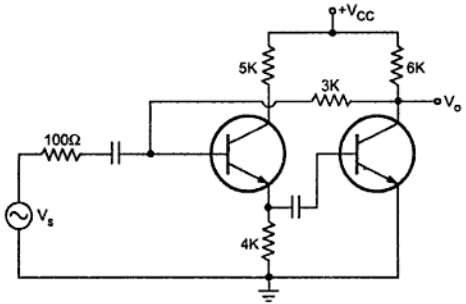


Fig. 1.100

18. For the circuit shown in Fig. 1.101

Calculate $R_{Mf} = V_o/I_s$, $A_{Vf} = V_o/V_s$, R_{if} *and* R'_{of}.

Given : $h_{fe} = 100$, $h_{ie} = 1K$, h_{re} *and* h_{oe} *negligible.*

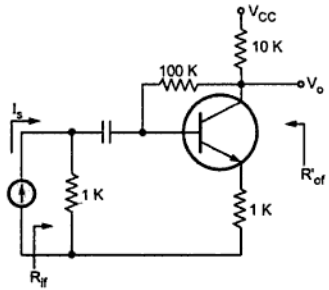


Fig. 1.101

(Ans. : i) $R_{Mf} = -8.031$ **K ii)** $A_{Vf} = -8.03$

iii) $R_{if} = 901.5\ \Omega$ **iv)** $R'_{of} = 8.36$ **K)**

❑❑❑

2 Oscillators

2.1 Introduction

The operation of the feedback amplifiers in which the negative feedback is used, has been discussed earlier. In this chapter, a device which works on the principle of positive feedback is discussed. The device is called an **Oscillator**.

Key Point : *An oscillator is a circuit which basically acts as a generator, generating the output signal which oscillates with constant amplitude and constant desired frequency.*

An oscillator does not require any input signal. An electrical device, alternator generates a sinusoidal voltage at a desired frequency of 50 Hz in our nation but electronic oscillator can generate a voltage of any desired waveform at any frequency. An oscillator can generate the output waveform of high frequency upto gigahertz.

In short, an oscillator is an amplifier, which uses a positive feedback and without any external input signal, generates an output waveform at a desired frequency. This chapter explains the various types of oscillator circuits.

2.2 Basic Theory of Oscillators

The feedback is a property which allows to feedback the part of the output, to the same circuit as its input. Such a feedback is said to be positive whenever the part of the

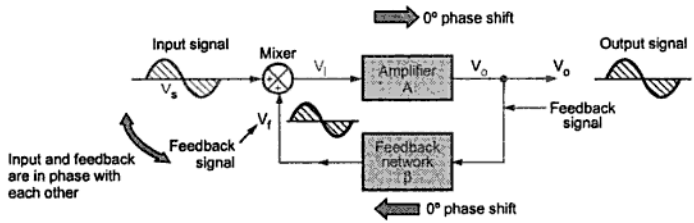


Fig. 2.1 Concept of positive feedback

output that is fed back to the amplifier as its input, is in phase with the original input signal applied to the amplifier. Consider a non-inverting amplifier with the voltage gain A as shown in the Fig. 2.1.

Assume that a sinusoidal input signal (voltage) V_s is applied to the circuit. As amplifier is non-inverting, the output voltage V_o is in phase with the input signal V_s. The part of the output is fed back to the input with the help of a feedback network. How much part of the output is to be fed back, gets decided by the feedback network gain β. No phase change is introduced by the feedback network. Hence the feedback voltage V_f is in phase with the input signal V_s.

Key Point: *As the phase of the feedback signal is same as that of the input applied, the feedback is called* ***positive feedback.***

2.2.1 Expression for Gain with Feedback

The amplifier gain is A i.e. it amplifies its input V_i, A times to produce output V_o.

$$\therefore \quad \boxed{A = \frac{V_o}{V_i}}$$

This is called **open loop gain** of the amplifier.

For the overall circuit, the input is supply voltage V_s and net output is V_o. The ratio of output V_o to input V_s considering effect of feedback is called **closed loop gain** of the circuit or **gain with feedback** denoted as A_f.

$$\therefore \quad \boxed{A_f = \frac{V_o}{V_s}}$$

The feedback is positive and voltage V_f is added to V_s to generate input of amplifier V_i. So referring Fig. 2.1 we can write,

$$\boxed{V_i = V_s + V_f} \qquad \ldots(1)$$

The feedback voltage V_f depends on the feedback element gain β. So we can write,

$$\boxed{V_f = \beta V_o} \qquad \ldots(2)$$

Substituting equation (2) in equation (1),

$$V_i = V_s + \beta V_o$$

$$\therefore \quad V_s = V_i - \beta V_o \qquad \ldots (3)$$

Substituting in expression for A_f,

$$A_f = \frac{V_o}{V_i - \beta V_o}$$

Dividing both numerator and denominator by V_i,

$$\therefore \quad A_f = \frac{(V_o / V_i)}{1 - \beta (V_o / V_i)}$$

$$\therefore \quad \boxed{A_f = \frac{A}{1 - A\beta}} \qquad \ldots \text{ as } A = \frac{V_o}{V_i}$$

Now consider the various values of β and the corresponding values of A_f for constant amplifier gain of A = 20.

A	β	A_f
20	0.005	22.22
20	0.04	100
20	0.045	200
20	0.05	∞

Table 2.1

Conclusions :

The above result shows that the gain with feedback increases as the amount of positive feedback increases. In the limiting case, the gain becomes infinite. This indicates that circuit can produce output without external input ($V_s = 0$), just by feeding the part of the output as its own input. Similarly, output cannot be infinite but gets driven into the oscillations. In other words, the circuit stops amplifying and starts oscillating.

Key Point : *Thus without an input, the output will continue to oscillate whose frequency depends upon the feedback network or the amplifier or both. Such a circuit is called as an oscillator.*

It must be noted that β the feedback network gain is always a fraction and hence $\beta < 1$. So the feedback network is an attenuation network. To start with the oscillations $A\beta > 1$ but the circuit adjusts itself to get $A\beta = 1$, when it produces sinusoidal oscillations while working as an oscillator.

2.3 Barkhausen Criterion

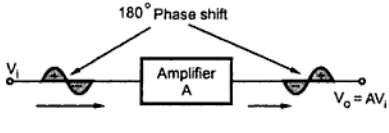


Fig. 2.2 Inverting amplifier

Consider a basic inverting amplifier with an open loop gain A. The feedback network attenuation factor β is less than unity. As basic amplifier is inverting, it produces a phase shift of 180° between input and output as shown in the Fig. 2.2.

Now the input V_i applied to the amplifier is to be derived from its output V_o using feedback network.

But the feedback must be positive i.e. the voltage derived from output using feedback network must be in phase with V_i. Thus the feedback network must introduce a phase shift of 180° while feeding back the voltage from output to input. This ensures positive feedback.

The arrangement is shown in the Fig. 2.3.

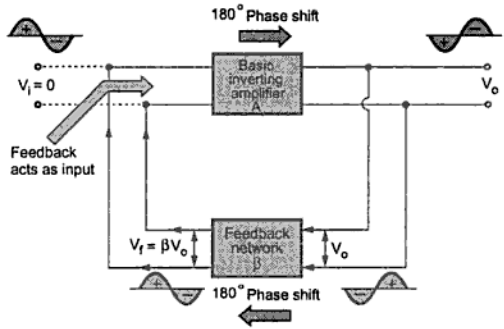


Fig. 2.3 Basic block diagram of oscillator circuit

Consider a fictitious voltage V_i applied at the input of the amplifier. Hence we get,

$$V_o = A\, V_i \qquad \ldots(1)$$

The feedback factor β decides the feedback to be given to input,

$$V_f = \beta\, V_o \qquad \ldots(2)$$

Substituting equation (1) into equation (2) we get,

$$V_f = A\, \beta\, V_i \qquad \ldots(3)$$

For the oscillator, we want that feedback should drive the amplifier and hence V_f must act as V_i. From equation (3) we can write that, V_f is sufficient to act as V_i when,

$$|\, A\, \beta\, | = 1 \qquad \ldots(4)$$

And the phase of V_f is same as V_i i.e. feedback network should introduce 180° phase shift in addition to 180° phase shift introduced by inverting amplifier. This ensures positive feedback. So total phase shift around a loop is 360°.

In this condition, V_f drives the circuit and without external input circuit works as an oscillator.

The two conditions discussed above, required to work the circuit as an oscillator are called **Barkhausen Criterion** for oscillation.

The **Barkhausen Criterion** states that :

1. The total phase shift around a loop, as the signal proceeds from input through amplifier, feedback network back to input again, completing a loop, is precisely 0° or 360°.
2. The magnitude of the product of the open loop gain of the amplifier (A) and the magnitude of the feedback factor β is unity i.e. $| A\beta | = 1$.

Satisfying these conditions, the circuit works as an oscillator producing sustained oscillations of constant frequency and amplitude.

In reality, no input signal is needed to start the oscillations. In practice, Aβ is made greater than 1 to start the oscillations and then circuit adjusts itself to get Aβ =1, finally resulting into self sustained oscillations. Let us see the effect of the magnitude of the product Aβ on the nature of the oscillations.

2.3.1 $| A\beta | > 1$

When the total phase shift around a loop is 0° or 360° and $| A\beta | > 1$, then the output oscillates but the oscillations are of growing type. The amplitude of oscillations goes on increasing as shown in the Fig. 2.4.

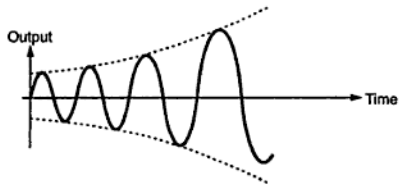


Fig. 2.4 Growing type oscillations

2.3.2 $| A\beta | = 1$

As stated by Barkhausen criterion, when total phase shift around a loop is 0° or 360° ensuring positive feedback and $| A\beta | = 1$ then the oscillations are with constant frequency and amplitude called sustained oscillations.

Such oscillations are shown in the Fig. 2.5.

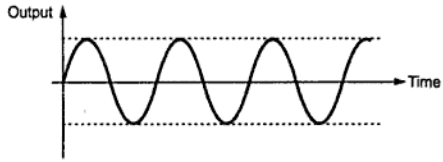


Fig. 2.5 Sustained oscillations

2.3.3 | Aβ | < 1

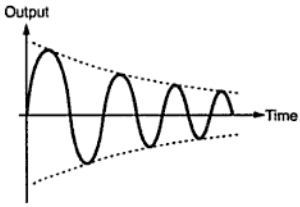


Fig. 2.6 Exponentially decaying oscillations

When total phase shift around a loop is 0° or 360° but |A β| < 1 then the oscillations are of decaying type i.e. such oscillation amplitude decreases exponentially and the oscillations finally cease. Thus circuit works as an amplifier without oscillations. The decaying oscillations are shown in the Fig. 2.6.

So to start the oscillations without input, |Aβ| is kept higher than unity and then circuit adjusts itself to get | A β | = 1 to result sustained oscillations.

2.3.4 Starting Voltage

It is mentioned that no external input is required in case of oscillators. In the earlier analysis also, the input V_i is assumed as fictitious input and practically no such input is required. The oscillator output supplies its own input under proper conditions. The obvious question is if no input is required, how oscillator starts ? And where does the starting voltage come from ?

Every resistance has some free electrons. Under the influence of normal room temperature, these free electrons move randomly in various directions. Such a movement of the free electrons generate a voltage called noise voltage, across the resistance. Such noise voltages present across the resistances are amplified. Hence to amplify such small noise voltages and to start the oscillations, | A β | is kept greater than unity at start. Such amplified voltage appears at the output terminals. The part of this output is sufficient to drive the input of amplifier circuit. Then circuit adjusts itself to get | Aβ | = 1 and with phase shift of 360° we get sustained oscillations.

Example 2.1 : *In a certain oscillator circuit, the gain of the amplifier is* $\left[\frac{-16\times10^6}{j\omega}\right]$ *and the feedback factor of the feedback network is* $\frac{10^3}{[2\times10^3+j\omega]^2}$. *Verify the Barkhausen Criterion for the sustained oscillations. Also find the frequency at which circuit will oscillate.*

Solution : From the given information we can write,

$$A = -\frac{16\times10^6}{j\omega} \text{ and } \beta = \frac{10^3}{[2\times10^3+j\omega]^2}$$

To verify the Barkhausen condition means to verify whether $|A\beta| = 1$ at a frequency for which $\angle A\beta = 0°$. Let us express, $A\beta$ in its rectangular form.

$$A\beta = -\frac{16\times10^6\times10^3}{j\omega[2\times10^3+j\omega]^2} = -\frac{16\times10^9}{j\omega[4\times10^6+4\times10^3 j\omega+(j\omega)^2]}$$

$$= -\frac{16\times10^9}{j\omega\left[4\times10^6+j\omega4\times10^3-\omega^2\right]} \quad \text{as } j^2 = -1$$

$$= -\frac{16\times10^9}{4\times10^6 j\omega+j^2\omega^2 4\times10^3-j\omega^3}$$

$$= -\frac{16\times10^9}{j\omega[4\times10^6-\omega^2]-[\omega^2\times4\times10^3]}$$

Rationalising the denominator function we get,

$$A\beta = -\frac{16\times10^9[-4\times10^3\omega^2-j\omega(4\times10^6-\omega^2)]}{\left\{(-4\times10^3\omega^2)+j\omega(4\times10^6-\omega^2)\right\}\left\{-(4\times10^3\omega^2)-j\omega(4\times10^6-\omega^2)\right\}}$$

Using $(a + b)(a - b) = a^2 - b^2$ in the denominator,

$$A\beta = \frac{+16\times10^9[4\times10^3\omega^2+j\omega(4\times10^6-\omega^2)]}{(-4\times10^3\omega^2)^2-[j\omega(4\times10^6-\omega^2)]^2}$$

$$= \frac{16\times10^9[4\times10^3\omega^2+j\omega(4\times10^6-\omega^2)]}{16\times10^6\omega^4+\omega^2(4\times10^6-\omega^2)^2}$$

Now to have $\angle A\beta = 0°$, the imaginary part of $A\beta$ must be zero. This is possible when,

$\therefore \quad \omega(4\times10^6-\omega^2) = 0$

$\therefore \quad \omega = 0 \text{ or } 4\times10^6-\omega^2 = 0$

$\therefore \quad \omega^2 = 4\times10^6$ Neglecting zero value of frequency

$\therefore \quad \omega = 2\times10^3$ **rad/sec**

At this frequency $|A\beta|$ can be obtained as,

$$|A\beta| = \frac{16\times10^9[4\times10^3\omega^2]}{16\times10^6\ \omega^4+\omega^2(4\times10^6-\omega^2)^2} \quad \text{at } \omega = 2\times10^3$$

$$= \frac{16\times10^9[4\times10^3\times4\times10^6]}{16\times10^6\times16\times10^{12}+4\times10^6[4\times10^6-4\times10^6]^2}$$

$$= \frac{2.56\times10^{20}}{2.56\times10^{20}+0} = 1$$

$\therefore$ At $\omega = 2\times10^3$ rad/sec, $\angle A\beta = 0°$ as imaginary part is zero while $|A\beta| = 1$. Thus Barkhausen Criterion is satisfied.

The frequency at which circuit will oscillate is the value of ω for which $|A\beta| = 1$ and $\angle A\beta = 0°$ at the same time

i.e. $\omega = 2\times10^3$ rad/sec.

But $\omega = 2\pi f$

$\therefore \quad f = \frac{\omega}{2\pi} = \frac{2\times10^3}{2\pi} = 318.309$ **Hz**

2.4 Classification of Oscillators

The oscillators are classified based on the nature of the output waveform, the parameters used, the range of frequency etc. The various ways in which oscillators are classified as :

2.4.1 Based on the Output Waveform

Under this, the oscillators are classified as sinusoidal and nonsinusoidal oscillators. The sinusoidal oscillators generate purely sinusoidal waveform at the output. While nonsinusoidal oscillators generate an output waveform as triangular, square, sawtooth etc. In this chapter, we are going to discuss only sinusoidal oscillators.

2.4.2 Based on the Circuit Components

The oscillators using the components resistance (R) and capacitor (C), are called RC oscillators. While the oscillators using the components inductance (L) and capacitor (C), are called LC oscillators. In some oscillators, crystal is used, which are called crystal oscillators.

2.4.3 Based on the Range of Operating Frequency

If the oscillators are used to generate the oscillations at audio frequency range which is 20 Hz to 100 - 200 kHz, then the oscillators are classified as low frequency (L.F.) or audio frequency (A.F.) oscillators. While the oscillators used at the frequency range more than

200 - 300 kHz upto gigahertz (GHz) are classified as high frequency (H.F.) or radio frequency (R.F.) oscillators. The RC oscillators are used at low frequency range while the LC oscillators are used at high frequency range.

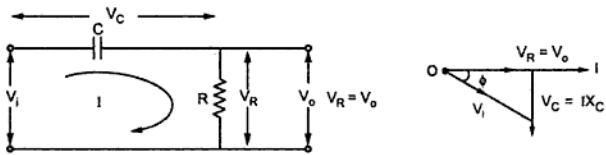
2.4.4 Based on : Whether Feedback is Used or Not ?

The oscillators in which the feedback is used, which satisfies the required conditions, are classified as feedback type of oscillators. The oscillators in which the feedback is not used to generate the oscillations, are classified as nonfeedback oscillators. The nonfeedback oscillators use the negative resistance region of the characteristics of the device used. The example of the nonfeedback type of oscillator is the UJT relaxation oscillator.

2.5 R-C Phase Shift Oscillator

RC phase shift oscillator basically consists of an amplifier and a feedback network consisting of resistors and capacitors arranged in ladder fashion. Hence such an oscillator is also called ladder type RC phase shift oscillator.

To understand the operation of this oscillator let us study RC circuit first, which is used in the feedback network of this oscillator. The Fig. 2.7 shows the basic RC circuit.



(a) Circuit Fig. 2.7 (b) Phasor diagram

The capacitor C and resistance R are in series. Now X_C is the capacitive reactance in ohms given by,

$$X_C = \frac{1}{2\pi f C} \quad \Omega$$

The total impedance of the circuit is,

$$Z = R - j X_C = R - j\left(\frac{1}{2\pi f C}\right) \Omega = |Z| \angle -\phi^\circ \Omega$$

The r.m.s. value of the input voltage applied is say V_i volts. Hence the current is given by,

$$I = \frac{V_i \angle 0^\circ}{Z} = \frac{V_i \angle 0^\circ}{|Z| \angle -\phi}$$

$$\therefore \quad I = \frac{V_i}{Z} \angle +\phi \quad A$$

where $|Z| = \sqrt{R^2 + (X_C)^2}$

and $\phi = \tan^{-1}\left(\frac{X_C}{R}\right)$

From expression of current it can be seen that **current I leads input voltage V_i by angle ϕ.**

The output voltage V_o is the drop across resistance R given by,

$$V_o = V_R = IR$$

The voltage across the capacitor is,

$$V_C = I X_C$$

The drop V_R is in phase with current I while the drop V_C lags current I by 90° i.e. I leads V_C by 90°. The phasor diagram is shown in the Fig. 2.7 (b).

By using proper values of R and C, **the angle ϕ is adjusted in practice equal to 60°**, as required for RC phase shift oscillator.

2.5.1 RC Feedback Network

As stated earlier, RC network is used in feedback path. In oscillator, feedback network must introduce a phase shift of 180° to obtain total phase shift around a loop as 360°. Thus if one RC network produces phase shift of $\phi = 60°$ then to produce phase shift of 180° such three RC networks must be connected in cascade. Hence in RC phase shift oscillator, the feedback network consists of three RC sections each producing a phase shift of 60°, thus total phase shift due to feedback is 180° (3×60°). Such a feedback network is shown in the Fig. 2.8.

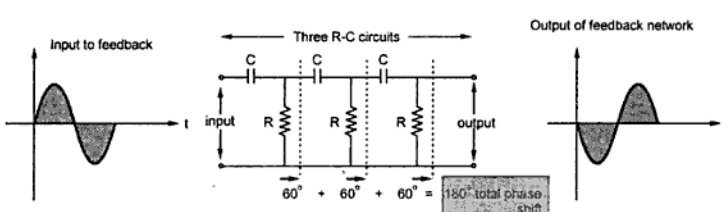


Fig. 2.8 Feedback network in RC phase shift oscillator

The network is also called the **ladder network**. All the resistance values and all the capacitance values are same, so that for a particular frequency, each section of R and C produces a phase shift of 60°.

2.5.2 Phase Shift Oscillator using Transistor

In a practical RC phase shift oscillator, a common emitter (CE) single stage amplifier is used as a basic amplifier. This produces 180° phase shift. The feedback network consists of 3 RC sections each producing 60° phase shift. Such a RC phase shift oscillator using BJT amplifier is shown in the Fig. 2.9.

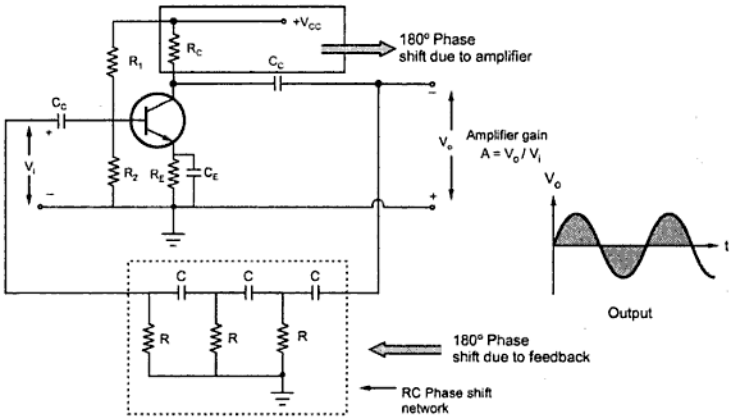


Fig. 2.9 Transistorised RC phase shift oscillator

The output of amplifier is given to feedback network. The output of feedback network drives the amplifier. The total phase shift around a loop is 180° of amplifier and 180° due to 3 RC section, thus 360°. This satisfies the required condition for positive feedback and circuit works as an oscillator.

The frequency of sustained oscillations generated depends on the values of R and C and is given by,

$$f = \frac{1}{2\pi\sqrt{6}\,R\,C}$$

The frequency is measured in Hz.

Actually to satisfy the Barkhausen condition, the expression for the frequency of oscillations is given by,

$$f = \frac{1}{2\pi R C} \cdot \frac{1}{\sqrt{6+4K}}$$

where $K = \frac{R_C}{R}$

As practically R_C/R is small, K is neglected,

The condition of h_{fe} for the transistor to obtain the oscillations is given by,

$$h_{fe} > 4K + 23 + \frac{29}{K}$$

And value of K for minimum h_{fe} is 2.7 hence minimum h_{fe} = 44.5. So transistor with h_{fe} less than 44.5 cannot be used in phase shift oscillator.

But for most of practical circuits, the expression for the frequency is considered as,

$$f = \frac{1}{2\pi\sqrt{6} R C}$$

2.5.3 Derivation for the Frequency of Oscillations

Replacing the transistor by its approximate h-parameter model, we get the equivalent oscillator circuit as shown in the Fig. 2.10.

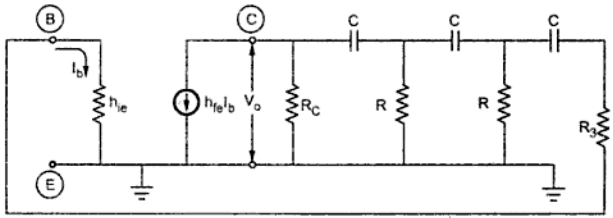


Fig. 2.10 Equivalent circuit using h-parameter model

Practically R_3 is used such that h_{ie} of transistor alongwith R_3 completes the need of R.

$$\therefore \quad R = h_{ie} + R_3$$

Note : If the resistances R_1 and R_2 are not neglected then the input impedance of the amplifier stage becomes as,

$$\boxed{R_i' = R_1 \,||\, R_2 \,||\, h_{ie}} \quad \ldots (1)$$

In such a case, the value of R_3 must be so selected that

$$\boxed{R_i' + R_3 = R} \quad \ldots (2)$$

Similarly we can replace, the current source $h_{fe}\, I_b$ by its equivalent voltage source. And assume the ratio of the resistance R_C to R be K.

$$\therefore \quad \boxed{K = \frac{R_C}{R}}$$

The modified equivalent circuit is shown in the Fig. 2.11.

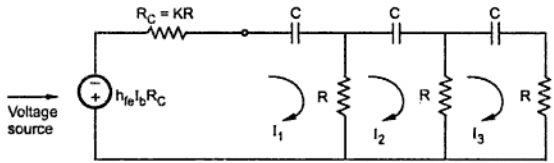


Fig. 2.11 Modified equivalent circuit

Applying KVL for the various loops in the modified equivalent circuit we get,

For Loop 1,

$$-I_1 R_C - \frac{1}{j\omega C} I_1 - I_1 R + I_2 R - h_{fe} I_b R_C = 0$$

Replacing R_C by KR and $j\omega$ by s we get,

$$\therefore \quad + I_1 \left[(K+1) R + \frac{1}{sC}\right] - I_2 R = -h_{fe} I_b KR \quad \ldots (3)$$

For Loop 2,

$$-\frac{1}{j\omega C} I_2 - I_2 R - I_2 R + I_1 R + I_3 R = 0$$

$$\therefore \quad -I_1 R + I_2 \left[2R + \frac{1}{sC}\right] - I_3 R = 0 \quad \ldots (4)$$

For Loop 3,

$$-I_3\frac{1}{j\omega C}-I_3R-I_3R+I_2R = 0$$

$$\therefore \quad -I_2R+I_3\left[2R+\frac{1}{sC}\right] = 0 \qquad \ldots (5)$$

Using Cramer's Rule to solve for I_3,

$$D = \begin{vmatrix} (K+1)R+\frac{1}{sC} & -R & 0 \\ -R & 2R+\frac{1}{sC} & -R \\ 0 & -R & 2R+\frac{1}{sC} \end{vmatrix}$$

$$= \left[(K+1)R+\frac{1}{sC}\right]\left[2R+\frac{1}{sC}\right]^2 - R^2\left[2R+\frac{1}{sC}\right] - R^2\left[(K+1)R+\frac{1}{sC}\right]$$

$$= \frac{[sRC(K+1)+1][2sCR+1]^2}{s^3C^3} - \frac{R^2(2sCR+1)}{sC} - \frac{R^2[(K+1)sRC+1]}{sC}$$

First term can be written as,

$$\frac{[sKRC + sRC + 1][4s^2C^2R^2 + 4sRC + 1]/s^3C^3}{} = \frac{4s^3KR^3C^3 + 4s^3R^3C^3 + 4s^2C^2R^2 + 4s^2kR^2C^2 + 4s^2R^2C^2 + 4sRC + sKRC + sRC + 1}{s^3C^3}$$

Second and the Third term can be combined to get,

$$= \frac{-R^2[KsRC + sRC + 1] - R^2[1 + 2sRC]}{sC}$$

$$= \frac{-[2R^2 + 3sR^3C + KsR^3C]}{sC}$$

Combining the two terms and taking LCM as s^3C^3 we get,

$$D = \frac{s^3C^3R^3[4K+4] + s^2C^2R^2[4K+8] + sRC[5+K] + 1 - [2R^2 + 3sR^3C + KsR^3C]s^2C^2}{s^3C^3}$$

$$= \frac{s^3C^3R^3[3K+1] + s^2C^2R^2[4K+6] + sRC[5+K] + 1}{s^3C^3} \qquad \ldots (6)$$

Now

$$D_3 = \begin{vmatrix} (K+1)R+\frac{1}{sC} & -R & -h_{fe}I_bKR \\ -R & 2R+\frac{1}{sC} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$= -R^2 (h_{fe} I_b KR)$$

$$= -K R^3 h_{fe} I_b \quad \ldots (7)$$

$$\therefore \quad I_3 = \frac{D_3}{D}$$

$$= \frac{-KR^3 h_{fe} I_b s^3 C^3}{s^3 C^3 R^3 [3K+1] + s^2 C^2 R^2 [4K+6] + sRC [5K+1] + 1} \quad \ldots (8)$$

Now I_3 = Output current of the feedback circuit

I_b = Input current of the amplifier

$I_c = h_{fe} I_b$ = Input current of the feedback circuit

$$\therefore \quad \beta = \frac{\text{Output of feedback circuit}}{\text{Input to feedback circuit}} = \frac{I_3}{h_{fe} I_b}$$

And $$A = \frac{\text{Output of amplifier circuit}}{\text{Input to amplifier circuit}} = \frac{I_3}{I_b} = h_{fe}$$

$$\therefore \quad A\beta = \frac{I_3}{h_{fe} I_b} \times h_{fe} = \frac{I_3}{I_b} \quad \ldots (9)$$

Using equation (9) we get,

$$A\beta = \frac{-KR^3 h_{fe} s^3 C^3}{s^3 C^3 R^3 [3K+1] + s^2 C^2 R^2 [4K+6] + sRC [5K+1] + 1} \quad \ldots (10)$$

Substituting $s = j\omega$, $s^2 = j^2\omega^2 = -\omega^2$, $s^3 = j^3\omega^3 = -j\omega^3$ in the equation (10) we get,

$$A\beta = \frac{-j\omega^3 KR^3 C^3 h_{fe}}{-j\omega^3 C^3 R^3 [3K+1] - \omega^2 C^2 R^2 [4K+6] + j\omega RC [5+K] + 1}$$

Separating the real and imaginary parts in the denominator we get,

$$A\beta = \frac{-j\omega^3 KR^3 C^3 h_{fe}}{[1 - 4K\omega^2 C^2 R^2 - 6\omega^2 C^2 R^2] - j\omega[3K\omega^2 R^3 C^3 + \omega^2 R^3 C^3 - 5RC - KRC]}$$

Dividing numerator and denominator by $j\omega^3 R^3 C^3$,

$$A\beta = \frac{Kh_{fe}}{\left\{\frac{(1 - 4K\omega^2 C^2 R^2 - 6\omega^2 C^2 R^2)}{-j\omega^3 R^3 C^3}\right\} - \left\{\frac{j\omega[3K\omega^2 R^3 C^3 + \omega^2 R^3 C^3 - 5RC - KRC]}{-j\omega^3 R^3 C^3}\right\}}$$

Replacing $-1/j = j$,

$$= \frac{K h_{fe}}{j\left\{\frac{1}{\omega^3 R^3 C^3} - \frac{4K}{\omega RC} - \frac{6}{\omega RC}\right\} + \left\{3K+1 - \frac{5}{\omega^2 R^2 C^2} - \frac{K}{\omega^2 R^2 C^2}\right\}}$$

Replacing $\frac{1}{\omega RC} = \alpha$ for simiplicity

$$\therefore \quad A\beta = \frac{K h_{fe}}{[3K+1-5\alpha^2 - K\alpha^2] + j[\alpha^3 - 4K\alpha - 6\alpha]} \quad \ldots (11)$$

As per the Barkhausen Criterion, $\angle A\beta = 0°$. Now the angle of numerator term kh_{fe} of the equation (11) is 0° hence to have angle of the Aβ term as 0°, the imaginary part of the denominator term must be 0.

$$\therefore \quad \alpha^3 - 4K\alpha - 6\alpha = 0$$

$$\alpha(\alpha^2 - 4K - 6) = 0$$

$$\therefore \quad \alpha^2 = 4K + 6 \text{ neglecting zero value}$$

$$\therefore \quad \alpha = \sqrt{4K+6}$$

$$\therefore \quad \frac{1}{\omega RC} = \sqrt{4K+6}$$

$$\boxed{\omega = \frac{1}{RC\sqrt{4K+6}}}$$

$$\therefore \quad \boxed{F = \frac{1}{2\pi RC\sqrt{4K+6}}} \quad \ldots(12)$$

This is the frequency at which $\angle A\beta = 0°$. At the same frequency, $|A\beta| = 1$.

Substituting $\alpha = \sqrt{4K+6}$ in the equation (11) we get,

$$A\beta = \frac{K h_{fe}}{3K+1-(4K+6)[5+K]} = \frac{K h_{fe}}{3K+1-20K-30-4K^2-6K}$$

$$= \frac{K h_{fe}}{-4K^2 - 23K - 29}$$

Now $|A\beta| = 1$

$$\therefore \quad \left|\frac{K h_{fe}}{-4K^2 - 23K - 29}\right| = 1$$

$$\therefore \quad K h_{fe} = 4K^2 + 23K + 29$$

$$\boxed{h_{fe} = 4K + 23 + \frac{29}{K}} \quad \ldots(13)$$

This must be the value of h_{fe} for the oscillations.

2.5.4 Minimum Value of h_{fe} for the Oscillations

To get minimum value of h_{fe},

$$\frac{d\,h_{fe}}{dk} = 0$$

$$\therefore \quad \frac{d}{dk}\left[4k + 23 + \frac{29}{k}\right] = 0$$

$$\therefore \quad \left[4 - \frac{29}{k^2}\right] = 0$$

$$\therefore \quad k^2 = \frac{29}{4}$$

$$\therefore \quad k = 2.6925 \text{ for minimum } h_{fe} \qquad \ldots (14)$$

Substituting in the equation (13),

$$(h_{fe})_{min} = 4\,(2.6925) + 23 + \frac{29}{(2.6925)}$$

$$\therefore \quad \boxed{(h_{fe})_{min} = 44.54} \qquad \ldots (15)$$

Key Point : *Thus for the circuit to oscillate, we must select the transistor whose (h_{fe}) min should be greater than 44.54.*

By changing the values of R and C, the frequency of the oscillator can be changed. But the values of R and C of all three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible. Hence the phase shift oscillator is considered as a fixed frequency oscillator, for all practical purposes.

Example 2.2: *Find the capacitor C and h_{fe} for the transistor to provide a resonating frequncy of 10 kHz of a transistorised phase shift oscillator. Assume $R_1 = 25\ k\Omega$, $R_2 = 57\ k\Omega$, $R_C = 20\ k\Omega$, $R = 7.1\ k\Omega$ and $h_{ie} = 1.8\ k\Omega$.*

Solution : Referring to equation (1),

$$R_i' = R_1 \parallel R_2 \parallel h_{ie} = 25\ k\Omega \parallel 57\ k\Omega \parallel 1.8\ k\Omega$$

$$\frac{1}{R_i'} = \frac{1}{25} + \frac{1}{57} + \frac{1}{1.8}$$

$$\therefore \quad R_i' = 1.631\ k\Omega$$

Now $R_i' + R_3 = R$

$$\therefore \quad R_3 = R - R_i' = 7.1 - 1.631$$

$$= 5.47\ k\Omega$$

$$k = \frac{R_C}{R} = \frac{20}{7.1} = 2.816$$

Now $$f = \frac{1}{2\pi RC\sqrt{6+4k}}$$

$$\therefore \quad 10\times10^3 = \frac{1}{2\pi\times7.1\times10^3\times C\times\sqrt{6+4\times2.816}}$$

$$\therefore \quad C = \mathbf{539.45\ pF}$$

$$h_{fe} \geq 4k + 23 + \frac{29}{k}$$ Refer equation (13)

$$\therefore \quad h_{fe} \geq 4\times2.816+23+\frac{29}{2.816}$$

$$\therefore \quad h_{fe} \geq \mathbf{44.562}$$

2.5.5 Advantages

The advantages of RC phase shift oscillator are,

1. The circuit is simple to design.
2. Can produce output over audio frequency range.
3. Produces sinusoidal output waveform.
4. It is a fixed frequency oscillator.

2.5.6 Disadvantages

By changing the values of R and C, the frequency of the oscillator can be changed. But the values of R and C of all three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible. Hence the phase shift oscillator is considered as a fixed frequency oscillator, for all practical purposes.

And the frequency stability is poor due to the changes in the values of various components, due to effect of temperature, aging etc.

Example 2.3 : *In a RC phase shift oscillator, the phase shift network uses the resistances each of 4.7 kΩ and the capacitors each of 0.47 μF. Find the frequency of oscillations.*

Solution : The given values are, $R = 4.7\ k\Omega$ and $C = 0.47\ \mu F$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{6}RC} = \frac{1}{2\pi\sqrt{6}\times4.7\times10^3\times0.47\times10^{-6}} = \mathbf{29.413\ Hz}$$

Example 2.4 : *Estimate the values of R and C for an output frequency of 1 kHz in a RC phase shift oscillator.*

Solution : $f = 1$ kHz

Now $$f = \frac{1}{2\pi\sqrt{6}RC}$$

Choose $C = 0.1\ \mu F$

$$\therefore \quad 1\times10^{3} = \frac{1}{2\pi\sqrt{6}R\times0.1\times10^{-6}}$$

$$\therefore \quad R = 649.747\ \Omega$$

Choose $R = 680\ \Omega$ standard value

2.5.7 Phase Shift Oscillator using Op-amp

The phase shift oscillator circuit can be realised by using operational amplifier instead of transistorised amplifier. The operational amplifier is available in integrated circuit version (IC). It provides a stabilised gain setting. The feedback circuit used is same as used in the transistorised phase shift oscillator. The op-amp is used in inverting mode to provide 180° phase shift. The output of op-amp is fed to three section R_C network which provides the needed 180° phase shift. The gain of the op-amp is adjusted with the help of the resistances R_f and R_i, shown in the Fig. 2.12. The gain is so adjusted that the product of gain of op-amp (A) and the feedback network gain (β) is slightly greater than one, to get the required oscillations. The basic circuit of the phase shift oscillator using op-amp, is shown in the Fig. 2.12.

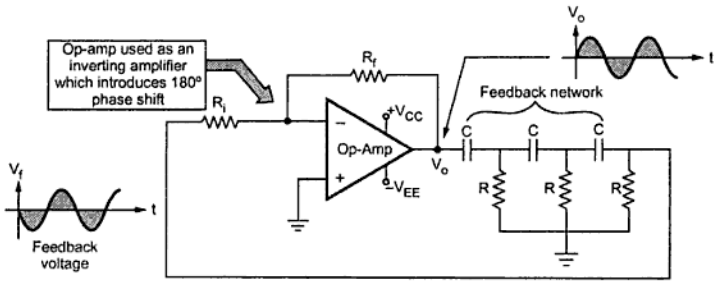


Fig. 2.12 Phase shift oscillator using op-amp

Let us find the transfer function of the RC feedback network.

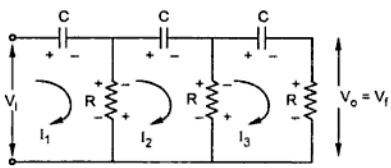


Fig. 2.13

Applying KVL to various loops we get,

$$I_1\left(R+\frac{1}{j\omega C}\right)-I_2 R = V_i \quad \ldots (15)$$

$$-I_1 R + I_2\left(2R+\frac{1}{j\omega C}\right)-I_3 R = 0 \quad \ldots (16)$$

$$0 - I_2 R + I_3\left(2R+\frac{1}{j\omega C}\right) = 0 \quad \ldots (17)$$

Replacing $j\omega$ by s and writing the equations in the matrix form,

$$\begin{vmatrix} R+\frac{1}{sC} & -R & 0 \\ -R & 2R+\frac{1}{sC} & -R \\ 0 & -R & 2R+\frac{1}{sC} \end{vmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} V_i \\ 0 \\ 0 \end{bmatrix} \quad \ldots (18)$$

Using the Cramer's rule to obtain I_3,

$$D = \begin{vmatrix} \frac{1+sRC}{sC} & -R & 0 \\ -R & \frac{1+2sRC}{sC} & -R \\ 0 & -R & \frac{1+2sRC}{sC} \end{vmatrix}$$

$$= \frac{(1+sRC)(1+2sRC)^2}{s^3C^3} - \frac{R^2(1+2sRC)}{sC} - \frac{R^2(1+sRC)}{sC}$$

$$= \frac{(1+sRC)(1+4sRC+4s^2C^2R^2) - R^2s^2C^2[1+2sRC+1+sRC]}{s^3C^3}$$

$$= \frac{1+5sRC+8s^2C^2R^2+4s^3C^3R^3-3s^3R^3C^3-2R^2s^2C^2}{s^3C^3}$$

$$= \frac{1+5sRC+6s^2C^2R^2+s^3C^3R^3}{s^3C^3} \quad \ldots (19)$$

$$D_3 = \begin{vmatrix} \frac{1+sRC}{sC} & -R & V_i \\ -R & \frac{1+2sRC}{sC} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$= V_i R^2 \quad \ldots (20)$$

$$\therefore \quad I_3 = \frac{D_3}{D} = \frac{V_i R^2 s^3 C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3}$$

Now $$V_o = V_f = I_3 R = \frac{V_i R^2 s^3 C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3} \quad \ldots (21)$$

$$\therefore \quad \beta = \frac{V_o}{V_i} = \frac{R^3 s^3 C^3}{1+5sCR+6s^2C^2R^2+s^3C^3R^3} \qquad \ldots (22)$$

Replacing s by $j\omega$, s^2 by $-\omega^2$, s^3 by $-j\omega^3$

$$\therefore \quad \beta = \frac{-j\omega^3 R^3 C^3}{1+5j\omega CR-6\omega^2C^2R^2-j\omega^3C^3R^3}$$

Dividing numerator and denominator by $-j\omega^3R^3C^3$ and replacing $\frac{1}{\omega RC}$ by α we get,

$$\therefore \quad \beta = \frac{1}{1+6j\alpha-5\alpha^2-j\alpha^3}$$

$$\therefore \quad \boxed{\beta = \frac{1}{(1-5\alpha^2)+j\alpha(6-\alpha^2)}} \qquad \ldots (23)$$

To have phase shift of 180°, the imaginary part in the denominator must be zero.

$$\therefore \quad \alpha(6-\alpha^2) = 0$$

$$\therefore \quad \alpha^2 = 6 \qquad \text{neglecting zero value}$$

$$\boxed{\alpha = \sqrt{6}}$$

$$\therefore \quad \frac{1}{\omega RC} = \sqrt{6}$$

$$\therefore \quad \omega = \frac{1}{RC\sqrt{6}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi RC\sqrt{6}}} \qquad \ldots (24)$$

This is the frequency with which circuit oscillates.

At this frequency,

$$\beta = \frac{1}{1-5\times\left(\sqrt{6}\right)^2} = -\frac{1}{29}$$

Negative sign indicates phase shift of 180°.

$$\therefore \quad \boxed{|\beta| = \frac{1}{29}} \qquad \ldots (25)$$

Now to have the oscillations, $|A\beta| \geq 1$

$$\therefore \quad |A|\,|\beta| > 1$$

$$|A| \geq \frac{1}{|\beta|} \geq \frac{1}{\left(\frac{1}{29}\right)}$$

$$\boxed{|A| \geq 29} \quad \ldots (26)$$

Key Point : *For the oscillations to occur, the gain of the op-amp must be equal to or greater than 29, which can be adjusted using the resistances R_f and R_i.*

2.5.8 FET Phase Shift Oscillator

The practical circuit of FET phase shift oscillator is shown in the Fig. 2.14.

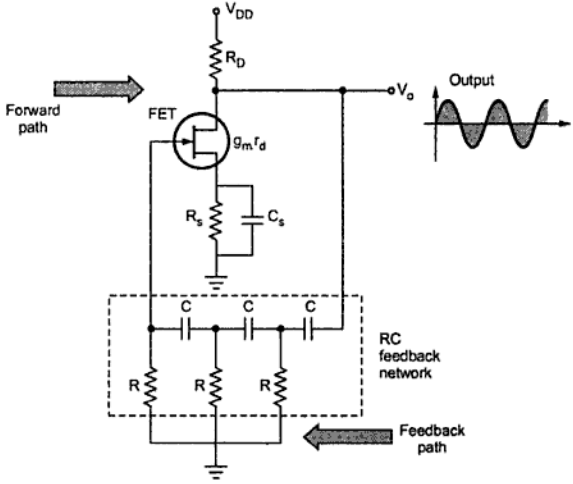


Fig. 2.14 FET phase shift oscillator

For the amplifier stage FET is used. It is self biased with a capacitor bypassed source resistance R_S and a drain bias resistance R_D. The important parameters of FET are g_m and r_d. From FET amplifier theory we can write,

$$\boxed{|A| = g_m R_L} \quad \ldots (27)$$

Where R_L is the parallel equivalent of R_D and r_d.

$$R_L = \frac{R_D r_d}{R_D + r_d} \quad \ldots (28)$$

Key Point : *The input impedance of the FET amplifier stage can be conveniently assumed as infinite, as long as the operating frequency is low enough to neglect the capacitive impedances.*

The feedback network is again three stage R_C network having gain,

$$|\beta| = \frac{1}{29}$$

$$\therefore \quad |A| \geq 29 \quad \ldots (29)$$

Hence the condition on gain of the amplifier is same as in case of op-amp, the frequency of the oscillator is given by,

$$f = \frac{1}{2\pi RC\sqrt{6}} \quad \ldots (30)$$

Example 2.5 : *A phase shift oscillator is to be designed with FET having g_m= 5000 μS, r_d = 4 kΩ while the resistance in the feedback circuit is 9.7 kΩ. Select the proper value of C and R_D to have the frequency of oscillations as 5 kHz.*

Solution : Using the expression for the frequency

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$\therefore \quad 5\times10^3 = \frac{1}{2\pi\times9.7\times10^3\times C\times\sqrt{6}}$$

$$\therefore \quad C = \mathbf{1.34\ nF}$$

Now using the equation (27),

$$|A| = g_m R_L$$

$$\therefore \quad |A| \geq 29$$

$$\therefore \quad g_m R_L \geq 29$$

$$\therefore \quad R_L \geq \frac{29}{g_m} \geq \frac{29}{5000\times10^{-6}} \geq 5.8\ \text{k}\Omega$$

With value of $R_L = 6.8\ k\Omega$,

$$R_L = \frac{R_D\, r_d}{R_D + r_d}$$

$$\therefore \quad 6.8\times10^3 = \frac{R_D \times 40\times 10^3}{R_D + 40\times10^3}$$

$$\therefore \quad R_D + 40\times10^3 = 5.8823\, R_D$$

$$\therefore \quad 4.8823\, R_D = 40\times10^3$$

$$\therefore \quad R_D = \mathbf{8.12\ k\Omega}$$

While for minimum value of $R_L = 5.8\ k\Omega$

$$R_D = \mathbf{6.78\ k\Omega}$$

2.6 Wien Bridge Oscillator

Generally in an oscillator, amplifier stage introduces 180° phase shift and feedback network introduces additional 180° phase shift, to obtain a phase shift of 360° (2π radians) around a loop. This is required condition for any oscillator. But Wien bridge oscillator uses a noninverting amplifier and hence does not provide any phase shift during amplifier stage. As total phase shift required is 0° or 2 nπ radians, in Wien bridge type no phase shift is necessary through feedback. Thus the total phase shift around a loop is 0°. Let us study the basic version of the Wien bridge oscillator and its analysis.

A basic Wien bridge used in this oscillator and an amplifier stage is shown in the Fig. 2.15.

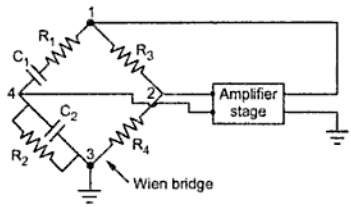


Fig. 2.15 Basic circuit of Wien bridge oscillator

The output of the amplifier is applied between the terminals 1 and 3, which is the input to the feedback network. While the amplifier input is supplied from the diagonal terminals 2 and 4, which is the output from the feedback network. Thus amplifier supplied its own input through the Wien bridge as a feedback network.

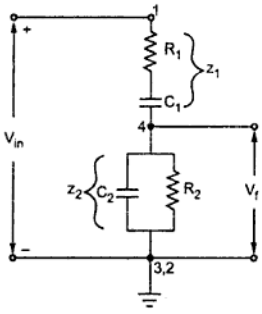


Fig. 2.16 Feedback network of Wien bridge oscillator

The two arms of the bridge, namely R_1, C_1 in series and R_2, C_2 in parallel are called **frequency sensitive arms**. This is because the components of these two arms decide the frequency of the oscillator. Let us find out the gain of the feedback network. As seen earlier input V_{in} to the feedback network is between 1 and 3 while output V_f of the feedback network is between 2 and 4. This is shown in the Fig. 2.16. Such a feedback network is called **lead-lag network**. This is because at very low frequencies it acts like a lead while at very high frequencies it acts like lag network.

2.6.1 Derivation for Frequency of Oscillations

Now from the Fig. 2.16, as shown,

$$Z_1 = R_1 + \frac{1}{j\omega C_1} = \frac{1 + j\omega R_1 C_1}{j\omega C_1}$$

$$Z_2 = R_2 \parallel \frac{1}{j\omega C_2} = \frac{R_2 \times \frac{1}{j\omega C_2}}{R_2 + \frac{1}{j\omega C_2}}$$

$$= \frac{R_2}{1 + j\omega R_2 C_2} \quad \ldots (1)$$

Replacing $j\omega = s$,

$$Z_1 = \frac{1 + s R_1 C_1}{s C_1}$$

and

$$Z_2 = \frac{R_2}{1 + s R_2 C_2}$$

$$I = \frac{V_{in}}{Z_1 + Z_2}$$

and

$$V_f = I Z_2$$

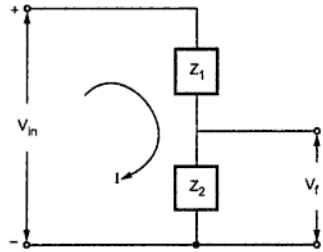


Fig. 2.17 Simplified circuit

$$\therefore \quad V_f = \frac{V_{in} Z_2}{Z_1 + Z_2}$$

$$\therefore \quad \boxed{\beta = \frac{V_f}{V_{in}} = \frac{Z_2}{Z_1 + Z_2}} \qquad \ldots(2)$$

Substituting the values of Z_1 and Z_2,

$$\beta = \frac{\left[\frac{R_2}{1+sR_2C_2}\right]}{\left[\frac{1+sR_1C_1}{sC_1}\right]+\left[\frac{R_2}{1+sR_2C_2}\right]}$$

$$\beta = \frac{sC_1R_2}{(1+sR_1C_1)(1+sR_2C_2)+sC_1R_2}$$

$$= \frac{sC_1R_2}{1+s(R_1C_1+R_2C_2)+s^2R_1R_2C_1C_2+sC_1R_2}$$

$$= \frac{sC_1R_1}{1+s(R_1C_1+R_2C_2+C_1R_2)+s^2R_1R_2C_1C_2}$$

Replacing s by $j\omega$, $s^2 = -\omega^2$

$$\therefore \quad \beta = \frac{j\omega C_1R_2}{(1-\omega^2R_1R_2C_1C_2)+j\omega(R_1C_1+R_2C_2+C_1R_2)} \qquad \ldots(3)$$

Rationalising the expression,

$$\beta = \frac{j\omega C_1R_2\left[(1-\omega^2R_1R_2C_1C_2)-j\omega(R_1C_1+R_2C_2+C_1R_2)\right]}{\left(1-\omega^2R_1R_2C_1C_2\right)^2+\omega^2(R_1C_1+R_2C_2+C_1R_2)^2}$$

$$\beta = \frac{\omega^2C_1R_2(R_1C_1+R_2C_2+C_1R_2)+j\omega C_1R_2(1-\omega^2R_1R_2C_1C_2)}{\left(1-\omega^2R_1R_2C_1C_2\right)^2+\omega^2\left(R_1C_1+R_2C_2+C_1R_2\right)^2} \qquad \ldots(4)$$

To have zero phase shift of the feedback network, its imaginary part must be zero.

$$\therefore \quad \omega(1 - \omega^2 R_1 R_2 C_1 C_2) = 0$$

$$\therefore \quad \omega^2 = \frac{1}{R_1 R_2 C_1 C_2} \text{ neglecting zero value.}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}} \qquad \ldots(5)$$

This is the frequency of the oscillator and it shows that the components of the frequency sensitive arms are the deciding factors, for the frequency.

In practice, $R_1 = R_2 = R$ and $C_1 = C_2 = C$ are selected.

$$\therefore \quad f = \frac{1}{2\pi\sqrt{R^2 C^2}}$$

$$f = \frac{1}{2\pi RC} \qquad \ldots(6)$$

At $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the gain of the feedback network becomes,

$$\beta = \frac{\omega^2 RC(3RC) + j\omega RC\left(1 - \omega^2 R^2 C^2\right)}{\left(1 - \omega^2 R^2 C^2\right) + \omega^2 (3RC)^2}$$

Substituting $f = \frac{1}{2\pi RC}$ i.e. $\omega = \frac{1}{RC}$,

we get the magnitude of the feedback network at the resonating frequency of the oscillator as,

$$\beta = \frac{3}{0 + \frac{1}{R^2 C^2} \times (3RC)^2} = \frac{3}{9}$$

$$\therefore \quad \boxed{\beta = \frac{1}{3}} \qquad \ldots(7)$$

The positive sign of β indicates that the phase shift by the feedback network is 0°. Now to satisfy the Barkhausen criterion for the sustained oscillations, we can write,

$$|A\beta| \geq 1$$

$$\therefore \quad |A| = \geq \frac{1}{|\beta|} \geq \frac{1}{\left(\frac{1}{3}\right)}$$

$$\therefore \quad \boxed{|A| \geq 3}$$

This is the required gain of the amplifier stage, without any phase shift.

If $R_1 \neq R_2$ and $C_1 \neq C_2$ then

$$\boxed{f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}}$$

Substituting in the equation (4) we get,

$$\boxed{\beta = \frac{C_1 R_2}{(R_1 C_1 + R_2 C_2 + C_1 R_2)}}$$

$$|A\beta| \geq 1$$

$$\therefore \quad \boxed{A \geq \frac{R_1 C_1 + R_2 C_2 + C_1 R_2}{C_1 R_2}} \qquad \ldots (8)$$

Key Point : *Another important advantage of the Wien bridge oscillator is that by varying the two capacitor values simultaneously, by mounting them on the common shaft, different frequency ranges can be provided.*

Let us see the transistorised version of the Wien bridge oscillator.

2.6.2 Transistorised Wien Bridge Oscillator

In this circuit, **two stage** common emitter transistor amplifier is used. Each stage contributes 180° phase shift hence the total phase shift due to the amplifier stage becomes 360° i.e. 0° which is necessary as per the oscillator conditions.

The practical, transistorised Wien bridge oscillator circuit is shown in the Fig. 2.18.

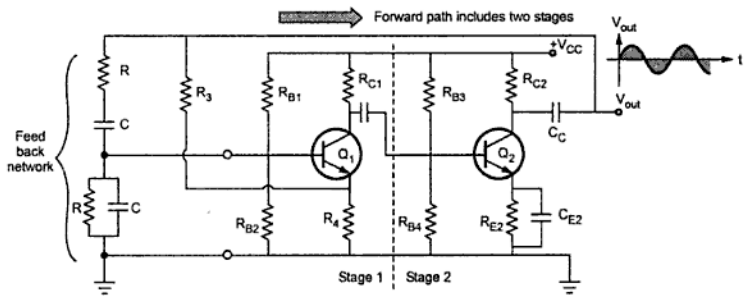


Fig. 2.18 Transistorised Wien bridge oscillator

The bridge consists of R and C in series, R and C in parallel, R_3 and R_4. The feedback is applied from the collector of Q_2 through the coupling capacitor, to the bridge circuit. The resistance R_4 serves the dual purpose of emitter resistance of the transistor Q_1 and also the element of the Wien bridge.

The two stage amplifier provides a gain much more than 3 and it is necessary to reduce it. To reduce the gain, the negative feedback is used without bypassing the resistance R_4. The negative feedback can accomplish the gain stability and can control the output magnitude. The negative feedback also reduces the distortion and therefore output obtained is a pure sinusoidal in nature. The amplitude stability can be improved using a nonlinear resistor for R_4. Due to this, the loop gain depends on the amplitude of the oscillations. Increase in the amplitude of the oscillations, increases the current through nonlinear resistance, which results into an increase in the value of nonlinear resistance R_4. When this value increases, a greater amount of negative feedback is applied. This reduces the loop gain. And hence signal amplitude gets reduced and controlled.

2.6.3 Wien Bridge Oscillator using Op-amp

If the amplifier circuit using transistors is replaced by the amplifier circuit using op-amp, with basic feedback network remains as the Wien bridge circuit, the oscillator is called Wien bridge oscillator using op-amp. The Fig. 2.19 shows the Wien bridge circuit using op-amp.

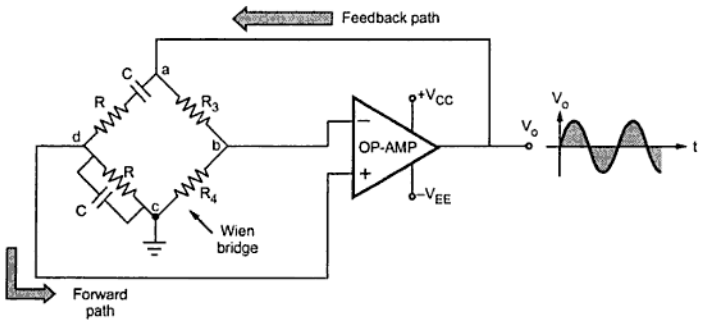


Fig. 2.19 Wien bridge oscillator using op-amp

The resistance R and capacitor C are the components of frequency sensitive arms of the bridge. The resistance R_3 and R_4 form the part of the feedback path. The op-amp output is connected to bridge input points a and c while bridge output points b and d are connected to the op-amp input. The gain of the op-amp can be adjusted by using the resistances R_3 and R_4. The gain of the op-amp is given by,

$$\boxed{A = 1 + \frac{R_3}{R_4}} \quad \ldots (9)$$

According to the oscillating conditions, $A \geq 3$.

$$\therefore \quad 1 + \frac{R_3}{R_4} \geq 3$$

$$\therefore \quad \boxed{\frac{R_3}{R_4} \geq 2} \quad \ldots (10)$$

Thus the ratio of R_3 and R_4 greater than or equal to two, will provide sufficient loop gain for the circuit to oscillate at the frequency calculated as,

$$\boxed{f = \frac{1}{2\pi RC}}$$

Key Point : *The op-amp is used in the non-inverting amplifier configuration to ensure the zero phase shift.*

Example 2.6 : *Determine whether the circuit shown in the Fig. 2.20, will work as an oscillator or not. If yes, determine the frequency of the oscillator.*

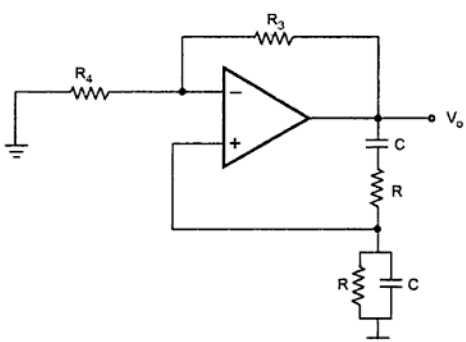


Fig. 2.20

Solution : The circuit is Wien bridge oscillator using op-amp. The gain of the op-amp is

$$A = 1 + \frac{R_3}{R_4} = 1 + \frac{6}{2} = 4$$

So $A > 3$

This satisfies the required oscillating condition. The feedback is given to non-inverting terminal ensuring the zero phase shift. Hence the circuit will work as the oscillator.

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 5.1\times 10^{3}\times 0.001\times 10^{-6}}$$

$$= \mathbf{31.2068\ kHz}$$

This will be the frequency of oscillations.

2.6.4 Wien Bridge Oscillator using FET

As a single stage FET amplifier gives a phase shift of 180° and it is required to have 360° phase shift from amplifier stage, the two stages of FET amplifier is the feature of the Wien bridge oscillator using FET.

The basic feedback network of Wien bridge remains same. Hence the condition of the oscillations, remains same.

The practical circuit of Wien bridge oscillator using two stage FET amplifier is shown in the Fig. 2.21.

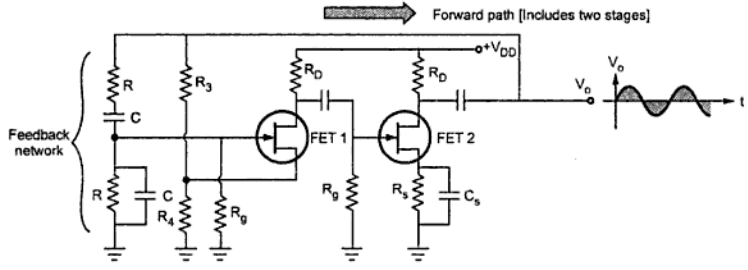


Fig. 2.21 FET Wien bridge oscillator

The RC series and parallel combination forms the frequency sensitive arms of the Wien bridge. The resistances R_3 and R_4 form the part of the feedback path. The unbypassed source resistance R_4 provides the negative feedback required for gain stabilization. The amplifier gain is the product of the gains of the two stages. The operation of the circuit is similar to the Wien bridge oscillator circuit with op-amp.

Key Point : *All the conditions derived earlier for the oscillating conditions are equally applicable to this circuit.*

Example 2.7 : *The frequency sensitive arms of the Wien bridge oscillator uses $C_1 = C_2 = 0.001\ \mu F$ and $R_1 = 10\ k\Omega$ while R_2 is kept variable. The frequency is to be varied from 10 kHz to 50 kHz, by varying R_2. Find the minimum and maximum values of R_2.*

Solution : The frequency of the oscillator is given by,

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

For $f = 10$ kHz,

$$10 \times 10^3 = \frac{1}{2\pi\sqrt{\left(10\times10^3 \times R_2 \times (0.001\times10^{-6}\right)^2}}$$

$\therefore$ $R_2 = \mathbf{25.33\ k\Omega}$

For $f = 50$ kHz

$$50 \times 10^3 = \frac{1}{2\pi\sqrt{\left(10\times10^3 \times R_2 \times (0.001\times10^{-6}\right)^2}}$$

$\therefore$ $R_2 = \mathbf{1.013\ k\Omega}$

So minimum value of R_2 is 1.013 kΩ while the maximum value of R_2 is 25.33 kΩ.

2.7 Comparison of RC Phase Shift and Wien Bridge Oscillators

The similarities and the differences between the two oscillators are given in the Table 2.2.

	RC Phase Shift Oscillator	Wien Bridge Oscillator
1.	It is a phase shift oscillator used for low frequency range.	It is also a phase shift oscillator used for low frequency range.
2.	The feedback network is RC network with three RC sections.	The feedback network is lead-lag network which is called Wien bridge circuit.
3.	The feedback network introduces 180° phase shift.	The feedback network does not introduce any phase shift.
4.	Amplifier circuit introduces 180° phase shift.	Amplifier circuit does not introduce any phase shift.
5.	The frequency of oscillations is, $f = \frac{1}{2\pi RC\sqrt{6}}$	The frequency of oscillations is, $f = \frac{1}{2\pi RC}$
6.	The amplifier gain condition is, $\|A\| \geq 29$	The amplifier gain condition is, $\|A\| \geq 3$
7.	The frequency variation is difficult.	Mounting the two capacitors on common shaft and varying their values, frequency can be varied.

Table 2.2

2.8 Tuned Oscillator Circuits

The oscillators which use the elements L and C to produce the oscillations are called LC oscillator or tuned oscillators. The circuit using elements L and C is called **tank circuit** or **oscillatory circuit**, which is an important part of LC oscillators. This circuit is also referred as resonating circuit, or tuned circuit. These oscillators are used for high frequency range from 200 kHz upto few GHz. Due to high frequency range, these oscillators are often used for sources of RF (radio frequency) energy. Let us study the basic action of LC tank circuit first.

2.8.1 Operation of LC Tank Circuit

The LC tank circuit consists of elements L and C connected in parallel as shown in the Fig. 2.22.

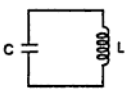


Fig. 2.22 LC tank circuit

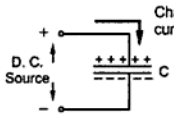


Fig. 2.23 Initial charging

Let capacitor is initially charged from a d.c. source with the polarities as shown in the Fig. 2.23.

When the capacitor gets charged, the energy gets stored in a capacitor called electrostatic energy. When such a charged capacitor is connected across inductor L in a tank circuit, the capacitor starts discharging through L, as shown in the Fig. 2.24. The arrow indicates direction of flow of conventional current. Due to such current flow, the magnetic field gets set up around the inductor L. Thus inductor starts storing the energy. When capacitor is fully discharged, maximum current flows through the circuit. At this instant all the electrostatic energy get stored as a magnetic energy in the inductor L. This is shown in the Fig. 2.25.

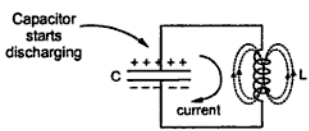


Fig. 2.24

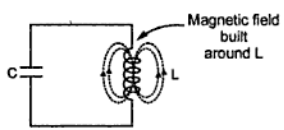


Fig. 2.25

Now the magnetic field around L starts collapsing. As per Lenz's law, this starts charging the capacitor with opposite polarity making lower plate positive and upper plate negative, as shown in the Fig. 2.26.

After some time, capacitor gets fully charged with opposite polarities, as compared to its initial polarities. This is shown in the Fig. 2.27. The entire magnetic energy gets converted back to electrostatic energy in capacitor.

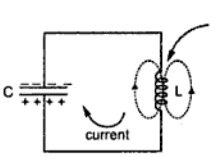


Fig. 2.26

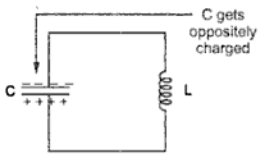


Fig. 2.27

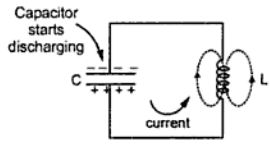


Fig. 2.28

Now capacitor again starts discharging through inductor L. But the direction of current through circuit is now opposite to the direction of current earlier in the circuit. This is shown in the Fig. 2.28. Again electrostatic energy is converted to magnetic energy. When capacitor is fully discharged, the magnetic field starts collapsing, charging the capacitor again in opposite direction.

Key Point: *Thus capacitor charges with alternate polarities and discharges producing alternating current in the tank circuit.*

This is nothing but oscillatory current. But every time when energy is transferred from C to L and L to C, the losses occur due to which amplitude of oscillating current keeps on decreasing everytime when energy transfer takes place. Hence actually we get exponentially decaying oscillations called damped oscillations. These are shown in the Fig. 2.29. Such oscillations stop after sometime.

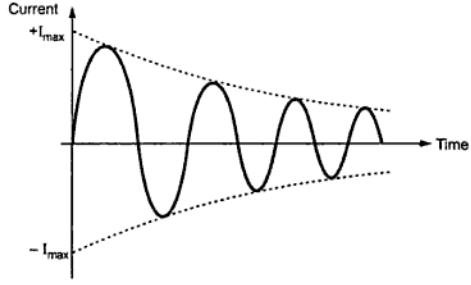


Fig. 2.29 Damped oscillations

Key Point : *In LC oscillator, the transistor amplifier supplies this loss of energy at the proper times.*

The care of proper polarity is taken by the feedback network. Thus LC tank circuit alongwith transistor amplifier can be used to obtain oscillators called LC oscillators. Due to supply of energy which is lost, the oscillations get maintained hence called **sustained oscillations** or **undamped oscillations**.

The frequency of oscillations generated by LC tank circuit depends on the values L and C and is given by,

$$f = \frac{1}{2\pi\sqrt{LC}}$$

where L is in henries and C is in farads.

2.8.2 Basic Form of LC Oscillator Circuit

As stated earlier, LC tuned circuit forms the feedback network while an op-amp, FET or bipolar junction transistor can be active device in the amplifier stage. The Fig. 2.30 (a) shows the basic form of LC oscillator circuit with gain of the amplifier as A_v. The amplifier output feeds the network consisting of impedances Z_1, Z_2 and Z_3. Assume an active device with infinite input impedance such as FET or op-amp. Then the basic circuit can be replaced by its linear equivalent circuit as shown in the Fig. 2.30 (b).

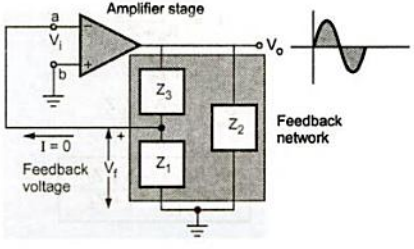


Fig. 2.30 (a) Basic form of LC oscillators

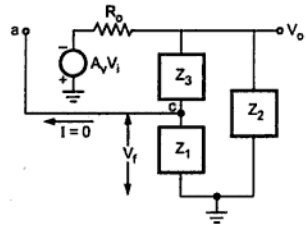


Fig. 2.30 (b) Equivalent circuit

Amplifier provides a phase shift of 180°, while the feedback network provides an additional phase shift of 180°, to satisfy the required condition.

i) Analysis of the amplifier stage

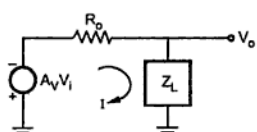


Fig. 2.31

As input impedance of the amplifier is infinite, there is no current flowing towards the input terminals. Let R_o be the output impedance of the amplifier stage.

As I = 0, Z_1, Z_3 appears in series and the combination in parallel with Z_2. The equivalent be Z_L i.e. load impedance. So circuit can be reduced, as shown in the Fig. 2.31.

$$\therefore \quad I = \frac{-A_V V_i}{R_o + Z_L} \qquad \ldots (1)$$

While $$V_o = I Z_L \qquad \ldots (2)$$

$$\therefore \quad V_o = \frac{-A_V V_i Z_L}{R_o + Z_L}$$

$$\therefore \quad \boxed{\frac{V_o}{V_i} = A = \frac{-A_V Z_L}{R_o + Z_L}} \qquad \ldots (3)$$

where A is the gain of the amplifier stage.

ii) Analysis of the feedback stage

For the feedback factor (β) calculation, consider only the feedback circuit as shown in the Fig. 2.32.

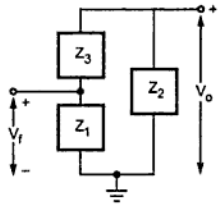


Fig. 2.32

From the voltage division in parallel circuit, we can write,

$$V_f = V_o\left[\frac{Z_1}{Z_1 + Z_3}\right] \quad \ldots (4)$$

$$\therefore \frac{V_f}{V_o} = \beta = \frac{Z_1}{Z_1 + Z_3} \quad \ldots (5)$$

But as the phase shift of the feedback network is 180°,

$$\therefore \quad \boxed{\beta = -\frac{Z_1}{Z_1 + Z_3}} \quad \ldots (6)$$

Obtain an expression for $-A\beta$ as basic Barkhausen condition is $-A\beta = 1$.
Refer equation (4) of the (section 2.3).

$$\therefore \quad -A\beta = \frac{-A_V Z_1 Z_L}{(R_o + Z_L)\times(Z_1 + Z_3)} \quad \ldots (7)$$

This is the required loop gain. Now Z_L can be written as $(Z_1 + Z_3) \| Z_2$ i.e.

$$Z_L = \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3} \quad \ldots (8)$$

$$\therefore \quad -A\beta = \frac{-A_V Z_1 \left[\frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}\right]}{\left[R_o + \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}\right](Z_1 + Z_3)}$$

Dividing numerator and denominator by $\frac{(Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}$,

$$= \frac{-A_V Z_1 Z_2}{\left[\frac{R_o (Z_1 + Z_2 + Z_3)}{(Z_1 + Z_3)} + Z_2\right](Z_1 + Z_3)}$$

$$= \frac{-A_V Z_1 Z_2}{R_o (Z_1 + Z_2 + Z_3) + Z_2 (Z_1 + Z_3)} \quad \ldots (9)$$

As Z_1 Z_2 and Z_3 are the pure reactive elements,

$$Z_1 = jX_1, \quad Z_2 = jX_2 \quad \text{and} \quad Z_3 = jX_3$$

where $X = \omega L$ for an inductive reactance

and $X = \frac{-1}{\omega C}$ for a capacitive reactance.

$$-A\beta = \frac{-A_V (jX_1)(jX_2)}{R_o (jX_1 + jX_2 + jX_3) + jX_2 (jX_1 + jX_3)}$$

$$\boxed{-A\beta = \frac{A_V X_1 X_2}{-X_2 (X_1 + X_3) + jR_o (X_1 + X_2 + X_3)}} \quad \ldots (10)$$

To have 180° phase shift, the imaginary part of the denominator must be zero.

$$\therefore \quad \boxed{X_1 + X_2 + X_3 = 0} \quad \ldots (11)$$

Substituting in the equation (10),

$$-A\beta = \frac{-A_V X_1 X_2}{X_2 (X_1 + X_3)}$$

But from the equation (11), $X_1 + X_3 = -X_2$

$$\therefore \quad -A\beta = \frac{-A_V X_1}{-X_2} = +A_V \left(\frac{X_1}{X_2}\right) \quad \ldots (12)$$

According to the Barkhausen criterion, $-A\beta$ must be positive and must be greater than or equal to unity. As A_V is positive, the $-A\beta$ will be positive only when X_1 and X_2 will have same sign. This indicates that X_1 and X_2 must be of same type of reactances either both inductive or capacitive.

While from the equation (11), we can say that $X_3 = -(X_1 + X_2)$ must be inductive if X_1, X_2 are capacitive while X_3 must be capacitive if X_1, X_2 are inductive.

Table 2.3 shows the various types of the LC oscillators depending on the design of the reactances X_1, X_2 and X_3.

Oscillator type	Reactance elements in the tank circuit		
	X_1	X_2	X_3
Hartley oscillator	L	L	C
Colpitts oscillator	C	C	L

Table 2.3

2.9 Hartley Oscillator

As seen earlier, a LC oscillator which uses **two inductive reactances** and **one capacitive reactance** in its feedback network is called **Hartley Oscillator.**

2.9.1 Transistorised Hartley Oscillator

The amplifier stage uses an active device as a transistor in common emitter configuration. The practical circuit is shown in the Fig. 2.33.

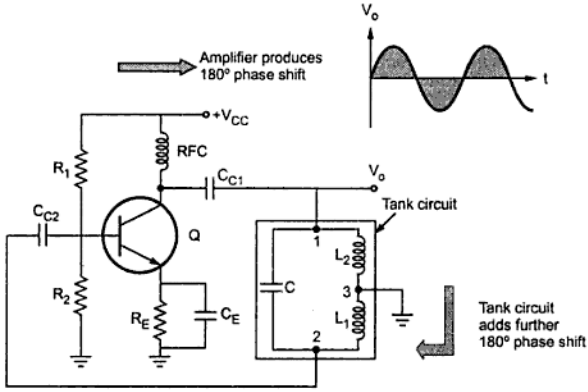


Fig. 2.33 Transistorised Hartley oscillator

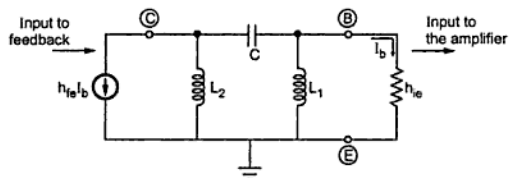
The resistances R_1 and R_2 are the biasing resistances. The RFC is the radio frequency choke. Its reactance value is very high for high frequencies, hence it can be treated as open circuit. While for d.c. conditions, the reactance is zero hence causes no problem for d.c. capacitors.

Hence due to RFC, the isolation between a.c. and d.c. operation is achieved. R_E is also a biasing circuit resistance and C_E is the emitter bypass capacitor. C_{C1} and C_{C2} are the coupling capacitor.

The common emitter amplifier provides a phase shift of 180°. As emitter is grounded, the base and the collector voltages are out of phase by 180°. As the centre of L_1 and L_2 is grounded, when upper end becomes positive, the lower becomes negative and viceversa. So the LC feedback network gives an additional phase shift of 180°, necessary to satisfy oscillation conditions.

2.9.2 Derivation of Frequency of Oscillations

The output current which is the collector current is $h_{fe}I_b$ where I_b is the base current. Assuming coupling condensers are short, the capacitor C is between base and collector.



The inductance L_1 is between base and emitter while the inductance L_2 is between collector and emitter. The equivalent circuit of the feedback network is shown in the Fig. 2.34.

Fig. 2.34 Equivalent circuit

As h_{ie} is the input impedance of the transistor. The output of the feedback is the current I_b which is the input current of the transistor. While input to the feedback network is the output of the transistor which is $I_c = h_{fe}I_b$, converting current source into voltage source we get,

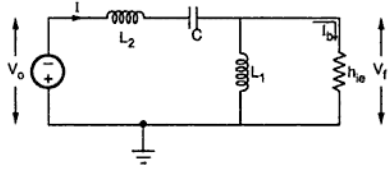


Fig. 2.35 Simplified equivalent circuit

$$V_o = h_{fe}I_b X_{L2} = h_{fe}I_b j\omega L_2 \quad \ldots (1)$$

Now L_1 and h_{ie} are in parallel, so the total current I drawn from the supply is,

$$I = \frac{-V_o}{[X_{L2} + X_C] + [X_{L1} \| h_{ie}]} \quad \ldots (2)$$

Key Point : *Negative sign, as current direction shown in opposite to the polarities of V_o.*

Now $$X_{L2} + X_C = j\omega L_2 + \frac{1}{j\omega C}$$

and $$X_{L1} \| h_{ie} = \frac{j\omega L_1 h_{ie}}{(j\omega L_1 + h_{ie})}$$

Substituting in the equation (2) we get,

$$I = \frac{-h_{fe} I_b j\omega L_2}{\left[j\omega L_2 + \frac{1}{j\omega C}\right] + \frac{j\omega L_1 h_{ie}}{(j\omega L_1 + h_{ie})}} \quad \ldots (3)$$

Replacing $j\omega$ by s,

$$I = \frac{-s h_{fe} I_b L_2}{\left[s L_2 + \frac{1}{sC}\right] + \frac{s L_1 h_{ie}}{(s L_1 + h_{ie})}}$$

$$= \frac{-s h_{fe} I_b L_2}{\frac{[1+s^2 L_2 C]}{sC} + \frac{s L_1 h_{ie}}{(s L_1 + h_{ie})}}$$

$$= \frac{-s\, h_{fe} I_b L_2 (sC)(s L_1 + h_{ie})}{[1+s^2 L_2 C][s L_1 + h_{ie}] + (sC)(s L_1 h_{ie})}$$

$$= \frac{-s^2 h_{fe} I_b L_2 C(s L_1 + h_{ie})}{s^3 L_1 L_2 C + sL_1 + h_{ie} + s^2 L_2 C h_{ie} + s^2 L_1 C h_{ie}}$$

$$= \frac{-s^2 h_{fe} I_b L_2 C(s L_1 + h_{ie})}{s^3 L_1 L_2 C + s^2 C\, h_{ie}(L_1 + L_2) + s L_1 + h_{ie}}$$

According to current division in parallel circuit,

$$I_b = I \times \frac{X_{L1}}{XL_1 + h_{ie}}$$

$$= I \times \frac{j\omega L_1}{(j\omega L_1 + h_{ie})}$$

$$\boxed{I_b = I \times \left[\frac{sL_1}{(sL_1 + h_{ie})}\right]} \quad \ldots (4)$$

Substituting value of I from equation (3) in equation (4),

$$I_b = \frac{-s^2 h_{fe} I_b L_2 C(sL_1 + h_{ie})}{[s^3 (L_1 L_2 C) + s^2 C\, h_{ie}(L_1 + L_2) + sL_1 + h_{ie}]} \times \frac{sL_1}{(sL_1 + h_{ie})}$$

$$= \frac{-s^3 h_{fe} I_b C L_1 L_2}{s^3 (L_1 L_2 C) + s^2 C h_{ie}(L_1 + L_2) + sL_1 h_{ie}}$$

$$\therefore \quad 1 = \frac{-s^3 h_{fe} C L_1 L_2}{s^3 (L_1 L_2 C) + s^2 C h_{ie}(L_1 + L_2) + sL_1 + h_{ie}} \quad \ldots (5)$$

Substituting $s = j\omega$, $s^2 = -\omega^2$, $s^3 = -j\omega^3$ we get

$$\therefore \quad 1 = \frac{j\omega^3 h_{fe} C L_1 L_2}{-j\omega^3 L_1 L_2 C - \omega^2 C h_{ie}(L_1 + L_2) + j\omega L_1 + h_{ie}}$$

$$= \frac{j\omega^3 h_{ie} C L_1 L_2}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)] + j\omega L_1 (1 - \omega^2 L_2 C)} \quad \ldots (6)$$

Rationalising the R.H.S of the above equation,

$$\therefore \quad 1 = \frac{j\omega^3 h_{fe} C L_1 L_2 [h_{ie} - \omega^2 C h_{ie}(L_1 + L_2) - j\omega L_1 (1 - \omega^2 L_2 C)]}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)]^2 + \omega^2 L_1^2 (1 - \omega^2 L_2 C)^2}$$

$$= \frac{\omega^4 h_{fe} L_1^2 L_2 C(1 - \omega^2 L_2 C) + j\omega^3 h_{fe} L_1 L_2 C [h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)}{[h_{ie} - \omega^2 C h_{ie}(L_1 + L_2)]^2 + \omega^2 L_1^2 (1 - \omega^2 L_1^2 L_2 C)^2} \quad \ldots (7)$$

To satisfy this equation, imaginary part of R. H. S. must be zero.

$$\therefore \quad \boxed{\omega^3 h_{fe} L_1 L_2 C [h_{ie} - \omega^2 h_{ie} C (L_1 + L_2)] = 0}$$

$$\therefore \quad \omega^3 h_{fe} h_{ie} L_1 L_2 C [1 - \omega^2 C (L_1 + L_2)] = 0$$

$$\therefore \quad 1 - \omega^2 C (L_1 + L_2) = 0$$

$$\therefore \quad \omega^2 = \frac{1}{C(L_1 + L_2)}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{C(L_1 + L_2)}}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{C(L_1 + L_2)}}} \qquad \ldots (8)$$

This is the frequency of the oscillations. At this frequency, the restriction of the value of h_{fe} can be obtained, by equating the magnitudes of the both sides of the equation (7).

$$\therefore \quad 1 = \frac{\omega^4 h_{fe} L_1^2 L_2 C(1 - \omega^2 L_2 C)}{0 + \omega^2 L_1^2 (1 - \omega^2 L_2 C)^2} \text{ at } \omega = \frac{1}{\sqrt{C(L_1 + L_2)}}$$

$$\therefore \quad 1 = \frac{h_{fe} L_2}{(1 - \omega^2 L_2 C)} \text{ at } \omega = \frac{1}{\sqrt{C(L_1 + L_2)}}$$

$$\therefore \quad 1 = \frac{h_{fe} L_2}{\left[1 - \dfrac{L_2 C}{C(L_1 + L_2)}\right]} = \frac{h_{fe} L_2}{L_1}$$

$$\therefore \quad \boxed{h_{fe} = \frac{L_1}{L_2}} \qquad \ldots (9\ a)$$

This is the value of h_{fe}, required to satisfy the oscillating conditions.

For a mutual inductance of M,

$$\boxed{h_{fe} = \frac{L_1 + M}{L_2 + M}} \qquad \ldots (9\ b)$$

Now $L_1 + L_2$ is the equivalent inductance of the two inductances L_1 and L_2, connected in series denoted as

$$\boxed{L_{eq} = L_1 + L_2} \qquad \ldots (10)$$

Hence the frequency of oscillations is given by,

$$f = \frac{1}{2\pi\sqrt{C L_{eq}}} \quad \ldots (11)$$

So if the capacitor C is kept variable, frequency can be varied over a large range as per the requirement.

In practice, L_1 and L_2 may be wound on a single core so that there exists a mutual inductance between them denoted as M.

In such a case, the mutual inductance is considered while determining the equivalent inductance L_{eq}. Hence,

$$L_{eq} = L_1 + L_2 + 2M \quad \ldots (12)$$

If L_1 and L_2 are assisting each other then sign of 2M is positive while if L_1 and L_2 are in series opposition then sign of 2M is negative.

The expression for the frequency of the oscillations remain same as given by (11).

A practical circuit where the mutual inductance exists between L_1 and L_2, of transistorised Hartley oscillator is shown in the Fig. 2.36.

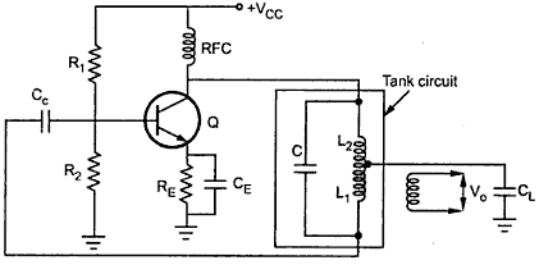


Fig. 2.36 Another form of transistorised Hartley oscillator

Example 2.8 : *In a transistorised Hartley oscillator the two inductances are 2 mH and 20 μH while the frequency is to be changed from 950 kHz to 2050 kHz. Calculate the range over which the capacitor is to be varied.*

Solution : The frequency is given by,

$$f = \frac{1}{2\pi\sqrt{C (L_{eq})}}$$

Where $L_{eq} = L_1 + L_2 = 2\times10^{-3} + 20\times10^{-6}$

$= 0.00202$ kHz

For $f = f_{max} = 2050$ kHz

$$2050\times10^3 = \frac{1}{2\pi\sqrt{C\times0.00202}}$$

$\therefore$ $C = 2.98$ pF

For $f = f_{min} = 950$ kHz

$$950\times10^3 = \frac{1}{2\pi\sqrt{C\times0.00202}} \quad C = 13.89 \text{ pF}$$

Hence C must be varied from 2.98 pF to 13.89 pF, to get the required frequency variation.

2.9.3 FET Hartley Oscillator

If FET is used as an active device in an amplifier stage, then the circuit is called FET Hartley oscillator. The practical circuit is shown in the Fig. 2.37.

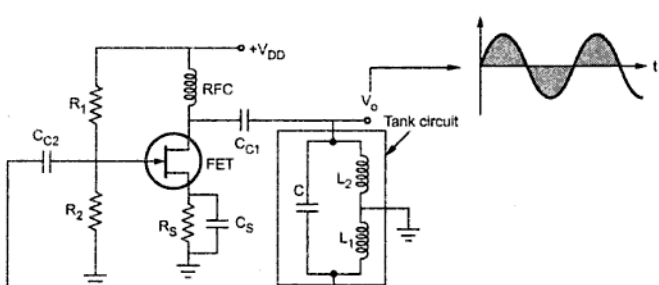


Fig. 2.37 FET Hartley oscillator

The resistances R_1, R_2 bias the FET along with R_S. The C_S in the source bypass capacitor. To maintain Q point stable, coupling capacitors C_{C1}, C_{C2} are used. These have very large values compared to capacitor C. The tank circuit is shown in a box.

We know,

$$X_1 + X_2 + X_3 = 0$$

And $X_1 = j\omega L_1$, $X_2 = j\omega L_2$ and $X_3 = \frac{1}{j\omega C}$

Solving for ω, we get the same expression for the frequency as derived earlier.

$$f = \frac{1}{2\pi\sqrt{C L_{eq}}}$$

where $L_{eq} = L_1 + L_2$ or $L_1 + L_2 + 2M$

This is dependent on whether L_1, L_2 are wound on the same core or not.

If $L_1 = L_2 = L$, then the frequency of oscillations is given by,

$$f = \frac{1}{2\pi\sqrt{2}\sqrt{LC}} \quad \ldots (13)$$

The condition for μ of FET for the oscillations is given by,

$$\mu = \frac{L_1}{L_2}$$

While if mutual inductance M exists then,

$$\mu = \frac{L_1 + M}{L_2 + M}$$

2.9.4 Hartley Oscillator using Op-amp

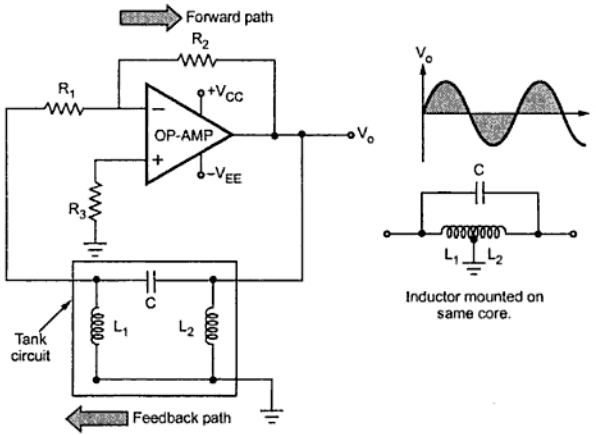
If operational amplifier circuit is used in an amplifier stage, then the circuit is called Hartley oscillator using op-amp. The practical circuit is shown in the Fig. 2.38(a).

The operation of the circuit is similar to the transistorised Hartley oscillator. The frequency of the oscillations is also given by the same expression derived earlier.

$$f = \frac{1}{2\pi\sqrt{C L_{eq}}}$$

where $L_{eq} = L_1 + L_2$ or $L_1 + L_2 + 2M$

Tank circuit in which L_1 and L_2 are wound on same core, is shown in the Fig. 2.38 (b).



(a) Oscillator circuit **(b) Tank circuit L_1, L_2 on same core**

Fig. 2.38 Hartley oscillator using op-amp

For the oscillations, the amplifier gain must be selected greater than or at least equal to the ratio of the two inductances.

$$A_v = \frac{L_1}{L_2} \quad \text{... (14)}$$

If the mutual inductance exists between L_1 and L_2 then

$$A_v = \frac{L_1 + M}{L_2 + M} \quad \text{... (15)}$$

This is similar to the result obtained in the equation (4) of section 2.9.2.

Example 2.9 : *Calculate the frequency of oscillations of a Hartley oscillator having $L_1 = 0.5$ mH, $L_2 = 1$ mH and $C = 0.2$ μF.*

Solution : The given values are,

$$L_1 = 0.5 \text{ mH}, \quad L_2 = 1 \text{ mH}, \quad C = 0.2 \text{ μF}$$

Now $$f = \frac{1}{2\pi\sqrt{L_{eq} C}}$$

and $$L_{eq} = L_1 + L_2 = 0.5 + 1 = 1.5 \text{ mH}$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{1.5\times10^{-3}\times0.2\times10^{-6}}} = \mathbf{9.19\ kHz}$$

Example 2.10 : *In a Hartley oscillator $L_1 = 20\,\mu H$, $L_2 = 2$ mH and C is variable. Find the range of C if frequency is to be varied from 1 MHz to 2.5 MHz. Neglect mutual inductance.*

Solution : $L_1 = 20\,\mu H$, $L_2 = 2$ mH

$$\therefore \quad L_{eq} = L_1 + L_2 = 20\times10^{-6} + 2\times10^{-3} = 2.002\times10^{-3}\ H$$

For $f = f_{max} = 2.5$ MHz.

$$f = \frac{1}{2\pi\sqrt{C\times L_{eq}}}$$

$$\therefore \quad 2.5\times10^{6} = \frac{1}{2\pi\sqrt{C\times2.002\times10^{-3}}}$$

$$\therefore \quad C = \mathbf{2.0244\ pF}$$

For $f = f_{min} = 1$ MHz.

$$1\times10^{6} = \frac{1}{2\pi\sqrt{C\times2.002\times10^{-3}}}$$

$$\therefore \quad C = \mathbf{12.6525\ pF}$$

Thus C must be varied from 2.0244 pF to 12.6525 pF.

2.10 Colpitts Oscillator

An LC oscillator which uses two capacitive reactances and one inductive reactance in the feedback network i.e. tank circuit, is called **Colpitts oscillator**.

2.10.1 Transistorised Colpitts Oscillator

The amplifier stage uses an active device as a transistor in common emitter configuration. The practical circuit is shown in the Fig. 2.39.

The basic circuit is same as transistorised Hartley oscillator, except the tank circuit. The common emitter amplifier causes a phase shift of 180°, while the tank circuit adds further 180° phase shift, to satisfy the oscillating conditions.

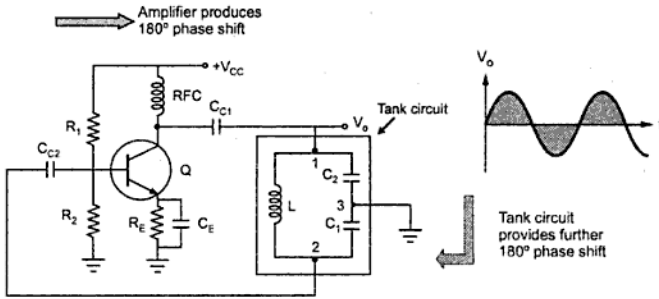


Fig. 2.39 Transistorised Colpitts oscillator

2.10.2 Derivation of frequency of Oscillations

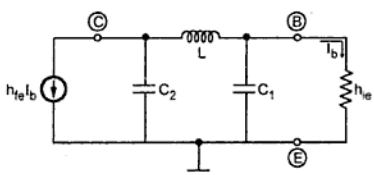


Fig. 2.40 Equivalent circuit

As seen earlier, the output current I_c which is h_{fe} I_b acts as input to the feedback network. While the base current I_b acts as the output current of the tank circuit, flowing through the input impedance of the amplifier h_{ie}. The equivalent circuit of the tank circuit is shown in the Fig. 2.40.

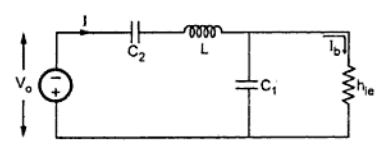


Fig. 2.41 Simplified equivalent circuit

Converting the current source into the voltage source. We get the equivalent circuit as shown in the Fig. 2.41.

$$V_o = h_{fe}\, I_b\, X_{C2} = h_{fe}\, I_b \frac{1}{j\omega C_2} \quad \ldots (1)$$

The total current I, drawn from the supply is,

$$I = \frac{-V_o}{[X_{C2} + X_L] + [X_{C1} \,||\, h_{ie}]} \quad \ldots (2)$$

Key Point : *The negative sign is because the current direction is assumed in the opposite direction to that, would be due to the polarities of* V_o.

Now $$X_{C2} + X_L = \frac{1}{j\omega C_2} + j\omega L$$

and $$X_{C1} \,||\, h_{ie} = \frac{\frac{1}{j\omega C_1} \times h_{ie}}{\left[\frac{1}{j\omega C_1} + h_{ie}\right]}$$

Substituting in the equation (2),

$$\therefore \quad I = \frac{-h_{fe} I_b \left(\frac{1}{j\omega C_2}\right)}{\left[\frac{1}{j\omega C_2} + j\omega L\right] + \left[\frac{\frac{h_{ie}}{j\omega C_1}}{h_{ie} + \frac{1}{j\omega C_1}}\right]} \quad \ldots (3)$$

Replacing jω by s,

$$\therefore \quad I = \frac{-h_{fe} I_b \left(\frac{1}{sC_2}\right)}{\left[\frac{1}{sC_2} + sL\right] + \left[\frac{\frac{h_{ie}}{sC_1}}{h_{ie} + \frac{1}{sC_1}}\right]}$$

$$= \frac{-h_{fe} I_b \left(\frac{1}{sC_2}\right)}{\frac{(1 + s^2 L C_2)}{sC_2} + \left[\frac{h_{ie}}{1 + sC_1 h_{ie}}\right]}$$

$$= \frac{-h_{fe} I_b \left(\frac{1}{sC_2}\right)(sC_2)(1 + sC_1 h_{ie})}{(1 + s^2 L C_2)(1 + sC_1 h_{ie}) + sC_2 h_{ie}}$$

$$= \frac{-h_{fe} I_b (1 + sC_1 h_{ie})}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + sC_1 h_{ie} + 1 + sC_2 h_{ie}}$$

$$= \frac{-h_{fe} I_b (1 + s C_1 h_{ie})}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + s h_{ie} (C_1 + C_2) + 1} \quad \ldots (4)$$

According to the current division in the parallel circuit,

$$I_b = I \times \frac{X_{C1}}{(X_{C1} + h_{ie})} = \frac{I \times \frac{1}{j\omega C_1}}{\left(h_{ie} + \frac{1}{j\omega C_1}\right)}$$

$$\therefore \quad \boxed{I_b = \frac{I}{(1 + s h_{ie} C_1)}} \quad \ldots (5)$$

Substituting value of I from the equation (4) in equation (5) we get,

$$\therefore \quad I_b = \frac{-h_{fe} I_b (1 + s C_1 h_{ie})}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + s h_{ie} (C_1 + C_2) + 1} \times \frac{1}{(1 + s C_1 h_{ie})}$$

$$= \frac{-h_{fe} I_b}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + s h_{ie} (C_1 + C_2) + 1}$$

$$\therefore \quad \boxed{1 = \frac{-h_{fe}}{s^3 L C_1 C_2 h_{ie} + s^2 L C_2 + s h_{ie} (C_1 + C_2) + 1}} \quad \ldots (6)$$

Replacing s by $j\omega$, and s^2 by $-\omega^2$ and s^3 by $-j\omega^3$

$$\therefore \quad 1 = \frac{-h_{fe}}{-j\omega^3 L C_1 C_2 h_{ie} - \omega^2 L C_2 + j\omega h_{ie} (C_1 + C_2) + 1}$$

$$= \frac{-h_{fe}}{(1 - \omega^2 L C_2) + j\omega h_{ie} [C_1 + C_2 - \omega^2 L C_1 C_2]} \quad \ldots (7)$$

There is no need to rationalise this as there are no j terms in the numerator, as in the equation (6) of section 2.9.2.

It can be seen that, to satisfy the equation, the imaginary part of the denominator of the right hand side must be zero.

$$\therefore \quad \boxed{\omega h_{ie} [C_1 + C_2 - \omega^2 L C_1 C_2] = 0}$$

$$\therefore \quad C_1 + C_2 - \omega^2 L C_1 C_2 = 0 \quad \ldots \text{Neglecting zero value of } \omega$$

$$\therefore \quad \omega^2 = \frac{(C_1 + C_2)}{L C_1 C_2} = \frac{1}{L\left[\frac{C_1 C_2}{(C_1 + C_2)}\right]}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{L\left[\frac{C_1 C_2}{(C_1 + C_2)}\right]}}}$$

Now $\frac{C_1 C_2}{C_1 + C_2}$ is nothing but the equivalent of two capacitors C_1 and C_2 in series.

$$\therefore \quad C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{L C_{eq}}}} \qquad \ldots (8)$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{L C_{eq}}}} \qquad \ldots (9)$$

This is the frequency of the oscillations in the Colpitts oscillator.

Substituting this frequency in the equation (7) and equating the magnitudes of the both sides, the restriction on the value of h_{fe} can be obtained as,

$$\therefore \quad \boxed{h_{fe} = \frac{C_2}{C_1}} \qquad \ldots (10)$$

Key Point : *Thus the behaviour of Colpitts oscillator is similar to the Hartley oscillator, as basic LC oscillator circuit is same, except the tank circuit.*

Let us see the FET and op-amp versions of the Colpitts oscillator.

2.10.3 Colpitts Oscillator using Op-amp

If in the basic circuit of Colpitts oscillator, the op-amp is used for an amplifier stage, the circuit is caused as Colpitts oscillator using op-amp. The tank circuit remains same as before. The practical circuit of Colpitts oscillator using op-amp is shown in the Fig. 2.42.

The oscillator frequency is given by the equation (9).

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{L C_{eq}}}}$$

where $\boxed{C_{eq} = \frac{C_1 C_2}{C_1 + C_2}}$

Key Point : *The condition on the transistor amplifier gain is now applicable for the op-amp gain.*

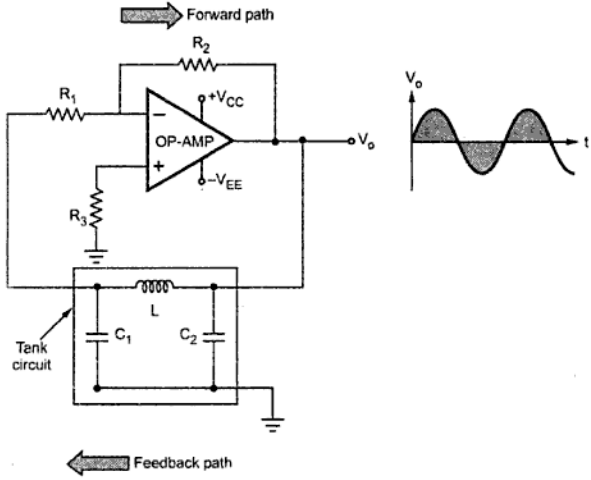


Fig. 2.42 Colpitts oscillator using op-amp

But in practice the gain is required to be designed much higher than given by the equation (10). This is mainly because of neglected inductor resistance and effect of the stray capacitance which is dominant at high frequencies.

2.10.4 Colpitts Oscillator using FET

If in the basic circuit of Colpitts oscillator, the FET is used as an active device in the amplifier stage, the circuit is called as FET Colpitts oscillator. The tank circuit remains same as before. The working of the circuit and oscillating fequency also remains the same.

The practical circuit of FET Colpitts oscillator is shown in the Fig. 2.43.

The condition for μ of FET for the oscillations is given by,

$$\mu = \frac{C_2}{C_1}$$

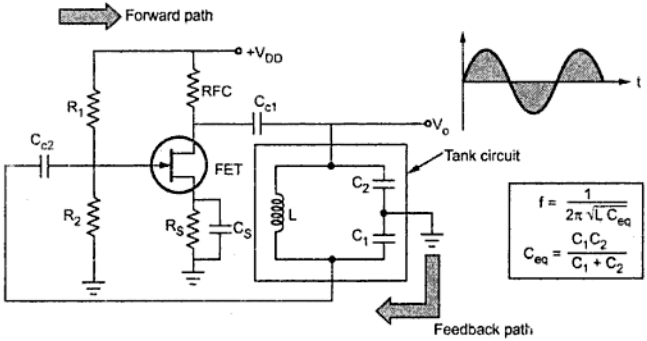


Fig. 2.43 FET Colpitts oscillator

Example 2.11 : *Find the frequency of the oscillations of a transistorised Colpitts oscillator having $C_1 = 150$ pF, $C_2 = 1.5$ nF and $L = 50$ μH*

Solution :

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{150\times10^{-12}\times1.5\times10^{-9}}{[150\times10^{-12} + 1.5\times10^{-9}]}$$

$$= 136.363 \text{ pF}$$

Now

$$f = \frac{1}{2\pi\sqrt{L\,C_{eq}}} = \frac{1}{2\pi\sqrt{50\times10^{-6}\times136.363\times10^{-12}}}$$

$$= \mathbf{1.927\ MHz}$$

Example 2.12 : *In a Colpitts oscillator, $C_1 = C_2 = C$ and $L = 100$ μH. The frequency of oscillations is 500 kHz. Determine value of C.*

Solution : The given values are,

$$L = 100\ \mu H,\ C_1 = C_2 = C \text{ and } f = 500 \text{ kHz}$$

Now

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$\therefore \quad 500\times10^3 = \frac{1}{2\pi\sqrt{100\times10^{-6}\times C_{eq}}}$$

$$\therefore \quad (500\times10^3)^2 = \frac{1}{4\pi^2\times100\times10^{-6}\times C_{eq}}$$

$$\therefore \quad C_{eq} = 1.0132\times10^{-9}\ F$$

but $$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \quad \text{and} \quad C_1 = C_2 = C$$

$$\therefore \quad C_{eq} = \frac{C\times C}{C + C} = \frac{C}{2}$$

$$\therefore \quad 1.0132\times10^{-9} = \frac{C}{2}$$

$$\therefore \quad C = 2.026\times10^{-9}\ F = \mathbf{2.026\ nF}$$

Example 2.13 : *Design the value of an inductor to be used in Colpitts oscillator to generate a frequency of 10 MHz. The circuit is used a value of C_1 = 100 pF and C_2 = 50 pF.*

Solution : Given, C_1 = 100 pF, C_2 = 50 pF, f = 10 MHz, L = ?

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{5000\times10^{-12}\times10^{-12}}{150\times10^{-12}} = C_{eq} = 33.33\times10^{-12}\ F$$

$$f = \frac{1}{2\pi\sqrt{L\,C_{eq}}}$$

$$10\times10^{6} = \frac{1}{2\pi\sqrt{L\,33.33\times10^{-12}}}$$

$$(10\times10^{6})^2 = \frac{1}{4\pi^2 L\,33.33\times10^{-12}}$$

$$L = \frac{1}{4\pi^2(10\times10^{6})^2(33.33\times10^{-12})} = 7.6\times10^{-6}\ H$$

$$= \mathbf{7.6\ \mu H}$$

2.11 Clapp Oscillator

To achieve the frequency stability, Colpitts oscillator circuit is slightly modified in practice, called Clapp oscillator. The basic tank circuit with two capacitive reactances and one inductive reactance remains same. But the modification in the tank circuit is that **one more capacitor C_3 is introduced in series with the inductance** as shown in the Fig. 2.44.

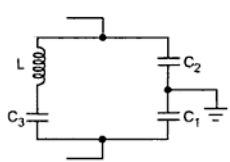


Fig. 2.44 Modified tank circuit

Key Point : *The value of C_3 is much smaller than the values of C_1 and C_2.*

Now the equivalent capacitance becomes,

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \quad \ldots (1)$$

While the oscillator frequency is given by the same expression as,

$$f = \frac{1}{2\pi\sqrt{L\,C_{eq}}} \quad \ldots (2)$$

Suppose $C_1 = C_2 = 0.001\ \mu F$, $L = 15\ \mu H$ and the new capacitor $C_3 = 50$ pF

so, $$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$$

$\therefore$ $$C_{eq} = 4.545 \times 10^{-11}$$

$\therefore$ $$f = \frac{1}{2\pi\sqrt{L\,C_{eq}}} = \frac{1}{2\pi\sqrt{15\times10^{-6}\times4.545\times50\times10^{-11}}} = 6.09\ \text{MHz}$$

If C_1 and C_2 are neglected then $C_{eq} = C_3$

$\therefore$ $$f = \frac{1}{2\pi\sqrt{L\,C_3}} = \frac{1}{2\pi\sqrt{15\times10^{-6}\times50\times10^{-12}}} = 5.82\ \text{MHz}$$

The frequencies are almost same, hence in practice the C_1, C_2 values are neglected and C_3 is assumed to be C_{eq}. Hence the frequency is given by,

$$f = \frac{1}{2\pi\sqrt{L\,C_3}} \quad \ldots (3)$$

Now across C_3, there is no transistor parameter and hence the frequency of the Clapp oscillator is stable and accurate. The transistor and stray capacitances have no effect on C_3 hence good frequency stability is achieved in Clapp oscillator. Hence practically Clapp oscillator is preferred over Colpitts oscillator. The transistorised Clapp oscillator is shown in the Fig. 2.45.

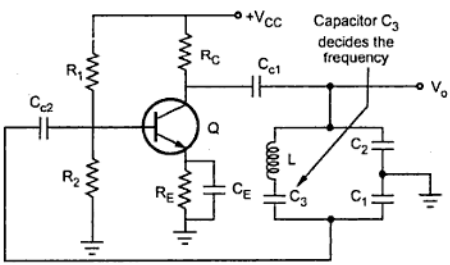


Fig. 2.45 Transistorised Clapp oscillator

Another advantage of C_3 is that it can be kept variable. As frequency is dependent on C_3, the frequency can be varied in the desired range.

2.11.1 Derivation of Frequency of Oscillations

The derivation is similar to the Colpitt's oscillator with C_3 in series with L in the equivalent circuit of transistorised Clapp oscillator. The equivalent circuit is shown in the Fig. 2.46.

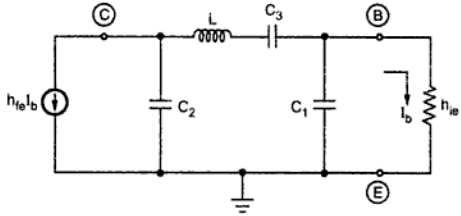


Fig. 2.46

Converting current source to voltage source we get the equivalent circuit as shown in the Fig. 2.47.

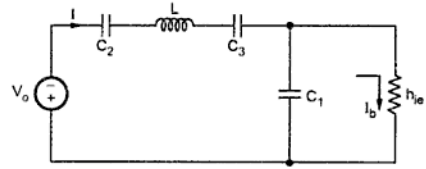


Fig. 2.47

$$V_o = h_{fe} I_b X_{C2}$$

$$\therefore \quad \boxed{V_o = h_{fe} I_b \cdot \frac{1}{j\omega C_2}} \qquad \ldots (4)$$

$$\therefore \quad I = \frac{-V_o}{[X_{C2} + X_{C3} + X_L] + [X_{C1} || h_{ie}]} \qquad \ldots (5)$$

The negative sign as the direction of I is assumed opposite to that which voltage source will force the current I through the circuit.

$$X_{C2} + X_{C3} + X_L = \frac{1}{j\omega C_2} + \frac{1}{j\omega C_3} + j\omega L$$

$$X_{C1} \parallel h_{ie} = \frac{\frac{1}{j\omega C_1} \times h_{ie}}{\frac{1}{j\omega C_1} + h_{ie}}$$

$$\therefore \quad I = \frac{-h_{fe} I_b \cdot \frac{1}{j\omega C_2}}{\frac{1}{j\omega C_2} + \frac{1}{j\omega C_3} + j\omega L + \left[\frac{\frac{1}{j\omega C_1} h_{ie}}{\frac{1}{j\omega C_1} + h_{ie}}\right]} \quad \ldots(6)$$

Replacing $j\omega$ by s,

$$I = \frac{-h_{fe} I_b \cdot \frac{1}{s C_2}}{\frac{1}{s C_2} + \frac{1}{s C_3} + sL + \left[\frac{\frac{h_{ie}}{s C_1}}{\frac{1}{s C_1} + h_{ie}}\right]} \quad \ldots (7)$$

$$= \frac{-h_{fe} I_b}{1 + \frac{C_2}{C_3} + s^2 L C_2 + \frac{s C_2 h_{ie}}{(1 + s C_1 h_{ie})}} \quad \ldots \text{Multiplying by } sC_2 \text{ to denominator}$$

$$= \frac{-h_{fe} I_b \cdot C_3}{C_3 + C_2 + s^2 L C_2 C_3 + \frac{s C_2 C_3 h_{ie}}{(1 + s C_1 h_{ie})}}$$

$$= \frac{-h_{fe} I_b C_3 (1 + s C_1 h_{ie})}{C_3 + sC_1 C_3 h_{ie} + C_2 + sC_1 C_2 h_{ie} + s^2 L C_2 C_3 + s^3 L C_1 C_2 C_3 h_{ie} + s C_2 C_3 h_{ie}}$$

$$\therefore \quad I = \frac{-h_{fe} I_b C_3 (1 + s C_1 h_{ie})}{s^3 L C_1 C_2 C_3 h_{ie} + s^2 L C_2 C_3 + s h_{ie} [C_2 C_3 + C_1 C_2 + C_1 C_3] + C_2 + C_3} \quad \ldots (8)$$

$$\therefore \quad I_b = I \times \frac{X_{C1}}{X_{C1} + h_{ie}} = \frac{I \times \frac{1}{j\omega C_1}}{\frac{1}{j\omega C_1} + h_{ie}} = \frac{I \times \frac{1}{sC_1}}{\frac{1}{sC_1} + h_{ie}}$$

$$\therefore \quad I_b = \frac{I}{(1 + s C_1 h_{ie})} \quad \ldots (9)$$

Substituting I,

$$I_b = \frac{-h_{fe} I_b C_3 (1 + s C_1 h_{ie})}{s^3 L C_1 C_2 C_3 h_{ie} + s^2 L C_2 C_3 + s h_{ie} [C_2 C_3 + C_1 C_2 + C_1 C_3] + C_2 + C_3} \times \frac{1}{(1 + s C_1 h_{ie})}$$

$$\therefore \quad 1 = \frac{-h_{fe} C_3}{s^3 L C_1 C_2 C_3 h_{ie} + s^2 L C_2 C_3 + s h_{ie} [C_1 C_2 + C_2 C_3 + C_3 C_1] + C_2 + C_3}$$

Substituting $s = j\omega$, $s^2 = j^2\omega^2 = -\omega^2$, $s^3 = -j\omega^3$

$$1 = \frac{-h_{fe} C_3}{-j\omega^3 L C_1 C_2 C_3 h_{ie} - \omega^2 L C_2 C_3 + j\omega h_{ie} [C_1 C_2 + C_2 C_3 + C_3 C_1] + C_2 + C_3}$$

$$\therefore 1 = \frac{-h_{fe} C_3}{C_2 + C_3 - \omega^2 L C_2 C_3 + j\omega h_{ie} \{[C_1 C_2 + C_2 C_3 + C_3 C_1] - \omega^2 L C_1 C_2 C_3\}} \quad \ldots (10)$$

As there is no imaginary part in numerator, to satisfy Barkhausen criterion, imaginary part in the denominator must be zero. But ω and h_{ie} are not zero hence,

$$\therefore \quad C_1C_2 + C_2C_3 + C_3C_1 - \omega^2 L C_1 C_2 C_3 = 0$$

$$\therefore \quad \omega^2 = \frac{C_1 C_2 + C_2 C_3 + C_3 C_1}{L C_1 C_2 C_3}$$

$$\therefore \quad \omega^2 = \frac{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}{L} = \frac{\frac{1}{C_{eq}}}{L}$$

$$\therefore \quad \omega^2 = \frac{1}{L C_{eq}}$$

$$\therefore \quad \boxed{\omega = \frac{1}{\sqrt{L C_{eq}}}} \quad \ldots (11)$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{L C_{eq}}}} \quad \ldots (12)$$

where $$\boxed{\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}$$

But as $C_3 << C_1$ and C_2, $C_{eq} = C_3$

$$\therefore \quad \boxed{f = \frac{1}{2\pi\sqrt{L C_3}}} \qquad \ldots (13)$$

This is the required frequency of oscillations for the Clapp oscillator.

2.11.2 Advantages

1. The frequency is stable and accurate.
2. The good frequency stability.
3. The stray capacitances have no effect on C_3 which decides the frequency.
4. Keeping C_3 variable, frequency can be varied in the desired range.

2.12 Tuned Collector Oscillator

Another type of LC oscillator is called tuned collector oscillator. A tank circuit is connected in the collector of the transistor, in which the primary of a transformer acts as an inductor L. While the voltage across the secondary of the transformer is used as a feedback voltage. The Fig. 2.48 shows the circuit of a tuned collector oscillator.

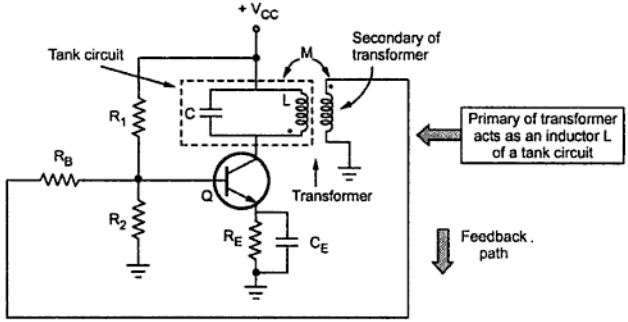


Fig. 2.48 Tuned collector oscillator

The collector of the transistor Q drives the LC resonating circuit with primary of transformer acting as L. The secondary winding is small and the feedback signal is taken from this winding, given to the base of transistor Q. The mutual inductance M exists between primary and secondary of the transformer. As indicated by the dots, transformer introduces a phase shift of 180° while 180° phase shift is introduced by the common emitter transistor Q. Thus the overall phase shift around a loop is 360°. This satisfies the Barkhausen criterion.

Ignoring the loading effect of base, the feedback fraction can be written as,

$$\therefore \quad \boxed{\beta = \text{Feedback fraction} = \frac{M}{L}}$$

For the oscillations to start, the voltage gain must be greater than the reciprocal of the feedback fraction ($1/\beta$).

$$\therefore \quad A > \frac{1}{\beta} > \frac{L}{M}$$

$$\therefore \quad \boxed{A_{min} = \frac{L}{M}}$$

The frequency of the sustained oscillations is given by,

$$\boxed{f_r = \frac{1}{2\pi\sqrt{LC}}}$$

This is decided by the primary winding inductance L and a capacitor C across it.

Key Point : *As transformer increases the size and cost and it also makes the circuit bulky hence this oscillator is rarely used in practice compared to Hartley, Colpitt and Clapp oscillators.*

By keeping tuning capacitor C variable, the frequency can be varied and also can be adjusted as per the requirement.

Example 2.14 : *A radio receiver uses a tuned collector oscillator with a fixed inductance of 30 μH while the frequency is to be varied from 300 kHz to 1.5 MHz. Find the range of tuning capacitor C over which it is to be varied.*

Solution : For a tuned collector oscillator,

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

where $L = 30\ \mu H$ and f_r to be varied 300 kHz to 1.5 MHz

$$\therefore \quad 300 \times 10^3 = \frac{1}{2\pi\sqrt{30\times10^{-6}\times C_1}} \quad \text{and} \quad 1.5 \times 10^6 = \frac{1}{2\pi\sqrt{30\times10^{-6}\times C_2}}$$

$$\therefore \quad C_1 = \mathbf{9.3816\ nF} \quad \text{and} \quad C_2 = \mathbf{375.263\ pF}$$

Hence C must be varied over 375.263 pF to 9.3816 nF, to achieve required frequency variations.

2.13 Frequency Stability of Oscillator

For an oscillator, the frequency of the oscillations must remain constant. The analysis of the dependence of the oscillating frequency on the various factors like stray capacitance, temperature etc. is called as the **frequency stability analysis.**

The measure of ability of an oscillator to maintain the desired frequency as precisely as possible for as long a time as possible is called **frequency stability** of an oscillator.

In a transistorised Colpitts oscillator or Hartley oscillator, the base-collector junction is reverse biased and there exists an internal capacitance which is dominant at high frequencies. This capacitance affects the value of capacitance in the tank circuit and hence the oscillating frequency.

Similarly the transistor parameters are temperature sensitive. Hence as temperature changes, the oscillating frequency also changes and no longer remains stable. Hence practically the circuits cannot provide stable frequency.

2.13.1 Factors Affecting the Frequency Stability

In general following are the factors which affect the frequency stability of an oscillator :

1. Due to the changes in temperature, the values of the components of tank circuit get affected. So changes in the values of inductors and capacitors due to the changes in the temperature is the main cause due to which frequency does not remain stable.
2. Due to the changes in temperature, the parameters of the active device used like BJT, FET get affected which inturn affect the frequency.
3. The variation in the power supply is another factor affecting the frequency.
4. The changes in the atmospheric conditions, aging and unstable transistor parameters affect the frequency.
5. The changes in the load connected, affect the effective resistance of the tank circuit.
6. The capacitive effect in transistor and stray capacitances, affect the capacitance of the tank circuit and hence the frequency.

The variation of frequency with temperature is given by the factor denoted as S.

$$S_{\omega,T} = \frac{\Delta\omega / \omega_r}{\Delta T / T_r} \text{ parts per million per } ^\circ C \quad \ldots (1)$$

where ω_r = Desired frequency

T_r = Operating temperature

$\Delta\omega$ = Change in frequency

ΔT = Change in temperature

The frequency stability is defined as,

$$S_{\omega} = \frac{d\theta}{d\omega} \quad \ldots (2)$$

where $d\theta$ = Phase shift introduced for a small frequency change in desired frequency f_r.

Key Point : *Larger the value of $d\theta/d\omega$, more stable is the oscillator.*

The **frequency stability can be improved** by the following modifications :

1. Enclosing the circuit in a constant temperature chamber.
2. Maintaining constant voltage by using the zener diodes.
3. The load effect is reduced by coupling the oscillator to the load loosely or with the help of a circuit having high input impedance and low output impedance.

2.14 Crystal Oscillators

The crystals are either naturally occurring or synthetically manufactured, exhibiting the **piezoelectric effect**. The piezoelectric effect means under the influence of the mechanical pressure, the voltage gets generated across the opposite faces of the crystal. If the mechanical force is applied in such a way to force the crystal to vibrate, the a.c. voltage gets generated across it. Conversely, if the crystal is subjected to a.c. voltage, it vibrates causing mechanical distortion in the crystal shape. Every crystal has its own resonating frequency depending on its cut. So under the influence of the mechanical vibrations, the crystal generates an electrical signal of very constant frequency. The crystal has a greater stability in holding the constant frequency. A crystal oscillator is basically a tuned-circuit oscillator using a piezoelectric crystal as its resonant tank circuit. The crystal oscillators are preferred when greater frequency stability is required. Hence the crystals are used in watches, communication transmitters and receivers etc.

The main substances exhibiting the piezoelectric effect are quartz, Rochelle salt and tourmaline. Rochelle salts have the greatest piezoelectric activity. For a given a.c. voltage, they vibrate more than quartz or tourmaline. Hence these are preferred in making microphones associated with portable tape recorders, headsets, loudspeakers etc. Rochelle salt is mechanically weakest of the three and break very easily. Tourmaline shows least piezoelectric effect but mechanically strongest. The tourmaline is most expensive and hence its use is rare in practice Quartz is a compromise between the piezoelectric activity of Rochelle salts and the strength of the tourmaline. **Quartz** is inexpensive and easily available in nature and hence very commonly used in the crystal oscillators.

Key Point : *Quartz is widely used for RF oscillators and the filters.*

2.14.1 Constructional Details

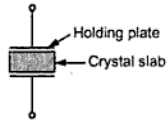


Fig. 2.49 Symbolic representation of a crystal

The natural shape of a quartz crystal is a hexagonal prism. But for its practical use, it is cut to the rectangular slab. This slab is then mounted between the two metal plates.

The symbolic representation of such a practical crystal is shown in the Fig. 2.49. The metal plates are called holding plates, as they hold the crystal slab in between them.

2.14.2 A.C. Equivalent Circuit

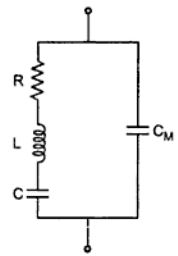


Fig. 2.50 A.C. equivalent circuit of a crystal

When the crystal is not vibrating, it is equivalent to a capacitance due to the mechanical mounting of the crystal. Such a capacitance existing due to the two metal plates separated by a dielectric like crystal slab, is called **mounting capacitance** denoted as C_M or C'.

When it is vibrating, there are internal frictional losses which are denoted by a resistance R. While the mass of the crystal, which is indication of its inertia is represented by an inductance L. In vibrating condition, it is having some stiffness, which is represented by a capacitor C. The mounting capacitance is a shunt capacitance. And hence the overall equivalent circuit of a crystal can be shown as in the Fig. 2.50.

RLC forms a resonating circuit. The expression for the resonating frequency f_r is,

$$f_r = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{Q^2}{1+Q^2}} \qquad ...(1)$$

Where

Q = quality factor of crystal

$$\therefore \quad Q = \frac{\omega L}{R} \qquad ...(2)$$

The Q factor of the crystal is very high, typically 20,000. Value of Q upto 10^6 also can be achieved. Hence $\sqrt{\frac{Q^2}{1+Q^2}}$ factor approaches to Unity and we get the resonating frequency as,

$$\boxed{f_r = \frac{1}{2\pi\sqrt{LC}}} \quad \ldots(3)$$

The crystal frequency is infact inversely proportional to the thickness of the crystal.

$$\boxed{f \propto \frac{1}{t}} \quad \text{where } t = \text{Thickness}$$

So to have very high frequencies, thickness of the crystal should be very small. But it makes the crystal mechanically weak and hence it may get damaged, under the vibrations. Hence practically crystal oscillators are used upto 200 or 300 kHz only.

The crystal has two resonating frequencies, series resonant frequency and parallel resonant frequency.

2.14.3 Series and Parallel Resonance

One resonant condition occurs when the reactances of series RLC leg are equal i.e. $X_L = X_C$. This is nothing but the series resonance. The impedance offered by this branch, under resonant condition is minimum which is resistance R. The series resonance frequency is same as the resonating frequency given by the equation (3).

$$\boxed{f_s = \frac{1}{2\pi\sqrt{LC}}} \quad \ldots (4)$$

The other resonant condition occurs when the reactances of series resonant leg equals the reactance of the mounting capacitor C_M. This is parallel resonance or antiresonance condition.

Under this condition the impedance offered by the crystal to the external circuit is maximum.

Under parallel resonance, the equivalent capacitance is,

$$C_{eq} = \frac{C_M C}{C_M + C} \quad \ldots (5)$$

Hence the parallel resonating frequency is given by,

$$\boxed{f_p = \frac{1}{2\pi\sqrt{LC_{eq}}}} \quad \ldots (6)$$

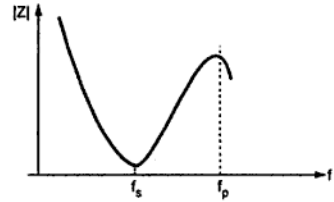


Fig. 2.51 (a) Crystal impedance versus frequency

When the crystal capacitance C is much smaller than C_M, then the Fig. 2.51(a) shows the behaviour of crystal impedance versus frequency.

Generally values of f_s and f_p are very close to each other and practically it can be said that there exists only one resonating frequency for a crystal.

The higher value of Q is the main advantage of crystal. Due to high Q of a resonant circuit, it provides very good frequency stability.

If we neglect the resistance R, the impedance of the crystal is a reactance jX which depends on the frequency as,

$$jX = -\frac{j}{\omega C_M} \cdot \frac{\omega^2 - \omega_s^2}{\omega^2 - \omega_p^2}$$

where ω_s = Series resonant frequency

ω_p = Parallel resonant frequency

The sketch of reactance against frequency is shown in the Fig. 2.51 (b).

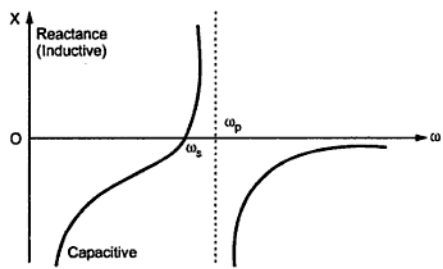


Fig. 2.51 (b) The reactance versus frequency

The oscillating frequency lies between ω_s and ω_p.

2.14.4 Crystal Stability

The frequency of the crystal tends to change slightly with time due to temperature, aging etc.

i) Temperature stability : It is defined as the change in the frequency per degree change in the temperature. This is Hz/MHz/°C. For 1°C change in the temperature, the frequency changes by 10 to 12 Hz in MHz. This is negligibly small. So for all practical purposes it is treated to be constant. But if this much change is also not acceptable then the crystal is kept in box where temperature is maintained constant, called constant temperature oven or constant temperature box.

ii) Long term stability : It is basically due to aging of the crystal material. Aging rates are 2×10^{-8} per year, for a quartz crystal. This is also negligibly small.

iii) Short term stability : In a quartz crystal, the frequency drift with time is, typically less than 1 part in 10^6 i.e. 0.0001 % per day. This is also very small.

Key Point : *Overall crystal has good frequency stability. Hence it is used in computers, counters, basic timing devices in electronic wrist watches, etc.*

2.14.5 Pierce Crystal Oscillator

The **Colpitts** oscillator can be modified by using the crystal to behave as an inductor. The circuit is called Pierce crystal oscillator. The crystal behaves as an inductor for a frequency slightly higher than the series resonance frequency f_s. The two capacitors C_1, C_2 required in the tank circuit along with an inductor are used, as they are used in **Colpitts** oscillator circuit. As only inductor gets replaced by the crystal, which behaves as an inductor, the basic working principle of Pierce Crystal Oscillator is same as that of **Colpitts** oscillator. The practical transistorised pierce crystal oscillator circuit is shown in the Fig. 2.52.

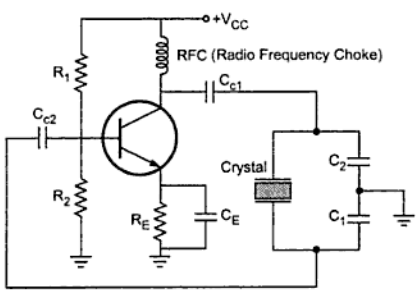
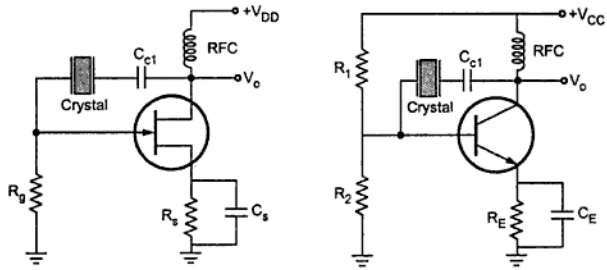


Fig. 2.52 Pierce crystal oscillator

The resistances R_1, R_2, R_E provide d.c. bias while the capacitor C_E is emitter bypass capacitor. RFC (Radio Frequency Choke) provides isolation between a.c. and d.c. operation. C_{c1} and C_{c2} are coupling capacitors.

The resulting circuit frequency is set by the series resonant frequency of the crystal, change in the supply voltages, temperature, transistor parameters have no effect on the circuit operating conditions and hence good frequency stability is obtained.

The oscillator circuit can be modified by using the internal capacitors of the transistor used instead of C_1 and C_2. The separate capacitors C_1, C_2 are not required in such circuit. Such circuits using FET and transistor are shown in the Fig. 2.53 (a) and (b).



(a) Using FET **(b) Using transistor**

Fig. 2.53 Pierce crystal oscillator

2.14.6 Miller Crystal Oscillator

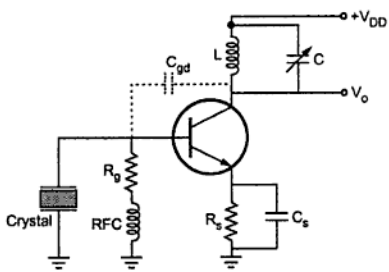


Fig. 2.54 Miller crystal oscillator

Similar to the modifications in Colpitts oscillator, the Hartley oscillator circuit can be modified, to get Miller crystal oscillator. In Hartley oscillator circuit, two inductors and one capacitor is required in the tank circuit. One inductor is replaced by the crystal which acts as an inductor for the frequencies slightly greater than the series resonant frequency. The transistorised Miller crystal oscillator circuit is shown in the Fig. 2.54.

The tuned circuit of L_1 and C is offtuned to behave as an inductor i.e. L_1. The crystal behaves as other inductance L_2 between base and ground. The internal capacitance of the

transistor acts as a capacitor required to fulfill the elements of the tank circuit. The crystal decides the operating frequency of the oscillator.

Example 2.15 : *A crystal L = 0.4 H, C = 0.085 pF and C_M = 1 pF with R = 5 kΩ. Find*

i) Series resonant frequency

ii) Parallel resonant frequency

iii) By what percent does the parallel resonant frequency exceed the series resonant frequency ?

iv) Find the Q factor of the crystal.

Solution : i) $$f_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.4\times0.085\times10^{-12}}}$$

$$= \mathbf{0.856\ MHz}$$

ii) $$C_{eq} = \frac{CC_M}{C+C_M} = \frac{0.085\times1}{0.085+1} = 0.078\ \text{pF}$$

$$\therefore \quad f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.4\times0.078\times10^{-12}}}$$

$$= \mathbf{0.899\ MHz}$$

iii) $$\%\ \text{increase} = \frac{0.899-0.856}{0.856}\times100 = \mathbf{5.023\%}$$

iv) $$Q = \frac{\omega_s L}{R} = \frac{2\pi f_s L}{R} = \frac{2\pi\times0.856\times10^6\times0.4}{5\times10^3}$$

$$= \mathbf{430.272}$$

Example 2.16 : *A crystal has L = 2 H, C = 0.01 pF and R = 2 kΩ. Its mounting capacitance is 2 pF. Calculate it series and parallel resonating frequency.*

Solution : $C_M = 2$ pF

Now $$f_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{\sqrt{2\times0.01\times10^{-12}}}$$

$$= \mathbf{1.125\ MHz}$$

$$C_{eq} = \frac{C_M C}{C_M + C} = \frac{2\times10^{-12}\times0.01\times10^{-12}}{2\times10^{-12}+0.01\times10^{-12}} = 9.95\times10^{-15}\ \text{F}$$

$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{\sqrt{2\times 9.95\times 10^{-15}}}$$

$$= 1.128 \text{ MHz}$$

So f_s and f_p values are almost same.

2.15 Amplitude Stabilization

The oscillator output amplitude if not stabilized, attains the extreme levels of saturation i.e. $\pm V_{sat}$. But this can cause the distortion in the output waveform. Hence it is necessary to minimize the distortion and reduce the output amplitude within the acceptable range. The circuit used in the oscillator for this purpose is called **oscillator amplitude stabilization circuit**. It makes the oscillations damped and ensures that are not sustained if amplitude increases beyond a particular value.

The amplitude stabilization circuit used for the phase shift oscillator is shown in the Fig. 2.55(a).

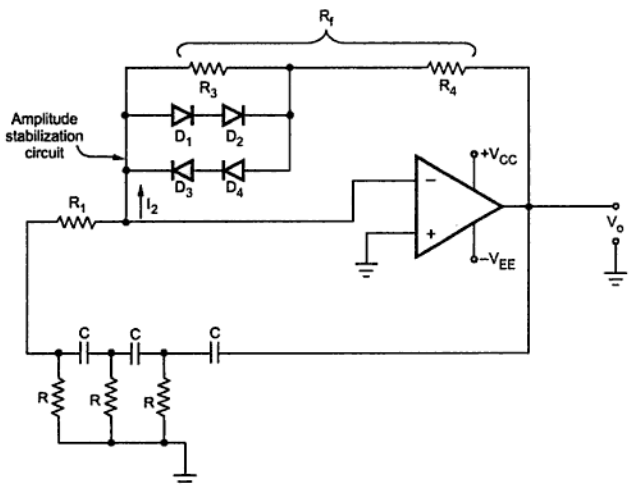


Fig. 2.55 (a) Amplitude stabilization of phase shift oscillator

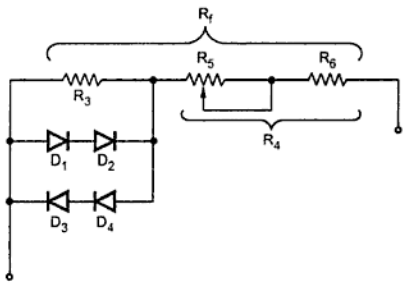


Fig. 2.55 (b) Use of adjustable resistors

When output amplitude exceeds some acceptable level, it makes the diodes D_3 and D_4 forward biased. Thus resistance R_3 gets shorted. Thus the gain of the inverting amplifier becomes $A_{CL} = -\frac{R_4}{R_1}$. The R_4 is so designed that this gain is not enough to sustain the oscillations of high amplitude.

The resistance R_4 can be made up of one fixed resistance R_6 and other variable resistance R_5 for variable adjustment of R_4, to overcome distortion. This is shown in the Fig. 2.55 (b).

The output of the oscillator can also be controlled as per the requirement, by connecting back to back zener diodes of appropriate ratings at the output.

Examples with Solutions

Example 2.17 : *For phase shift oscillator, the feedback network uses R = 6 kΩ and C = 1500 pF. The transistorised amplifier used, has a collector resistance of 18 kΩ. Calculate the frequency of oscillations and minimum value of h_{fe} of the transistor.*

Solution : R = 6 kΩ, C = 1500 pF, R_C = 18 kΩ

Now $$K = \frac{R_C}{R} = \frac{18}{6} = 3$$

$$\therefore \quad f = \frac{1}{2\pi RC\sqrt{6+4K}} = \frac{1}{2\pi \times 6\times 10^{3}\times 1500\times 10^{-12}\sqrt{6+12}}$$

$$= \mathbf{4.168\ kHz}$$

$$(h_{fe})_{min} = 4K + 23 + \frac{29}{K} = 4 \times 3 + 23 + \frac{29}{3}$$

$$= \mathbf{44.67}$$

Example 2.18 : *Find the resistance R and h_{fe} for the transistor to provide a resonating frequency of 5 kHz of a transistorised phase shift oscillator. The biasing resistance are 25 kΩ and 47 kΩ. The load resistance is 10 kΩ. The capacitor in the tank circuit is 1000 pF while h_{ie} of the transistor is 2 kΩ.*

Solution : Referring to equation (1 of section 2.5.3), the input impedance is given by,

$$R_i' = R_1 \parallel R_2 \parallel h_{ie}$$

Now $R_1 = 25\ k\Omega$, $R_2 = 47\ k\Omega$, and $h_{ie} = 2\ k\Omega$

$$\therefore \quad R_i' = \frac{1}{\frac{1}{25\times10^3}+\frac{1}{47\times10^3}+\frac{1}{2\times10^3}}$$

$$= 1.7816\ k\Omega$$

$$K = \frac{R_C}{R}$$

Now $R_C = 10\ k\Omega$

Now $$f = \frac{1}{2\pi RC\sqrt{6+4K}}$$

$$\therefore \quad 5\times10^3 = \frac{1}{2\pi R\times1000\times10^{-12}\times\sqrt{6+4K}}$$

$$\therefore \quad R\sqrt{6+4K} = 31830.989$$

Now $$K = \frac{R_C}{R} = \frac{10\times10^3}{R}$$

$$\therefore \quad R\sqrt{6+\frac{4\times10\times10^3}{R}} = 31830.989$$

$$\therefore \quad R^2\left(6+\frac{40\times10^3}{R}\right) = (31830.989)^2$$

$$\therefore \quad R^2\,\frac{[6R+40\times10^3]}{R} = (31830.989)^2$$

$$6R^2 + 40\times10^3R - (31830.989)^2 = 0$$

$$\therefore \quad R = \frac{-40\times10^3 \pm\sqrt{(40\times10^3)^2+4\times6\times(31830.989)^2}}{2\times6}$$

$$= \mathbf{16.74\ k\Omega} \qquad \text{Neglecting negative value}$$

$$\therefore \quad K = \frac{R_C}{R} = \frac{10}{16.74} = 0.5973$$

$$\therefore \quad h_{fe} \geq 4K + 23 + \frac{29}{K}$$

$$\geq 4\times0.5973 + 23 + \frac{29}{0.5973} \geq \mathbf{73.94}$$

Example 2.19 : *A quartz crystal has the following constants, L = 50 mH, C_1 = 0.02 pF, R = 500 Ω and C_2 = 12 pF. Find the values of f_s and f_p. If the external capacitance across the crystal changes from 5 pF to 6 pF, find the change in frequency of oscillations.*

Solution : L = 50 mH, C_1 = 0.02 pF, R = 500 Ω, C_2 = 12 pF

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{0.02\times12\times10^{-12}\times10^{-12}}{[0.02+12]\times10^{-12}}$$

$$= 0.01996 \text{ pF}$$

$$\therefore \quad f_s = \frac{1}{2\pi\sqrt{L C_1}} = \frac{1}{2\pi\sqrt{50\times10^{-3}\times0.02\times10^{-12}}}$$

$$= \mathbf{5.0329 \text{ MHz}}$$

and

$$f_p = \frac{1}{2\pi\sqrt{L C_{eq}}} = \frac{1}{2\pi\sqrt{50\times10^{-3}\times0.01996\times10^{-12}}}$$

$$= \mathbf{5.0379 \text{ MHz}}$$

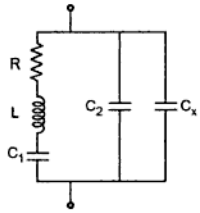


Fig. 2.56

Let C_s = 5 pF connected across the crystal.

$$\therefore \quad C_2' = C_2 + C_x$$

$$= 12 + 5$$

$$= 17 \text{ pF}$$

$$\therefore \quad C_{eq}' = \frac{C_1 C_2'}{C_1 + C_2'}$$

$$= 0.019976 \text{ pF}$$

$$\therefore \quad f_p' = \frac{1}{2\pi\sqrt{L C_{eq}'}}$$

$$= 5.03588 \text{ MHz}$$

New C_x = 6 pF is connected then,

$$C_2'' = C_2 + C_x = 12 + 6$$

$$= 18 \text{ pF}$$

$$\therefore \quad C_{eq}'' = \frac{C_1 C_2''}{C_1 + C_2''} = 0.0199778 \text{ pF}$$

$$\therefore \quad f_p'' = \frac{1}{2\pi\sqrt{L C_{eq}''}} = 5.035716 \text{ MHz}$$

$$\therefore \quad \text{Change} = f_p' - f_p'' = (5.03588 - 5.035716) \times 10^6$$

$$= \mathbf{164\ Hz}$$

Example 2.20 : *Find C and h_{fe} of a transistor to provide f_o of 50 kHz of a RC transistorised phase shift oscillator. Given : $R_1 = 22\ k\Omega$, $R_2 = 68\ k\Omega$, $R_C = 20\ k\Omega$, $R = 6.8\ k\Omega$*

Solution :

$$R_i' = R_1 \parallel R_2 \parallel h_{ie} = 22\ k\Omega \parallel 68\ k\Omega \parallel 2\ k\Omega = 1.8243\ k\Omega$$

Now $R_i' + R_3 = R$

$$\therefore \quad R_3 = R - R_i' = 6.8 - 1.8243 = 4.9757\ k\Omega$$

$$K = \frac{R_C}{R} = \frac{20}{6.8} = 2.9411$$

$$\therefore \quad f = \frac{1}{2\pi RC\sqrt{6+4K}}$$

$$\therefore \quad 50 \times 10^3 = \frac{1}{2\pi \times 6.8 \times 10^3 \times C \times \sqrt{6+4\times 2.9411}}$$

$$\therefore \quad C = \mathbf{111.062\ pF}$$

And $$h_{fe} \geq 4K + 23 + \frac{29}{K} \geq 4 \times 2.9411 + 23 + \frac{29}{2.9411}$$

$$\therefore \quad h_{fe} \geq \mathbf{44.6246}$$

Example 2.21 : *The frequency sensitive arms of the Wien bridge oscillator uses $C_1 = C_2 = 0.001\ \mu F$ and $R_1 = 10\ k\Omega$ while R_2 is kept variable. The frequency is to be varied from 20 kHz to 70 kHz by varying R_2. Find the minimum and maximum values of R_2.*

Solution : The frequency of the oscillator is given by,

$$f = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

For $f = 20$ kHz,

$$20 \times 10^3 = \frac{1}{2\pi\sqrt{10\times 10^3 \times R_2 \times (0.001\times 10^{-6})^2}}$$

$$\therefore \quad R_2 = \mathbf{6.33\ k\Omega}$$

For $f = 70$ kHz

$$70 \times 10^3 = \frac{1}{2\pi\sqrt{10\times 10^3 \times R_2 \times (0.001\times 10^{-6})^2}}$$

$\therefore \quad R_2 = 0.516\ k\Omega$

So minimum value of R_2 is 0.516 kΩ while the maximum value of R_2 is 6.33 kΩ.

Example 2.22 : *In a Hartley oscillator, L_1 = 15 mH and C = 50 pF. Calculate L_2 for a frequency of 168 kHz. The mutual inductance between L_1 and L_2 is 5 μH. Also find the required gain of the transistor to be used for the oscillations.*

Solution : For a Hartley oscillator,

$$f = \frac{1}{2\pi\sqrt{L_{eq}\,C}} \qquad \text{where } L_{eq} = L_1 + L_2 + 2M$$

$$\therefore \quad 168\times10^{3} = \frac{1}{2\pi\sqrt{L_{eq}\times50\times10^{-12}}}$$

$$\therefore \quad L_{eq} = 17.95\ mH$$

$$\therefore \quad 17.95\times10^{-3} = 15\times10^{-3} + L_2 + 5\times10^{-6}$$

$$\therefore \quad L_2 = \mathbf{2.945\ mH}$$

Now $$h_{fe} = \frac{L_1 + M}{L_2 + M}$$

$$= \frac{15\times10^{-3} + 5\times10^{-6}}{2.945\times10^{-3} + 5\times10^{-6}}$$

$$= \mathbf{5.08}$$

Example 2.23 : *A two stage FET oscillator uses the phase shifting network shown in the Fig. 2.57.*

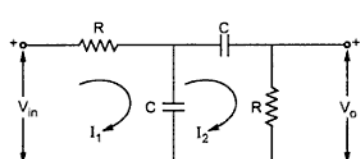


Fig. 2.57

Show that the frequency of oscillations is $f = \frac{1}{2\pi RC}$ and the gain of the amplifier stage must exceed 3.

Solution : Let the two loop currents be I_1 and I_2. Applying KVL to the two loops, we get,

$$V_{in} = I_1 R + I_1 \times \frac{1}{j\omega C} - I_2 \times \frac{1}{j\omega C} \quad \ldots (i)$$

$$0 = I_2 R + I_2 \times \frac{1}{j\omega C} - I_1 \times \frac{1}{j\omega C} + I_2 \times \frac{1}{j\omega C} \quad \ldots (ii)$$

Replacing $j\omega = s$ and writing in the matrix form,

$$\begin{bmatrix} R+\frac{1}{sC} & -\frac{1}{sC} \\ -\frac{1}{sC} & R+\frac{2}{sC} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V_{in} \\ o \end{bmatrix}$$

Using Cramer's rule, to solve for I_2,

$$D = \begin{vmatrix} R+\frac{1}{sC} & -\frac{1}{sC} \\ -\frac{1}{sC} & R+\frac{2}{sC} \end{vmatrix} = \left(R+\frac{1}{sC}\right)\left(R+\frac{2}{sC}\right) - \frac{1}{s^2C^2}$$

$$= \frac{(1+sRC)(2+sRC)}{s^2C^2} - \frac{1}{s^2C^2}$$

$$= \frac{2+3sRC+s^2R^2C^2-1}{s^2C^2} = \frac{1+3sRC+s^2R^2C^2}{s^2C^2}$$

$$D_2 = \begin{vmatrix} R+\frac{1}{sC} & V_{in} \\ -\frac{1}{sC} & 0 \end{vmatrix} = +\frac{V_{in}}{sC}$$

$$\therefore \quad I_2 = \frac{D_2}{D} = \frac{V_{in} s^2C^2}{sC[1+3sRC+s^2R^2C^2]} = \frac{V_{in} sC}{1+3sRC+s^2R^2C^2}$$

Now

$$V_o = I_2 R = \frac{V_{in} sRC}{1+3sRC+s^2R^2C^2}$$

$$\therefore \quad \beta = \frac{V_o}{V_{in}} = \frac{sRC}{1+3sRC+s^2R^2C^2}$$

Replacing s by $j\omega$, s^2 by $-\omega^2$,

$$\beta = \frac{j\omega RC}{1-\omega^2R^2C^2+3j\omega RC}$$

Retionalising the expression for β,

$$\beta = \frac{j\omega RC[(1-\omega^2R^2C^2)-3j\omega RC]}{(1-\omega^2R^2C^2)^2+9\omega^2R^2C^2}$$

$$= \frac{3\omega^2 R^2 C^2 + j\omega RC(1-\omega^2 R^2 C^2)}{(1-\omega^2 R^2 C^2)^2 + 9\omega^2 R^2 C^2}$$

As amplifier is two stage, it gives 360° phase shift hence phase shift of $\beta = 0°$ hence the imaginary part of β must be 0.

$$\therefore \quad \omega RC\,(1 - \omega^2 R^2 C^2) = 0$$

$$\therefore \quad 1 - \omega^2 R^2 C^2 = 0 \text{ neglecting zero value}$$

$$\therefore \quad \omega^2 = \frac{1}{R^2 C^2}$$

$$\therefore \quad \omega = \frac{1}{RC}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi RC}}$$

Now at this frequency, the magnitude of β,

$$\beta = \frac{3 \times \frac{1}{R^2C^2} \times R^2C^2}{0 + 9 \times \frac{1}{R^2C^2} \times R^2C^2}$$

$$= \frac{3}{9} = \frac{1}{3}$$

Now let A be the effecitve gain of the amplifier stage

$$\therefore \quad |A\beta| \geq 1$$

$$\therefore \quad |A| \geq \frac{1}{|\beta|} \geq \frac{1}{\frac{1}{3}}$$

$$\therefore \quad \boxed{|A| \geq 3}$$

So gain must exceed 3, for the oscillations.

Example 2.24 : *A FET Hartley oscillator circuit uses coupled coils in the tank circuit, each with inductance of 0.1 mH and mutual inductance of 0.025 mH. The circuit uses a fixed capacitor of 100 pF in series with a variable capacitor of 100 pF (trimmer) :*

(i) Calculate % change in frequency when direction of coupling between coils is reversed, trimmer capacitance set to zero.

(ii) Repeat calculations in part (i) when trimmer capacitance is changed from 0 to 100 pF, assume any one direction of coupling.

Solution : $L_1 = 0.1$ mH, $L_2 = 0.1$ mH, $M = 0.025$ mH, $C = 100$ pF

(i) Assume one particular coupling direction for which,

$$L_{eq} = L_1 + L_2 + 2M = 0.25 \text{ mH}$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{L_{eq}\, C}} = \frac{1}{2\pi\sqrt{0.25\times10^{-3}\times100\times10^{-12}}}$$

$$= 1.00658 \text{ MHz}$$

Let the direction of coupling is reversed,

$$L_{eq} = L_1 + L_2 - 2M = 0.15 \text{ mH}$$

$$\therefore \quad f' = \frac{1}{2\pi\sqrt{L_{eq}\, C}} = \frac{1}{2\pi\sqrt{0.15\times10^{-3}\times100\times10^{-12}}} = 1.2994 \text{ MHz}$$

$$\therefore \quad \% \text{ change} = \frac{f'-f}{f}\times 100 = \frac{1.2994-1.00658}{1.00658}\times100 = \mathbf{29.09\%}$$

(ii) Let us assume direction of coupling such that,

$$L_{eq} = L_1 + L_2 + 2M = 0.25 \text{ mH}$$

$$C_t = \text{Trim capacitor} = 100 \text{ pF}$$

$$\therefore \quad C_{eq} = \frac{C\times C_t}{C+C_t} = 50 \text{ pF}$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{L_{eq}\, C_{eq}}} = \frac{1}{2\pi\sqrt{0.25\times10^{-3}\times50\times10^{-12}}}$$

$$= 1.4235 \text{ MHz}$$

If now direction of coupling is reversed,

$$L_{eq} = L_1 + L_2 - 2M = 0.15 \text{ mH}$$

$$\therefore \quad f' = \frac{1}{2\pi\sqrt{L_{eq}\, C_{eq}}} = \frac{1}{2\pi\sqrt{0.15\times10^{-3}\times50\times10^{-12}}}$$

$$= 1.83776 \text{ MHz}$$

$$\therefore \quad \% \text{ change} = \frac{f'-f}{f}\times 100 = \frac{1.83776-1.4235}{1.4235}\times100$$

$$= \mathbf{29.101\ \%}$$

Example 2.25 : *Design a RC phase shift oscillator to generate 5 kHz sine wave with 20 V peak to peak amplitude. Draw the designed circuit. Assume h_{fe} = 150.* **(May-2006)**

Solution : For RC phase shift oscillator,

$$h_{fe} = 4K + 23 + \frac{29}{K} \quad \text{... given } h_{fe} = 150$$

$$\therefore \quad 150 = 4K + 23 + \frac{29}{K}$$

$$\therefore \quad 4K^2 - 127\,K + 29 = 0$$

$$\therefore \quad K = 31.52 \text{ , } 0.23$$

$$f = \frac{1}{2\pi R C\sqrt{6+4K}} \quad \text{... given } f = 5 \text{ kHz}$$

$$\therefore \text{Choose} \quad C = 1000 \text{ pF}$$

$$\therefore \quad 5\times10^{3} = \frac{1}{2\pi R\times1000\times10^{-12}\times\sqrt{6+4\times0.23}}$$

$$\therefore \quad R = 12.1 \text{ k}\Omega \approx \mathbf{12\ k\Omega}$$

$$K = \frac{R_C}{R} \quad \text{i.e. } R_C = KR = \mathbf{2.7\ k\Omega}$$

Neglecting effect of biasing resistances assuming them to be large and selecting transistor with h_{ie} = 2 kΩ ,

$$R_i' = h_{ie} = 2 \text{ k}\Omega$$

∴ Last resistance in phase shift network

$$R_3 = R - R_i' = 12 - 2 = \mathbf{10\ k\Omega}$$

Using the back to back connected zener diodes of 9.3 V (Vz) each at the output of emitter follower and using this at the output of the oscillator, the output amplitude can be controlled to 10 V i.e. 20 V peak to peak.

Key Point : *The zener diode 9.3 V and forward biased diode of 0.7 V gives total 10 V.*

The designed circuit is as shown in the Fig. 2.58.

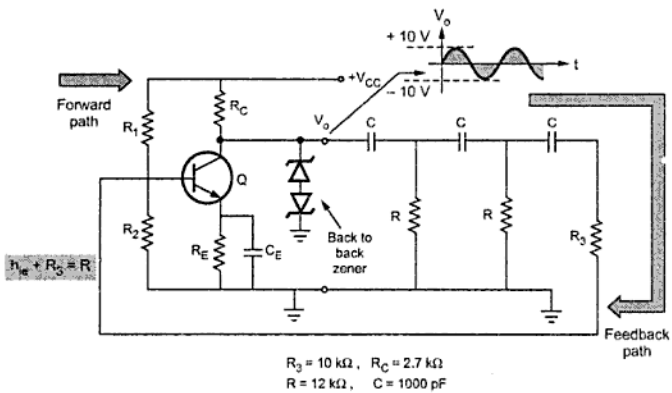


Fig. 2.58 Transistorised RC phase shift oscillator

Example 2.26 : *In a Colpitts oscillator, the values of the inductors and capacitors in the tank circuit are L = 40 mH, C_1 = 100 pF and C_2 = 500 pF.*

1) Find the frequency of oscillation.

2) If the output voltage is 10 V, find the feedback voltage.

3) Find the minimum gain, if the frequency is changed by changing 'L' alone.

4) Find the value of C_1 for a gain of 10.

5) Also, find the new frequency of oscillation.

Solution :

1) $$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

Where $$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{100\times10^{-12}\times500\times10^{-12}}{100\times10^{-12}+500\times10^{-12}} = 83.333\times10^{-12}\ \text{F}$$

$\therefore$ $$f = \frac{1}{2\pi\sqrt{40\times10^{-3}\times83.333\times10^{-12}}} = \mathbf{87.1727\ kHz}$$

2) The input voltage is not required for the oscillator. The feedback voltage, which is the part of the output voltage is enough to drive the oscillator.

$$V_o = 10\ \text{V}$$

For Colpitt's oscillator, gain = $\frac{C_2}{C_1}$

$\therefore$ Gain = $\frac{500}{100} = 5$

$\therefore$ Feedback voltage = $\frac{V_o}{\text{Gain}} = \frac{10}{5} = 2$ V

3) Minimum gain = $\frac{C_2}{C_1} = 5$

$h_{fe(min)} = \frac{C_2}{C_1} = 5$

4) Gain = $10 = \frac{C_2}{C_1}$

$\therefore$ $10 = \frac{500 \text{ pF}}{C_1}$

$\therefore$ $C_1 = 50$ pF

5) For $C_1 = 50$ pF and $C_2 = 500$ pF

$$C_{eq} = \frac{50\times10^{-12}\times500\times10^{-12}}{50\times10^{-12}+500\times10^{-12}} = 45.4545 \text{ pF}$$

$\therefore$ $$f = \frac{1}{2\pi\sqrt{L\,C_{eq}}} = \frac{1}{2\pi\sqrt{40\times10^{-3}\times45.4545\times10^{-12}}}$$

= **118.032 kHz** ...New frequency

Example 2.27 : *Design the Colpitts oscillator to get the frequency of 1 MHz with FET having* $\mu = 20$.

Solution : The frequency required is, $f = 1$ MHz and for FET, $\mu = 20$

Now $\mu = \frac{C_2}{C_1}$ for oscillations

$\therefore$ $20 = \frac{C_2}{C_1}$

$\therefore$ $C_2 = 20\,C_1$ ... (1)

Let $C_1 = 0.01\,\mu$F hence $C_2 = 0.2\,\mu$F

$\therefore$ $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$

$$= \frac{0.01\times10^{-6}\times0.2\times10^{-6}}{(0.01\times10^{-6}+0.2\times10^{-6})}$$

$$= 9.5238\times10^{-9}\ \text{F}$$

Now $$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$\therefore \quad 1\times10^{6} = \frac{1}{2\pi\sqrt{L\times9.5238\times10^{-9}}}$$

$$\therefore \quad L = 2.66\ \mu\text{H}$$

The biasing resistances can be selected as,

$$R_1 = 12\ \text{M}\Omega \quad \text{and} \quad R_2 = 8\ \text{M}\Omega$$

These resistances must be large.

The designed circuit is shown in the Fig. 2.59.

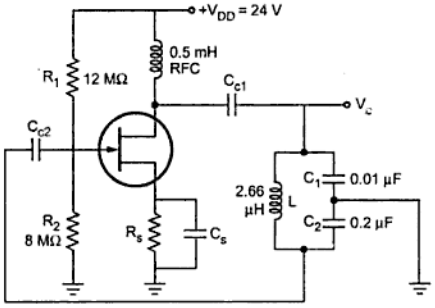


Fig. 2.59

Example 2.28 : *A Hartley oscillator having the following parameters, L_1 = 500 μH, L_2 = 5000 μH, M = 300 μH, C = 150 pF. Find the frequency of oscillations.* **(R.U. : 2006)**

Solution : $L_{eq} = L_1 + L_2 + 2M = [500 + 5000 + 2 \times 300]\ \mu\text{H} = 6100\ \mu\text{H}$

$$f = \frac{1}{2\pi\sqrt{C\,L_{eq}}} = \frac{1}{2\pi\sqrt{150\times10^{-12}\times6100\times10^{-6}}}$$

$$= \mathbf{166.3832\ kHz}$$

Example 2.29 : *The parameters of a crystal oscillator equivalent circuit are L_s = 0.8 H, C_s = 0.08 pF, R_s = 5 k Ω and C_M = 1 pF. Determine the resonating frequencies f_s and f_p.*

(R.U. : 2005)

Solution : $L_s = 0.8$ H, $C_s = 0.08$ pF, $R_s = 5$ kΩ, $C_M = 1$ pF

$$f_s = \frac{1}{2\pi\sqrt{L_s C_s}} = \frac{1}{2\pi\sqrt{0.8\times0.08\times10^{-12}}} = \mathbf{629.1151\ kHz}$$

$$C_{eq} = \frac{C_M C_s}{C_M + C_s} = \frac{1\times10^{-12}\times0.08\times10^{-12}}{(1+0.08)\times10^{-12}} = 7.4074 \times 10^{-14}\ \text{F}$$

$$\therefore \quad f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.8\times7.4074\times10^{-14}}} = \mathbf{653.7956\ kHz}$$

Example 2.30 : *Prove that the ratio of the parallel to series resonant frequencies of crystal is approximately given by,*

$\frac{f_p}{f_s} \cong \left(1 + \frac{C}{2C_M}\right)$ *where C_M = Mounting capacitance.*

(R.U. : 2004)

Solution : For a crystal,

$$f_s = \frac{1}{2\pi\sqrt{LC}} \quad \text{while} \quad f_p = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$\therefore \quad \frac{f_p}{f_s} = \frac{1}{2\pi\sqrt{LC_{eq}}} \times \frac{2\pi\sqrt{LC}}{1} = \sqrt{\frac{C}{C_{eq}}} \quad \text{but } C_{eq} = \frac{CC_M}{C+C_M}$$

$$\therefore \quad \frac{f_p}{f_s} = \sqrt{\frac{C}{\frac{CC_M}{C+C_M}}} = \sqrt{\frac{C(C+C_M)}{CC_M}} = \sqrt{1+\frac{C}{C_M}} = \left(1+\frac{C}{C_M}\right)^{1/2}$$

$(1 + x)^n = 1 + n x + \ldots$ ...Mathematical series

$$\therefore \quad \boxed{\frac{f_p}{f_s} \cong 1 + \frac{1}{2}\times\frac{C}{C_M}} \quad \text{(Neglecting higher order terms)} \quad \text{... Proved}$$

Example 2.31 : *If C = 0.04 pF and C_M = 2 pF then by what percent does the parallel resonant frequency exceed the series resonant frequency ?* **(R.U. : 2003)**

Solution : The series and parallel resonating frequencies are,

$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} \quad \text{and} \quad f_s = \frac{1}{2\pi\sqrt{LC}}$$

$$\therefore \quad \frac{f_p}{f_s} = \frac{1}{2\pi\sqrt{LC_{eq}}} \times 2\pi\sqrt{LC} = \sqrt{\frac{C}{C_{eq}}} \quad \text{where } C_{eq} = \frac{CC_M}{C+C_M}$$

$$\therefore \quad \frac{f_p}{f_s} = \sqrt{\frac{C}{\frac{CC_M}{C+C_M}}} = \sqrt{\frac{C(C+C_M)}{CC_M}} = \sqrt{1+\frac{C}{C_M}}$$

$$= \sqrt{1+\frac{0.04}{2}} = 1.00995$$

$$f_p = 1.00995\ f_s$$

$$\therefore \quad \% \text{ increase} = \frac{1.00995\ f_s - f_s}{f_s} \times 100 = \mathbf{0.995\ \%}$$

Example 2.32 : *Calculate the operating frequency and the feedback fraction for the oscillator as shown in the Fig. 2.60 and the mutual inductance of the coils is 20 μH.*

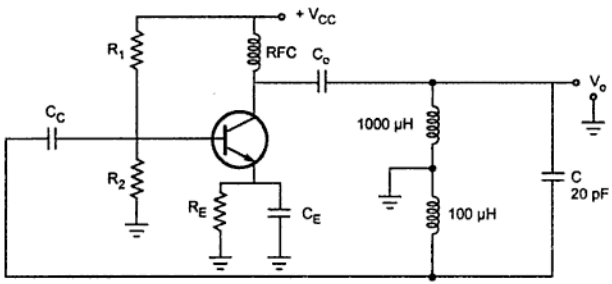


Fig. 2.60

Also mention the name of the oscillator.

Solution : C = 20 pF, L_2 = 1000 μH, L_1 = 100 μH, M = 20 μH

$$\therefore \quad L_{eq} = L_1 + L_2 + 2M = [100 + 1000 + 2 \times 20] = 1140\ \mu H$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{L_{eq}C}} = \frac{1}{2\pi\sqrt{1140\times10^{-6}\times20\times10^{-12}}} = \mathbf{1.054\ MHz}$$

The feedback fraction β is given by,

$$\beta = \frac{V_f}{V_o} = \frac{X_{L1}}{X_{L1}+X_{L2}} = \frac{L_1}{L_1+L_2} = \frac{100\times10^{-6}}{(100+1000)\times10^{-6}} = \mathbf{0.0909}$$

It is a Hartley oscillator.

Example 2.33 : *It is desired to design phase shift oscillator using FET having $g_m = 5000\ \mu S$, $r_d = 40\ k\Omega$ and feedback circuit value of $R = 10\ k\Omega$. Select the value of C and R_D to have the frequency of operation as 1 kHz and $A > 29$.* **(R.U. : 1995)**

Solution : Using the expression of the frequency,

$$f = \frac{1}{2\pi RC\sqrt{6}} \quad \text{i.e.} \quad 1 \times 10^3 = \frac{1}{2\pi \times 10 \times 10^3 \times C \times \sqrt{6}}$$

$$\therefore \quad C = \mathbf{6.4974\ nF}$$

For FET phase shift oscillator,

$$|A| = g_m R_L \quad \text{and} \quad |A| \geq 29$$

$$\therefore \quad g_m R_L \geq 29 \quad \text{i.e.} \quad R_L \geq \frac{29}{5000 \times 10^{-6}} \geq 5.8\ k\Omega$$

With $R_L = 5.8\ k\Omega$, $\quad R_L = \dfrac{R_D r_d}{R_D + r_d}$ i.e. $5.8 \times 10^3 = \dfrac{R_D \times 40 \times 10^3}{R_D + 40 \times 10^3}$

$$\therefore \quad R_D + 40 \times 10^3 = 6.8965\ R_D \quad \text{i.e.} \quad 5.8965\ R_D = 40 \times 10^3$$

$$\therefore \quad R_D = \mathbf{6.7836\ k\Omega}$$

Example 2.34 : *What is name of following oscillator, explain its working and calculate the value of inductance (L) offered by the crystal at oscillation frequency $f_s = 1$ MHz.*

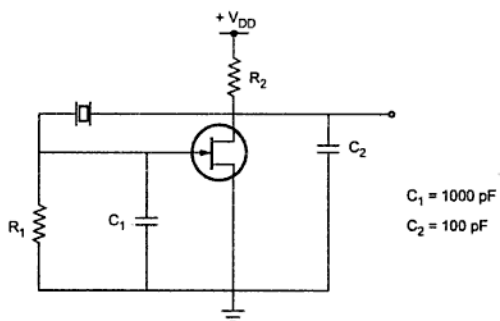


Fig. 2.61

If crystal has bulk resistance $R_s = 700\ \Omega$ then draw its electrical equivalent circuit with component values. **(R.U. : May - 2008)**

Solution : The name of the oscillator is Pierce oscillator

$$C_1 = 1000 \text{ pF}, \quad C_2 = 100 \text{ pF}, \quad f_s = 1 \text{ MHz}$$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} = \frac{1000 \times 100 \times 10^{-24}}{[1000 + 100] \times 10^{-12}} = 90.909 \times 10^{-12} \text{ F}$$

At resonance, $X_L = X_{Ceq}$ i.e. $2\pi fL = \frac{1}{2\pi f C_{eq}}$

$$\therefore \quad L = \frac{1}{(2\pi f)^2 C_{eq}} = \frac{1}{(2\pi \times 1 \times 10^6)^2 \times 90.909 \times 10^{-12}}$$

$$= \mathbf{0.27863 \text{ mH} = 279 \ \mu H}$$

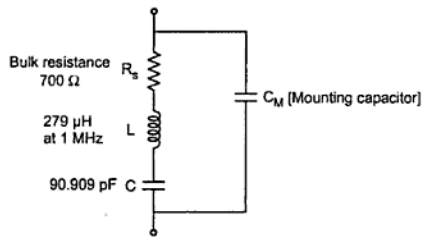


Fig. 2.61(a)

The Fig. 2.61(a) shows the electrical equivalent of the crystal.

At series resonance,

$X_L = X_C$ for crystal

$\therefore$ C = 90.909 pF for crystal

The mounting capacitance is about 1 to 2 pF.

Example 2.35 : *The oscillator circuit is shown in the Fig. 2.62.*

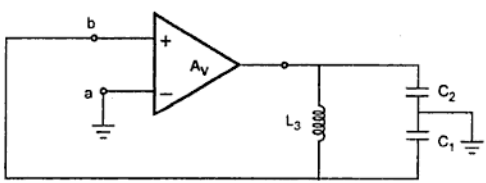


Fig. 2.62

a) If the inductance coil L_3 has the internal resistance r_3 and is taken into account, show that the frequency of oscillations is given by,

$$\omega^2 = \frac{1}{L_3}\left[\frac{1}{C_1} + \frac{1}{C_2}\left(1 + \frac{r_3}{R_o}\right)\right]$$

b) If $\frac{r_3}{R_o} << 1$, *show that the minimum amplifier gain required for the oscillations is,*

$$A_V = \frac{C_1}{C_2} + \frac{C_2 + C_1}{L_3} r_3 R_o$$

(R.U. : 1998)

Solution : a) The equivalent circuit from the basic form of Lc oscillator circuit is shown in the Fig. 2.62 (a).

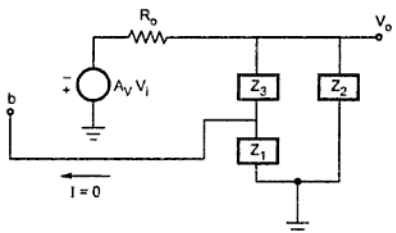


Fig. 2.62(a)

$\therefore Z_1 = -j X_{C1}$, $Z_2 = -j X_{C2}$,

$Z_3 = r_3 + jX_{L3}$

R_0 is the output impedance of the amplifier.

The input impedance of the amplifier is assumed infinite hence there is no input current to the amplifier stage.

As I = 0 to the amplifier, Z_1 and Z_3 appear in series and the combination is in parallel with Z_2.

The circuit is reduced to as shown in the Fig. 2.62 (b).

$$\therefore I = \frac{-A_V V_i}{R_o + Z_L}$$

While $V_o = I Z_L$

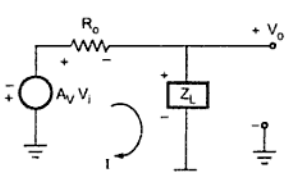


Fig. 2.62(b)

$$\therefore \quad V_o = \frac{-A_V V_i Z_L}{R_o + Z_L} \quad \text{i.e.} \quad \boxed{\frac{V_o}{V_i} = A = \frac{-A_V Z_L}{R_o + Z_L}} \qquad ...(1)$$

where A = Gain of the amplifier stage

and $Z_L = Z_2 \parallel (Z_1 + Z_3) = \frac{Z_2(Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}$ ...(2)

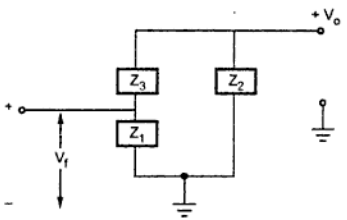


Fig. 2.62 (c)

For calculating the feedback fraction β, consider the feedback circuit as shown in the Fig. 2.62 (c).

From the voltage division rule,

$$V_f = \frac{V_o Z_1}{Z_1 + Z_3}$$

$$\therefore \beta = \frac{V_f}{V_o} = \frac{Z_1}{Z_1 + Z_3} \qquad \ldots(3)$$

But as the phase shift of the feedback network is 180°,

$$\beta = -\frac{Z_1}{Z_1 + Z_3} \qquad \ldots(4)$$

$$\therefore \quad -A\beta = \frac{-A_V Z_L}{R_o + Z_L} \times \frac{Z_1}{Z_1 + Z_3} \qquad \text{where } Z_L = \frac{Z_2(Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}$$

$$= \frac{-A_V \left[\frac{Z_2(Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}\right] Z_1}{\left[R_o + \frac{Z_2(Z_1 + Z_3)}{Z_1 + Z_2 + Z_3}\right](Z_1 + Z_3)} = \frac{-A_V Z_1 Z_2}{R_o(Z_1 + Z_2 + Z_3) + Z_2(Z_1 + Z_3)}$$

$$= \frac{-A_V}{\frac{R_o(Z_1 + Z_2 + Z_3)}{Z_1 Z_2} + \frac{Z_2(Z_1 + Z_3)}{Z_1 Z_2}} = \frac{-A_V}{R_o\left[\frac{1}{Z_1} + \frac{1}{Z_2} + \frac{Z_3}{Z_1 Z_2}\right] + 1 + \frac{Z_3}{Z_1}} \qquad \ldots(5)$$

Now $\frac{1}{Z_1} = Y_1 = j\,\omega C_1$, $\frac{1}{Z_2} = Y_2 = j\,\omega C_2$, $Z_3 = r_3 + j\,\omega L_3$

$$\therefore \quad -A\beta = \frac{-A_V}{R_o[j\omega C_1 + j\omega C_2 + (r_3 + j\omega L_3)(j\omega C_1)(j\omega C_2) + 1 + (r_3 + j\omega L_3)(j\,\omega C_1)}$$

$$= \frac{-A_V}{R_o[j\omega(C_1 + C_2) - (r_3 + j\omega L_3)(\omega^2 C_1 C_2)] + 1 + (r_3 + j\omega L_3)(j\omega C_1)}$$

$$= \frac{-A_V}{j\,\omega\,[R_o(C_1 + C_2) - \omega^2 L_3 R_o C_1 C_2 + r_3 C_1] - R_o r_3 \omega^2 C_1 C_2 + 1 - \omega^2 L_3 C_1} \qquad \ldots(6)$$

For $-A\beta$ to be real, imaginary part of denominator must be zero.

$$\therefore \quad R_o\,(C_1 + C_2) - \omega^2\, L_3\, R_o\, C_1 C_2 + r_3 C_1 = 0$$

$$\therefore \quad \omega^2 L_3 R_o C_1 C_2 = R_o (C_1 + C_2) + r_3 C_1 \text{ i.e. } \omega^2 = \frac{R_o(C_1 + C_2) + r_3 C_1}{L_3 R_o C_1 C_2}$$

$$\therefore \quad \omega^2 = \frac{1}{L_3}\left[\frac{1}{C_1} + \frac{1}{C_2} + \frac{r_3}{R_o C_2}\right] = \frac{1}{L_3}\left[\frac{1}{C_1} + \frac{1}{C_2}\left(1 + \frac{r_3}{R_o}\right)\right] \quad \text{...Proved}$$

b) Equating imaginary part to zero, in the equation (6),

$$-A\beta = \frac{-A_V}{1 - R_o r_3 \omega^2 C_1 C_2 - \omega^2 L_3 C_1} = \frac{A_V}{-1 + \omega^2 [R_o r_3 C_1 C_2 + L_3 C_1]}$$

But for the oscillations, $\frac{A_V}{-1 + \omega^2 [R_o r_3 C_1 C_2 + LC_1]} \geq 1$

$$\therefore \quad (A_V)_{min} = -1 + \omega^2 [R_o r_3 C_1 C_2 + L_3 C_1] \quad \ldots(7)$$

But, $\omega^2 = \frac{1}{L_3}\left[\frac{1}{C_1} + \frac{1}{C_2}\right]$ $\quad \ldots \frac{r_3}{R_o} << 1$ hence $1 + \frac{r_3}{R_o} = 1$

Using in equation (7),

$$(A_V)_{min} = -1 + \frac{1}{L_3}\left[\frac{1}{C_1} + \frac{1}{C_2}\right][R_o r_3 C_1 C_2 + L_3 C_1]$$

$$= -1 + \frac{1}{L_3}(C_1 + C_2) R_o r_3 + \frac{(C_1 + C_2)}{C_2} = -1 + \frac{1}{L_3}(C_1 + C_2) R_o r_3 + 1 + \frac{C_1}{C_2}$$

$$= \frac{C_1}{C_2} + \left(\frac{C_2 + C_1}{L_3}\right) r_3 R_o \quad \text{...Proved}$$

Example 2.36 : *Design a phase shift oscillator using FET or op-amp., to work with 2 kHz frequency. Assume that input resistance without feedback is very high.* **(R.U. : May-2008)**

Solution : $f = 2$ kHz

$$f = \frac{1}{2\pi RC\sqrt{6}} \quad \text{...For phase shift oscillator}$$

Choose $C = 1$ nF

$$\therefore \quad 2 \times 10^3 = \frac{1}{2\pi R \times 1 \times 10^{-9} \times \sqrt{6}}$$

$$\therefore \quad R = 32.487 \text{ k}\Omega$$

Select FET with $g_m = 5000$ μS and $r_d = 50$ kΩ

For phase shift oscillator, $|A| \geq 29$ and $|A| = g_m R_L$

$\therefore \quad g_m R_L \geq 29$

i.e. $\quad R_L \geq \frac{29}{g_m} \geq \frac{29}{5000 \times 10^{-6}} \geq 5.8\ k\Omega$

Select $\quad R_L = 6.8\ k\Omega$

But $\quad R_L = \frac{R_D r_d}{R_D + r_d}$ i.e. $6.8 \times 10^3 = \frac{R_D \times 50 \times 10^3}{R_D + 50 \times 10^3}$

$\therefore \quad R_D = 7.87\ k\Omega$

Review Questions

1. *What is the Barkhausen criterion for the feedback oscillators?*
2. *Explain the classification of the feedback oscillators.*
3. *Classify various oscillators based on output waveforms circuit components, operating frequencies and feedback used.*
4. *Draw a neat circuit diagram of a phase shift oscillator using BJT. Derive an expression for its frequency of oscillations. Determine the minimum 'h_{fe}' for the transistor.*
5. *Draw the Wien bridge oscillator using BJT. Show that the gain of the amplifier must be at least 3 for the oscillations to occur.*
6. *Why the negative feedback is incorporated in the Wien bridge oscillator circuit ?*
7. *Show that the gain of Wien bridge oscillator using BJT amplifier must be atleast 3 for the oscillations to occur.*
8. *What is the type of feedback incorporated in the Wien bridge oscillator circuit ? Explain its working.*
9. *Discuss and explain the basic circuit of an LC oscillator and derive the condition for the oscillations.*
10. *Discuss and explain the basic circuit of an LC oscillator and derive the condition for the oscillations.*
11. *Why the LC oscillators are not suitable for low frequency applications. ? Explain the principle of working of basic LC oscillators.*
12. *Write the short notes on :*
    a. LC oscillators *b. RC oscillators*
    c. Colpitts oscillator *d. Hartley oscillator.*
13. *Explain the working of Hartley oscillator. Derive the formula for the frequency.*
14. *Derive an expression for frequency of oscillation of Hartley oscillator using BJT.*
15. *Derive an expression for frequency of oscillation of Hartley oscillator using transistor.*
16. *Explain the working of Colpitts oscillator. State the formula for the frequency.*
17. *Derive an expression for frequency of oscillation of transistorized Colpitts oscillator.*

18. *Why are RC oscillators preferred for the generation of low frequencies ?*
19. *Derive an expression for the frequency of oscillations of RC-phase shift oscillators using BJT.*
20. *Explain the working of Clapp oscillator.*
21. *What is Piezoelectric effect ? Draw and explain a.c. equivalent circuit of a crystal.*
22. *What is Piezoelectric effect ? Explain the working of Crystal oscillator.*
23. *How frequency stability can be improved in the oscillators ?*
24. *What are the factors that affect the frequency stability of an oscillator. How frequency stability can be improved in oscillators.*
25. *Explain the working of Pierce crystal oscillator.*
26. *Explain the working of Miller crystal oscillator.*
27. *Where does the starting voltage for an oscillator come from ?*
28. *Find C and h_{fe} of a transistor to provide a resonating frequency of 10 kHz of a transistor phase shift oscillator. R_1 = 24 kΩ, R_2 = 68 kΩ, R_C = 18 kΩ, R = 6.8 kΩ and h_{ie} = 2 kΩ.*
(Ans. : 575 pF, ≥ 44.543)
29. *A crystal has L = 0.1 H, C = 0.01 pF, R = 10 kΩ and C_M = 1 pF. Find*
a. Series resonance frequency b. Q factor. **(Ans. : 5.03 MHz, 5.05 MHz, 316.04)**
30. *In a Colpitts oscillator C_1 = 0.00 μF and C_1 = 0.01 μF and L = 5 μH*
a. Calculate frequency of oscillations. b. If L is doubled, find the new frequency.
c. Find L, to double the frequency in (a). **(Ans. : 2.36 MHz, 1.67 MHz, 1.25 μH)**
31. *A crystal oscillator has L = 0.4 H, C = 0.085 pF and Mounting capacitance C_M = 1 pF with R = 5 kΩ. Find series and parallel resonant frequencies. By what percent does the parallel resonant frequencies ? By what percent does the parallel resonant frequency exceed the series resonant frequency ? Also find the Q-factor of the crystal.*
32. *What type of feedback is employed in oscillators ? And what are its advantages ? Discuss the conditions for sustaining oscillations.*
33. *Find the capacitor C and h_{fe} for the transistor to provide a resonating frequency of 10 kHz of transistorized phase-shift oscillator. Assume R_1 = 25 kΩ, R_2 = 60 kΩ, R_C = 40 kΩ, R = 7.1 kΩ and h_{fe} = 1.8 kΩ*

❑❑❑

3 Multivibrators and Blocking Oscillators

3.1 Introduction

The different types of sinusoidal as well as nonsinusoidal waveforms are used in variety of electronic applications. The nonsinusoidal waveforms include the waveforms such as square wave, rectangular wave, triangular wave, sawtooth, ramp etc. There are certain electronic circuits which are in use to generate such nonsinusoidal waveforms.

Key Point : *The electronic circuits which are used to generate nonsinusoidal waveforms are called multivibrators.*

The multivibrator is nothing but a two stage amplifier, operating in two modes. The modes are called **states** of the multivibrator. The output of the first stage is fed to the input of the second stage while the output of the second stage is fed back to the input of the first stage. These input signals drive the active device of one stage to saturation while the other to cut-off. The new set of signals, generating exactly opposite effects, then follows. Thus the cut-off stage now saturates while the saturated stage becomes cut-off.

Key Point : *The overall operation of the multivibrator is based on the fact that no two active devices have exactly identical characteristics.*

This chapter provides the detail analysis of different types of multivibrator circuits.

3.2 Types of Multivibrators

There are three types of multivibrator circuits in use, namely,

a) Bistable multivibrator

b) Monostable multivibrator

c) Astable multivibrator

Let us see the basic concept behind the operation of these three types of multivibrators.

3.2.1 Bistable Multivibrator

As the name suggests, the bistable multivibrator has **two stable states**. The multivibrator can exist indefinitely in either of the two stable states. It requires an external trigger pulse to change from one stable state to another. The circuit remains in one stable state unless an external trigger pulse is applied.

Key Point : *The bistable multivibrator is also known by variety of other names as* ***Eccles-Jordan circuit, trigger circuit, scale-of-2 toggle circuit, flip-flop and binary.***

The bistable multivibrator is used for the performance of many digital operations such as counting and storing of the binary information. This multivibrator circuit also finds an application in the generation and processing of pulse-type waveforms.

3.2.2 Monostable Multivibrator

The monostable multivibrator has **only one stable state**. The other state is unstable referred as quasi-stable state. When an external trigger pulse is applied to the circuit, the circuit goes into the quasi-stable state from its normal stable state. After sometime interval, the circuit automatically returns to its stable state. The circuit does not require any external pulse to change from quasi-stable to stable state. The time interval for which the circuit remains in the quasi-stable state is determined by the circuit components and can be designed as per the requirement.

Key Point : *The monostable multivibrator is also known by variety of other names such as* ***one-shot, single-shot, a single cycle, a single swing, a single step multivibrator*** *or a* ***univibrator.*** *It is also called* ***gating circuit*** *or* ***delay circuit.***

The circuit is used to generate the rectangular waveform and hence can be used to gate other circuits hence called **gating circuit**. The time between the transition from quasi-stable state to stable state can be predetermined and hence it can be used to introduce time delays with the help of fast transition. Due to this application, it is also called **delay circuit**.

3.2.3 Astable Multivibrator

The astable multivibrator has **both the states as quasi-stable states.** None of the states is stable state. Due to this, the multivibrator automatically makes the successive transitions from one quasi-stable state to other, without any external triggering pulse. The rate of transition from one quasi-stable state to other is determined by the circuit components.

Key Point : *As this multivibrator does not require any external pulse for the transition, is called* ***free running multivibrator.***

The astable multivibrator is nothing but an oscillator. It is used as the generator of square waves. As it requires no triggering it is used as a basic source of fast waveforms.

Both monostable and astable multivibrators find extensive application in pulse circuitry.

3.3 Bistable Multivibrator

The general form of bistable multivibrator circuit is shown in the Fig. 3.1.

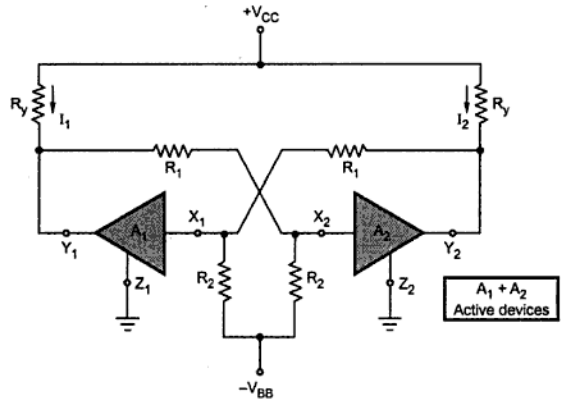


Fig. 3.1 General form of bistable multivibrator circuit

The A_1 and A_2 are the active devices which are transistors. X, Y and Z are the three terminals of transistor. **The supply polarities are as shown in the Fig. 3.1 for npn transistors and must be reversed for pnp transistors.** The output of each transistor amplifier stage is directly coupled to the input of the other stage.

Let I_1 and I_2 be the quiescent currents of the two stages. From the symmetry of the circuit, it is expected that both the currents must be same. These will be same if both the devices are operated in cut-off region or in saturation region. But practically this has no significance.

Let us assume that both the devices are in active region and carry equal currents I_1 and I_2. These currents can be obtained using the Kirchhoff's laws and such a state of the circuit is called **equilibrium state.** But this state is not stable though equilibrium. Let us see why this state is unstable.

Assume that the current I_1 increases under this condition of equilibrium. Due to this, voltage at Y_1 will decrease. This will further decrease the voltage at X_2. This change in voltage at X_2 will be amplified and inverted by A_2 and the output voltage at Y_2 will increase. Thus input voltage at X_1 will increase. This will decrease the voltage at Y_1 further, by further increase in current I_1. The cycle will repeat. The I_1 will keep on increasing and I_2 will keep on decreasing and this drives circuit away from equilibrium.

This happens due to regenerative feedback used and will occur only when the loop gain of circuit is more than unity.

Key Point : *Thus the stable state of bistable multivibrator is one in which the currents and voltages satisfy Kirchhoff's laws and are consistent with the device characteristics and it satisfies the condition that its loop gain is less than unity.*

This is possible only when either of the two transistors is below cut-off or either of the two is in saturation.

Key Point : *Thus in a stable state of bistable multivibrator, one of the transistors is OFF or one of the transistors is ON.*

Practically the bistable multivibrator is designed with one of the transistors is OFF and other is ON i.e. one is below cut-off and other is in saturation. **Both the transistors are never ON or OFF simultaneously.**

There are two types of transistor bistable multivibrator circuits in use, which are :

a) Fixed bias transistor circuit

b) Self biased transistor circuit

Let us discuss these circuits in detail.

3.3.1 Fixed Bias Transistor Bistable Multivibrator

A fixed bias bistable multivibrator circuit using npn transistors is shown in the Fig. 3.2.

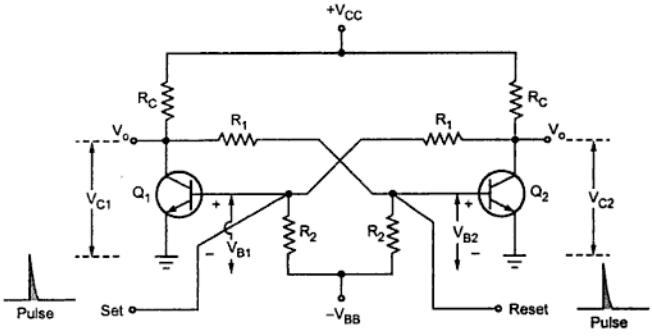


Fig. 3.2 Fixed bias bistable multivibrator

The circuit uses two npn transistors Q_1 and Q_2. The collector of Q_2 is coupled to the base of Q_1 through resistance R_1 while the collector of Q_1 is connected to the base of Q_2 through another resistance R_1.

The characteristics of both the transistors are never identical hence after giving supply one of the transistors start conducting ahead of the other.

To understand the operation of the circuit, let us assume that Q_2 starts conducting ahead of Q_1 and hence current drawn by Q_2 is more than the current drawn by Q_1. As explained earlier, due to regenerative feedback, current drawn by Q_2 keeps on increasing and that drawn by Q_1 keeps on decreasing. Finally this cumulative process drives the transistor Q_2 to saturation and Q_1 to cut-off. This is a stable state of the multivibrator. The circuit remains in this state till an external trigger pulse is applied at the set or reset terminal.

If a positive going pulse is applied at the set or reset terminal, it will drive the transistor Q_1 to saturation and the transistor Q_2 to cut-off. This is nothing but the second stable state of the multivibrator. The circuit remains in this stable state though the applied pulse is removed.

Key Point : *It will remain in this state till another pulse is applied to reset terminal.*

Thus the two stable states of the bistable multivibrator are :

1) Q_1 OFF (cut-off) and Q_2 ON (saturation)

2) Q_2 OFF (cut-off) and Q_1 ON (saturation)

The change of states is totally dependent on the applied pulse at the proper terminal i.e. set or reset terminal. The spacing of the triggering pulses finally decides the shape of the output waveform.

Under saturation condition, collector current I_C is maximum. Hence the resistance R_C must be chosen in such a way that the value of current I_C will not exceed the maximum permissible value of the collector current for the transistor. So R_C must be chosen such that $I_C \approx V_{CC}/R_C$ is less than the maximum permissible current.

The values of R_1, R_2 and V_{BB} must be chosen in such a way that in one state the base current is large enough to drive the transistor into saturation while in other state the emitter junction is well below cut-off.

The change in the collector voltages resulting due to the transition from one state to other is called **output voltage swing** denoted as V_w.

$$\therefore \quad \boxed{V_w = V_{C1} - V_{C2}} \qquad \ldots (1)$$

The waveforms at the two collectors are complement of each other and are shown in the Fig. 3.3. For the cut-off transistor, the collector voltage is nothing but V_{CC}, neglecting loading of R_1.

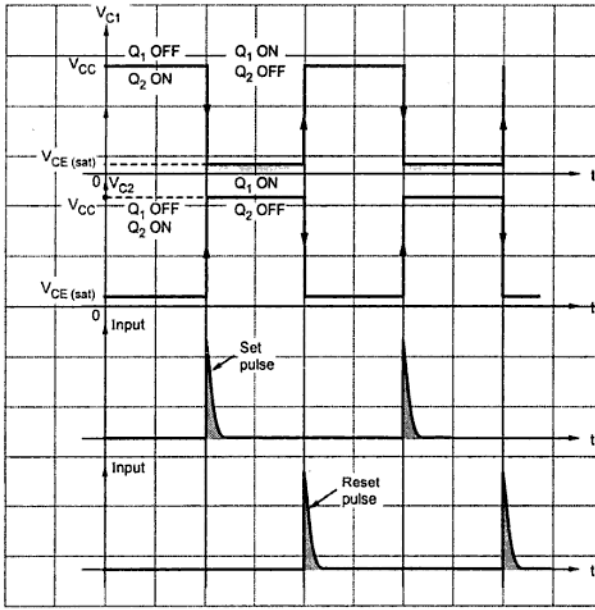


Fig. 3.3 Output waveforms of bistable multivibrator

The detail analysis of fixed bias multivibrator circuit will be clear from the example 3.1. **The solution shows how to calculate steady state currents and voltages for the circuit.**

Example 3.1 : *The fixed bias bistable multivibrator uses following parameters :*

$V_{CC} = +12\ V$, $V_{BB} = -8\ V$, $R_1 = 10\ k\Omega$, $R_2 = 50\ k\Omega$, $R_C = 2.2\ k\Omega$

The transistors are silicon transistors with a minimum value of h_{fe} *as 30. Calculate the stable state currents and voltages when*

i) All junction voltages are neglected ii) Assuming V_{CE} *(sat) = 0.2 V and* V_{BE} *(sat) = 0.7 V.*

Solution : The circuit is similar to the circuit shown in the Fig. 3.2. Assume that Q_1 is OFF and Q_2 is ON.

Case i : Junction voltages of ON transistor are neglected.

i.e. $V_{CE2} = 0$ V and $V_{BE2} = 0$ V ... (1)

As emitter is grounded we can say,

$V_{C2} = 0$ V and $V_{B2} = 0$ ... (2)

Now draw the equivalent circuit in a part from base of Q_1 to the collector of Q_2 as shown in Fig. 3.4 (a).

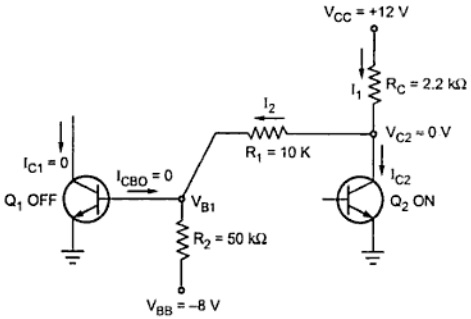


Fig. 3.4 (a)

Now $$V_{B1} = -V_{BB}\left(\frac{R_1}{R_1 + R_2}\right) \quad \text{... (3)}$$

$$= -8\left(\frac{10}{10+50}\right) = -1.33 \text{ V}$$

As $V_{B1} < V_{BE}$ (cut-off) i.e. 0.7 V, it ensures that Q_1 is OFF. To verify whether Q_2 is ON or not, calculate I_{C2}.

$$I_1 = \frac{V_{CC}}{R_C} = \frac{12}{2.2\times10^3} \quad \text{... (4)}$$

$$= \mathbf{5.45\ mA}$$

$$I_2 = \frac{V_{BB}}{R_1 + R_2} = \frac{8}{(10+50)} = 0.133 \text{ mA} \quad \text{...(5)}$$

$\therefore$ $$I_{C2} = I_1 - I_2 = \mathbf{5.316\ mA} \quad \text{... (6)}$$

$$\therefore \quad (I_{B2})_{min} = \frac{I_{C2}}{(h_{fe})_{min}} = \frac{5.316}{30} = \mathbf{0.177\ mA} \qquad \ldots(7)$$

Now to calculate actual I_{B2} and verify that $I_{B2} > (I_{B2})_{min}$ let us draw part of circuit showing collector of Q_1 to base of Q_2.

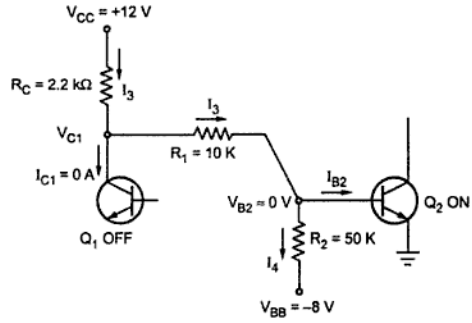


Fig. 3.4 (b)

Now I_3 = Current through R_C and R_1, as $I_{C1} = 0$

$$\therefore \quad I_3 = \frac{V_{CC}}{R_C + R_1} \quad \text{as } V_{B2} = 0\ V \qquad \ldots(8)$$

$$= \frac{12}{2.2+10} = 0.9836\ mA$$

and $$I_4 = \frac{V_{B2} - V_{BB}}{R_2} = \frac{0-(-8)}{50} = \mathbf{0.16\ mA} \qquad \ldots(9)$$

$$\therefore \quad I_{B2} = I_3 - I_4 \qquad \ldots(10)$$

$$= \mathbf{0.8236\ mA}$$

As $I_{B2} > (I_{B2})_{min}$, the transistor Q_2 is indeed in saturation.

$$\therefore \quad V_{C1} = V_{CC} - I_3 R_C = 12 - 0.98396 \times 2.2 \qquad \ldots(11)$$

$$= \mathbf{9.836\ V}$$

Hence the stable state current and voltages are :

$I_{C1} = 0A$	$I_{C2} = 5.316\ mA$	$I_{B1} = 0\ A$	$I_{B2} = 0.8236\ mA$
$V_{C1} = 9.836\ V$	$V_{C2} = 0\ V$	$V_{B1} = -1.33\ V$	$V_{B2} = 0\ V$

$$\text{Output swing} = V_{C1} - V_{C2} = 9.836 - 0$$

$$\therefore \quad V_w = \mathbf{9.836\ V}$$

Case ii : $V_{CE}(sat) = 0.2$ V and $V_{BE}(sat) = 0.7$ V

For the transistor Q_2, as emitter is grounded, from these voltages we can write,

$$V_{C2} = 0.2 \text{ V and } V_{B2} = 0.7 \text{ V} \qquad \ldots(1)$$

Referring to Fig. 3.4 (a), we can write the equations to obtain the stable state currents and voltages.

Now V_{B1} will be due to V_{BB} and V_{C2} hence using superposition principle, considering effect of each independently we can write,

$$V_{B1} = -V_{BB}\left(\frac{R_1}{R_1+R_2}\right)\Bigg|_{V_{C2}=0} + V_{C2}\left(\frac{R_2}{R_1+R_2}\right)\Bigg|_{V_{BB}=0} \qquad \ldots(2)$$

$$= -8\left(\frac{10}{10+50}\right)+(0.2)\left(\frac{50}{10+50}\right)$$

$$= \mathbf{-1.16\ V}$$

Key Point : *As V_{B1} is less than V_{BE} (cut-off) hence Q_1 is indeed OFF.*

$$I_1 = \frac{V_{CC}-V_{C2}}{R_C} = \frac{12-0.2}{2.2} = 5.36 \text{ mA} \qquad \ldots(3)$$

$$I_2 = \frac{V_{C2}+V_{BB}}{R_1+R_2} = \frac{0.2+8}{(10+50)} = 0.136 \text{ mA} \qquad \ldots(4)$$

$$\therefore \quad I_{C2} = I_1 - I_2 = 5.36 - 0.136 \qquad \ldots(5)$$

$$= \mathbf{5.223\ mA}$$

$$\therefore \quad (I_{B2})_{min} = \frac{I_{C2}}{(h_{fe})_{min}} = \frac{5.223}{30} \qquad \ldots(6)$$

$$= \mathbf{0.174\ mA}$$

To calculate I_{B2}, refer Fig. 3.4 (b), with $V_{B2} = 0.7$ V

$$\therefore \quad I_3 = \frac{V_{CC}-V_{B2}}{R_C+R_1} = \frac{12-0.7}{(2.2+10)} = 0.926 \text{ mA} \qquad \ldots(7)$$

and $$I_4 = \frac{V_{B2}-V_{BB}}{R_2} = \frac{0.7-(-8)}{50} = 0.174 \text{ mA} \qquad \ldots(8)$$

$$= 0.174 \text{ mA}$$

$$\therefore \quad I_{B2} = I_3 - I_4 = \mathbf{0.752\ mA}$$

Key Point : *As $I_{B2} > (I_{B2})_{min}$ the transistor Q_2 is indeed ON.*

$$\therefore \quad V_{C1} = V_{CC} - I_3 R_C = 12 - 0.926 \times 2.2 \quad \ldots (10)$$

$$= 9.9628 \text{ V}$$

Hence the stable state currents and voltages are :

$I_{C1} = 0$ mA	$I_{C2} = 5.223$ mA	$I_{B1} = 0$ mA	$I_{B2} = 0.752$ mA
$V_{C1} = 9.9628$ V	$V_{C2} = 0.2$ V	$V_{B1} = -1.16$ V	$V_{B2} = 0.7$ V

$$V_w = V_{C1} - V_{C2} \quad \ldots (11)$$

$$= 9.7628 \text{ V}$$

3.3.2 Loading Considerations

The bistable multivibrator is used to drive other circuits and hence most of the times, there are shunting load resistances connected to both the collectors of the transistors. Such loads reduce the magnitude of the collector voltages V_{C1} and V_{C2} of the OFF transistors, in the respective alternate stable states. This reduces the output voltage swing. And if V_{C1} decreases, I_{B2} also decreases and hence transistor Q_2 cannot be ensured to be in saturation. Hence the loading effect must be considered while designing. And the components of the multivibrator must be designed so that under the heaviest load also, one transistor remains in saturation and other in cut-off.

Calculation of heaviest load current

To calculate heaviest load current, consider the load resistance connected to transistor Q_1 as shown in the Fig. 3.5.

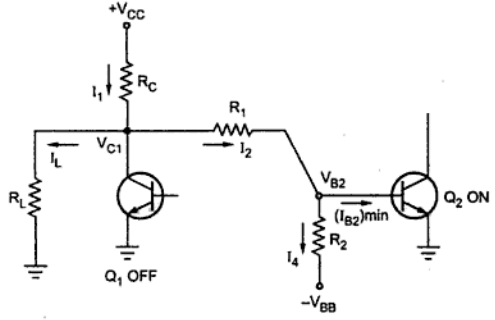


Fig. 3.5 Loading effect

Now V_{B2} and $(I_{B2})_{min}$ required to keep Q_2 in saturation is known. The current I_4 can be calculated.

$$I_4 = \frac{V_{B2} - V_{BB}}{R_2} \quad \ldots (1)$$

Now $$I_2 = I_4 + (I_{B2})_{min} \quad \ldots(2)$$

$$I_2 = \frac{V_{C1} - V_{B2}}{R_1} \quad \ldots (3)$$

From equation (3), V_{C1} can be determined.

$$V_{C1} = V_{CC} - I_1 R_C \quad \ldots(4)$$

Hence current I_1 can be obtained.

and $$I_1 = I_L + I_2 \quad \ldots(5)$$

Thus the load current I_L can be obtained. As to obtain this I_L, $(I_{B2})_{min}$ is consider, this is the heaviest load which circuit can drive, maintaining Q_2 in saturation. The corresponding R_L minimum can be obtained as,

$$\boxed{R_L = \frac{V_{C1}}{I_L}} \quad \ldots (6)$$

Key Point : *Since the resistance R_1 also loads the OFF transistor, the value of R_1 must be large compared with R_C.*

To ensure a loop gain in excess of unity during the transition between the states it is necessary to satisfy inequality,

$$\boxed{R_1 < h_{fe} R_C} \quad \ldots (7)$$

3.3.2.1 Design of Fixed Bias Bistable Multivibrator

For the design purpose assume that the values of V_{CC}, V_{BB}, $(h_{fe})_{min}$ and I_C (sat) values are known. Now use the following hints to get the design :

1) Assume Q_1, Q_2 to be npn transistors and assume suitable junction voltages depending on whether transistors are silicon or germanium.
2) The base current of the ON transistor is taken as 1.5 times the minimum value.
$$I_B = 1.5\ (I_B)_{min}$$
3) The current through R_2 of the ON transistor is taken as one tenth of its collector current.
4) The current through R_1 towards ON transistor can be neglected and hence current drawn from supply by ON transistor can be assumed equal to the collector current of ON transistor so in Fig. 3.4, $I_1 = I_{C2}$ can be assumed ignoring I_2.

The unknown resistances can be obtained as below :

Assume Q_2 ON and Q_1 OFF. Consider the equivalent circuit shown in the Fig. 3.6 (a)

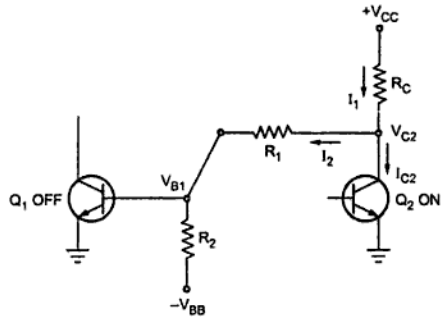


Fig. 3.6 (a)

$$V_{C2} = V_{CE}(sat)$$

$$\therefore \quad I_1 = \frac{V_{CC} - V_{CE}(sat)}{R_C} \approx I_{C2} \qquad \text{neglecting } I_2$$

$$\therefore \quad \boxed{R_C = \frac{V_{CC} - V_2}{I_{C2}}} \qquad \text{and } I_{C2} = I_C(sat) \text{ known.}$$

So R_C can be determined.

Refer to another equivalent circuit shown in the Fig. 3.6 (b).

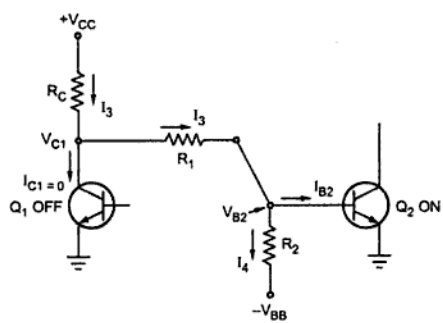


Fig. 3.6 (b)

Now $I_4 = \frac{I_{C2}}{10}$ ..... as per hint (3)

And $I_4 = \frac{V_{B2} - (-V_{BB})}{R_2}$

$\therefore$ $\boxed{R_2 = \frac{V_{B2} + V_{BB}}{I_4}}$

Thus R_2 is known.

Now current through R_1 is I_3.

And $I_3 = I_4 + I_{B2}$

$I_{B2} = 1.5\ (I_{B2})_{min}$ ..... known

$\therefore$ I_3 is known.

Now $I_3 = \frac{V_{CC} - V_{B2}}{R_1 + R_C}$

$\therefore$ $\boxed{R_1 = \frac{V_{CC} - V_{B2}}{I_3} - R_C}$

So R_1 is also known.

Thus the final design can be obtained.

Key Point : *For the pnp transistors the supply polarities must be reversed and accordingly the changes must be made while using the above mentioned equations, to calculate the unknown resistances.*

3.3.3 Self Biased Transistor Bistable Multivibrator

The need for the negative power supply in fixed bias bistable multivibrator can be eliminated by using a common emitter resistance R_E. This resistance provides the necessary bias to keep one transistor ON and other OFF, in the stable state. Such type of biasing is called **self biasing** and the circuit is called **self biased bistable multivibrator** circuit. The resistance R_E is connected between a common emitter terminal of both the transistors and the ground. The circuit of self biased bistable multivibrator is shown in the Fig. 3.7.

The circuit uses two npn transistors Q_1 and Q_2. For pnp transistors the polarity of V_{CC} must be reversed.

Key Point : *In the fixed bias, $-V_{BB}$ provides the necessary biasing voltage to ensure one transistor OFF. In this circuit, this required biasing voltage is provided by the $I_E R_E$ drop.*

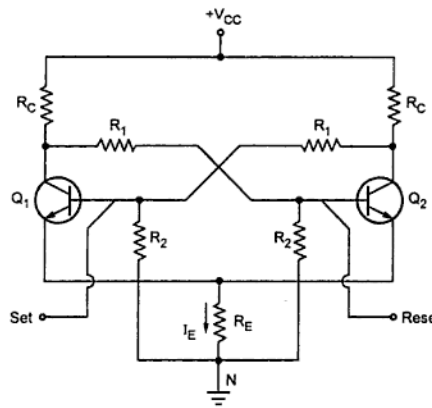


Fig. 3.7 Self biased bistable multivibrator

Except this fact that the external supply at V_{BB} terminal is not required, the working of this circuit is similar to that of fixed bias circuit. The voltage waveforms available at the two collectors are complement of each other and are same as shown in the Fig. 3.3.

The calculations of stable state currents and voltages are in principle, the same as shown for fixed bias and are illustrated in the following example.

Example 3.2 : *Calculate the stable state currents and voltages for the self biased bistable multivibrator which uses n-p-n silicon transistors. The various parameters for the circuit are :*

$V_{CC} = 12\ V$, $R_1 = 30\ k\Omega$, $R_C = 4\ k\Omega$, $R_2 = 10\ k\Omega$ *and* $R_E = 500\ \Omega$

Also find the minimum value of h_{fe} *which will keep the ON transistor in saturation.*

Solution : Assume that the transistor Q_1 is cut-off and the transistor Q_2 is in saturation. Let us draw again the equivalent circuit from the base of Q_1 to the collector of Q_2.

This is shown in the Fig. 3.8.

Another equivalent circuit from collector of Q_1 to base of Q_2 is shown in the Fig. 3.9.

To calculate the various voltages, it is necessary to calculate the current I_{C1}, I_{B2} as Q_2 is ON. The currents $I_{C1} = I_{B1} = 0$ as Q_1 is OFF.

Now it is not very easy to calculate these currents by writing the equations from the equivalent circuits shown in the Fig. 3.8 and 3.9. So to calculate the currents let us obtain Thevenin's equivalent circuit once across collector and ground while another across base and ground for the same transistor Q_2 assuming it as the load.

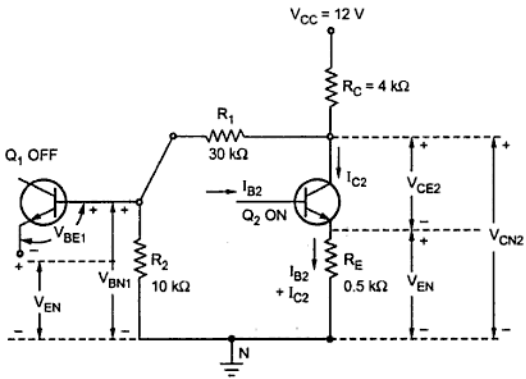


Fig. 3.8 Equivalent circuit

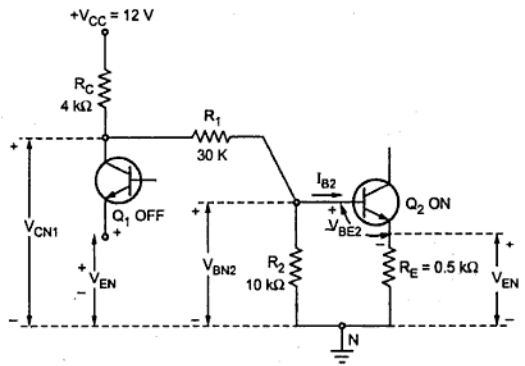


Fig. 3.9 Equivalent circuit

To replace collector circuit of Q_2 by Thevenin's equivalent, consider Q_2 as open shown in the Fig. 3.10.

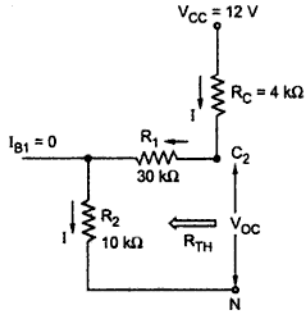


Fig. 3.10

Referring to Fig. 3.10,

$$V_{OC} = I(R_1 + R_2) = \frac{V_{CC}}{(R_1 + R_2 + R_C)}(R_1 + R_2)$$

$$= \frac{12 \times 40}{(30+10+4)} = 10.9 \text{ V}$$

and $$R_{TH} = (R_1 + R_2) \parallel R_C \quad \text{with } V_{CC}\text{-N short}$$

$$= \frac{40 \times 4}{40+4} = 3.363 \text{ k}\Omega$$

To replace base circuit of Q_2 by Thevenin's equivalent, consider Q_2 open and draw circuit as shown in the Fig. 3.11.

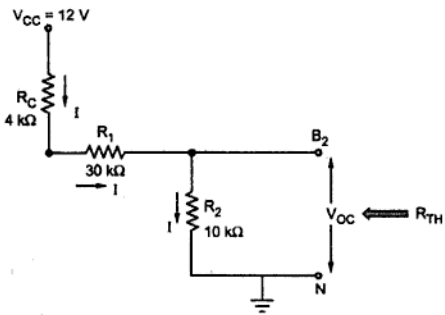


Fig. 3.11

$$\therefore \quad V_{OC} = I R_2 = \frac{V_{CC}}{(R_C + R_1 + R_2)} \cdot R_2$$

$$= \frac{12 \times 10}{(4 + 30 + 10)} = 2.73 \text{ V}$$

and $$R_{TH} = (R_2) \parallel (R_1 + R_C)$$

$$= \frac{10 \times 34}{44} = 7.727 \text{ k}\Omega$$

Thus the equivalent circuit for Q_2 ON, using Thevenin's result calculated above, is as shown in the Fig. 3.12.

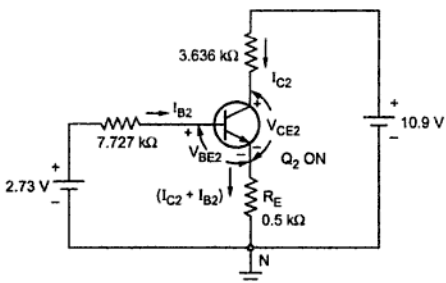


Fig. 3.12

For silicon transistors,

$$V_{BE}(\text{sat}) = 0.8 \text{ V and } V_{CE}(\text{sat}) = 0.4 \text{ V}$$

Applying KVL to base-emitter loop,

$$-7.727 I_{B2} - V_{BE2} - (I_{C2} + I_{B2}) 0.5 + 2.73 = 0$$

With $V_{BE2} = 0.8$ V, $\quad I_{B2} + 0.06075 I_{C2} = 0.2345 \quad \ldots (1)$

Applying KVL to collector-emitter loop,

$$-3.636 I_{C2} - V_{CE2} - (I_{C2} + I_{B2}) 0.5 + 10.9 = 0$$

With $V_{CE2} = 0.4$ V, $4.14 I_{C2} + 0.5 I_{B2} = 10.5 \quad \ldots (2)$

Solving equations (1) and (2) simultaneously we get,

$$I_{C2} = 2.526 \text{ mA} \quad \text{and} \quad I_{B2} = 0.0847 \text{ mA}$$

$$\therefore \quad (h_{fe})_{min} = \frac{I_{C2}}{I_{B2}} = \frac{2.526}{0.0847}$$

$$\therefore \quad (h_{fe})_{min} = \mathbf{29.815}$$

The various voltages can be obtained now by referring Fig. 3.8 and Fig.3.9.

$$V_{EN} = (I_{B2} + I_{C2})\, R_E = 1.305 \text{ V}$$

$$V_{CN2} = V_{CE2} + V_{EN} = 0.4 + 1.305 = 1.705 \text{ V}$$

$$V_{BN2} = V_{BE2} + V_{EN} = 0.8 + 1.305 = 2.105 \text{ V}$$

$$V_{BN1} = V_{CN2} \times \frac{R_2}{R_1 + R_2} = 1.705 \times \left(\frac{10}{40}\right) = 0.4262 \text{ V}$$

$$V_{BE1} = V_{BN1} - V_{EN} = 0.4262 - 1.305 = -0.8788 \text{ V}$$

As $V_{BE1} < V_{BE}(sat)$ which is about 0.8 V, the transistor Q_1 is indeed OFF.

$$V_{CN1} = \frac{V_{CC} R_1}{(R_C + R_1)} + \frac{V_{BN2} R_C}{R_C + R_1} \quad \text{using Superposition principle}$$

$$= \frac{12 \times 30}{34} + \frac{2.105 \times 4}{34} = 10.8358 \text{ V}$$

Thus the stable state voltages and currents are :

$I_{C1} = 0$ mA	$I_{C2} = 2.526$ mA	$I_{B1} = 0$ mA	$I_{B2} = 0.0847$ mA
$V_{CN1} = 10.835$ V	$V_{CN2} = 1.705$ V	$V_{BN1} = 0.4262$ V	$V_{BN2} = 2.105$ V
and $V_{EN} = +1.305$ V			

The voltage V_{EN} provides the required self bias.

Function of C_E :

The drop across the resistance R_E is normally same in both the stable states. But during the transition from one state to another, the emitter current I_E varies by small amount say by ΔI_E. Hence to keep the voltage V_{EN} constant which provides the required self bias, during the transition period, a capacitor C_E is generally used across the resistance R_E.

Key Point : *The stable states are not affected by C_E but voltage V_{EN} gets maintained constant between transition of states which helps the multivibrator to settle down to its new state quickly.*

3.3.3.1 Design of Self Biased Bistable Multivibrator

Similar to the design of fixed bias bistable multivibrator assume that V_{CC}, $(h_{fe})_{min}$, $I_C(sat)$ for ON transistor and all junction voltages are known.

The following are the additional hints for the design :

1) $I_B(sat)$ is assumed as twice the minimum value.

$\therefore \quad I_B(sat) = 2\,(I_B)_{min}$

2) Assume $R_1 = R_2$

3) The current through R_1 which is connected between collector of ON transistor and base of OFF transistor, can be neglected.

Hence the unknown resistances can be obtained in the order R_E, R_C and then $R_1 = R_2$.

3.3.4 Speed-up Capacitors or Commutating Capacitors

The bistable multivibrator remains in the stable state till the triggering pulse is applied to set or reset terminal. In some applications, it is necessary that the transition from one state to other should occur instantaneously, when abruptly changing pulse is applied to the circuit. This means **transition time** of the circuit should be as small as possible.

Key Point : *The transition time is defined as the time interval during which conduction transfers from one transistor to other.*

In practice, the switching characteristics can be improved by passing the high frequency components of the pulses. For this purpose, small capacitances are used in shunt with the coupling resistors R_1. Due to this, the transition time reduces considerably without affecting the stable states. These capacitors allow fast rise and fall times. Thus it avoids any distortion in the output waveform. As these capacitors help the multivibrator

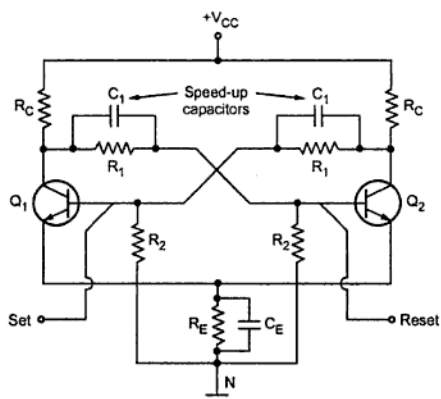


Fig. 3.13 Practical self biased bistable multivibrator

in making instantaneous transitions between the states, they are known as **commutating capacitors, speed-up capacitors** or **transpose capacitors.**

A self biased bistable multivibrator, using npn transistors and the speed-up capacitors is shown in the Fig. 3.13. See Fig. 3.13 on previous page.

The values of commutating capacitors lie in the range of tens to some hundreds of picofarads.

The smallest allowable interval between triggers is called **resolving time** of the binary. This means, the resolving time should be sufficient so that all the transients die out completely and hence the flip-flop can be triggered reliably.

Key Point : *Thus, resolving time decides the maximum frequency of triggering to which binary can respond.*

$$\therefore \quad \boxed{f_{max} = \frac{1}{\text{Resolving time}}}$$

The sufficient resolving time ensures that succeeding trigger can reliably cause the change of state.

The f_{max} is given by the expression,

$$\therefore \quad \boxed{f_{max} = \frac{1}{2\,C_1\,(R_1 \,||\, R_2)} = \frac{(R_1 + R_2)}{2C_1\,R_1\,R_2}}$$

This expression helps us to find value of $C_1 = C_2$ for the maximum frequency.

3.3.5 Applications

The various applications of bistable multivibrator are :

1) Used for the performance of many digital operations like counting and storing of digital information.
2) Used as memory element in shift registers, counters etc.
3) Used in processing of pulse type waveforms.
4) Used to generate the symmetrical square wave. This is possible by using triggering pulses of equal interval, corresponding to the frequency required.
5) Can be used as a frequency divider.

3.4 Collector Coupled Monostable Multivibrator

As mentioned earlier, the monostable multivibrator has one stable state. When an external trigger is applied, the circuit changes its state from stable to quasi-stable state. And then automatically, after sometime interval T, the circuit returns back to the original normal stable state. The time T is dependent on the circuit components.

The Fig. 3.14 shows the collector coupled monostable multivibrator circuit, which uses npn transistors. This circuit is also called collector to base coupled monostable multivibrator or one shot multivibrator.

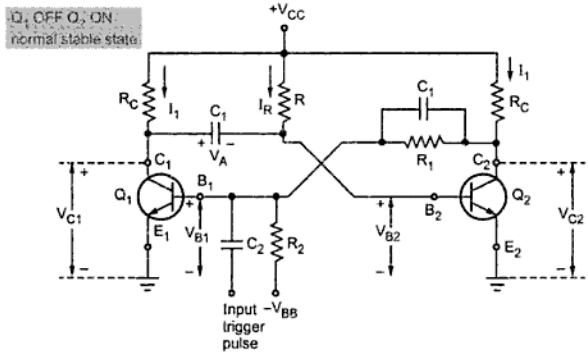


Fig. 3.14 Collector coupled monostable multivibrator

The Q_1 and Q_2 are identical npn transistors. The two collector resistances are equal to R_C. The output of Q_2 i.e. collector of Q_2 is coupled to the base of Q_1 through a resistance R_1, which is shunted by a small capacitor C_1. The capacitor C_1 is a speed-up capacitor required to make the transition fast and reduce the transition time. The collector of Q_1 is coupled to the base of Q_2 through a capacitor C. Thus a d.c. coupling in bistable multivibrator is replaced by a capacitive coupling. The resistance R at the input of Q_2 is returned to the supply voltage V_{CC}.

The value of R_2 and $-V_{BB}$ are chosen such that the transistor Q_1 is OFF, by reverse biasing it. The transistor Q_2 is ON i.e. in saturation. This is possible by forward biasing Q_2 with the help of V_{CC} and resistance R. Thus Q_2 ON and Q_1 OFF is the **normal stable state** of the circuit. The positive triggering pulse is to be applied to the base of Q_1 through capacitor C_2. It must be noted that the triggering is unsymmetrical and is to be applied to one transistor only and not to both simultaneously.

When a positive trigger of sufficient magnitude and duration is applied to the base of Q_1, the transistor Q_1 starts conducting. Due to this, voltage at its collector V_{C1} decreases. This is coupled to base of Q_2 through C. But voltage across capacitor cannot change

instantaneously. Hence decrease in V_{C1} directly cause a decrease in the base voltage of Q_2 i.e. V_{B2}. The drop in voltage is about $I_1 R_C$. This decreases the forward bias of Q_2 and hence collector current I_2 decreases. Thus the collector voltage of Q_2 increases which is applied to the base of Q_1, through R_1. This further increases the base potential of Q_1 and Q_1 is quickly driven in saturation and at the same time, the transistor Q_2 gets driven to cut-off. This is quasi-stable state of the circuit.

The circuit will remain in this quasi-stable state for only a finite time T. In the quasi-stable state, the capacitor C starts charging through the path V_{CC}, R and ON transistor Q_1. As it starts charging towards V_{CC}, the base of Q_2 experiences rise in voltage. When this voltage becomes more than cut in voltage V_γ of Q_2, then Q_2 starts conducting. And due to the regenerative action, Q_1 is turned OFF. Thus the circuit returns back to its stable state.

Key Point : *The circuit remains in the stable state till next triggering pulse occurs.*

3.4.1 Pulse Width of Collector Coupled Monostable Multivibrator

The pulse width is the time for which the circuit remains in the quasi-stable state. It is also called gate width and denoted as T.

Derivation of Pulse Width

To derive its expression, consider the voltage variation at base of Q_2.

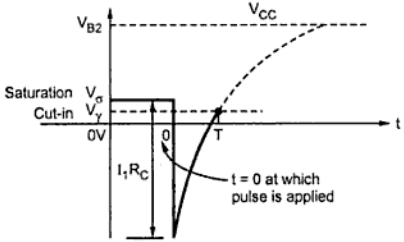


Fig. 3.15 V_{B2} Vs t graph

Initially Q_2 is in saturation **and hence $V_{B2} = V_{BE2}(sat) = V_\sigma$ which is about 0.8 V for silicon transistor.** When the pulse is **applied at t = 0,** then at $t = 0^+$, as capacitor voltage cannot change instantaneously, the voltage V_{B2} decreases by I_1R_C. Then capacitor charges exponentially hence V_{B2} also increases exponentially, whose final value at $t \to \infty$ is V_{CC}. But when V_{B2} becomes equal to V_γ then Q_2 starts conducting and circuit comes back to stable state. This is the time T at which transition occurs. The graph of V_{B2} against time is shown in the Fig. 3.15.

To write equation for exponential charging of capacitor we can write,

$t = 0^+$, $\quad V_i = V_\sigma - I_1 R_C$

$t = \infty$, $\quad V_f = V_{CC}$

$$\therefore \quad \boxed{V_C = V_f - (V_i - V_f)\, e^{-t/\tau}} \quad \text{... (Basic equation)}$$

where τ = Time constant

$$\therefore \quad V_{B2} = V_{CC} - (V_{CC} - V_\sigma + I_1 R_C)\ e^{-t/\tau} \quad \ldots (1)$$

At t = T, $V_{B2} = V_\gamma$ ... (2)

Substituting equation (2) into equation (1) and solving for T we get,

$$\therefore \quad \boxed{T = \tau ln\left(\frac{V_{CC} + I_1 R_C - V_\sigma}{V_{CC} - V_\gamma}\right)} \quad \ldots (3)$$

where V_σ = 0.3 V for germanium

= 0.8 V for silicon

When Q_1 is in saturation under quasi-stable state we can write,

$$V_{C1} = V_{CE}(sat) \quad \ldots (4)$$

$$\therefore \quad I_1 R_C = V_{CC} - V_{CE}(sat) \quad \ldots (5)$$

Substituting in equation (3),

$$\therefore \quad T = \tau ln\left(\frac{V_{CC} + V_{CC} - V_{CE}(sat) - V_{BE}(sat)}{V_{CC} - V_\gamma}\right) \quad \ldots (6)$$

This is because, $V_\sigma = V_{BE}(sat)$

$$\therefore \quad T = \tau ln\left(\frac{2V_{CC} - V_{CE}(sat) - V_{BE}(sat)}{V_{CC} - V_\gamma}\right) \quad \ldots (7)$$

$$\therefore \quad T = \tau ln\left\{\frac{2\left[V_{CC} - \left(\frac{V_{CE}(sat) + V_{BE}(sat)}{2}\right)\right]}{V_{CC} - V_\gamma}\right\} \quad \ldots (8)$$

$$\therefore \quad T = \tau ln(2) + \tau ln\left\{\left[\frac{V_{CC} - \left(\frac{V_{CE}(sat) + V_{BE}(sat)}{2}\right)}{V_{CC} - V_\gamma}\right]\right\} \quad \ldots (9)$$

At room temperature,

$$V_{CE}(sat) + V_{BE}(sat) \approx 2V_\gamma \quad \ldots (10)$$

Substituting in equation (9),

$$\therefore \quad T = \tau\, ln\,(2) + \tau\, ln\,(1)$$

$$\therefore \quad \boxed{T = \tau \ln (2)} \qquad \ldots (11)$$

The time constant τ for the charging path of capacitor C is RC.

$$\therefore \quad \tau = RC \qquad \ldots (12)$$

$$\therefore \quad \boxed{T = 0.69\ RC} \qquad \ldots (13)$$

Thus the gate width is dependent on transistor characteristics, supply voltages and resistance values. It is dependent on temperature, as $V_{BE}(sat)$, $V_{CE}(sat)$ and V_γ depend on the temperature.

Key Point : *The gate width T decreases as the temperature increases. Larger the value of V_{CC}, smaller is this effect.*

One remedy for this temperature effect is to connect R not to V_{CC} but to source V whose value decreases as the temperature decreases, thus compensating the effect of temperature.

3.4.2 Waveforms of Monostable Multivibrator

To obtain the waveforms, let us assume that the external pulse is applied at t = 0 and reverse transition from quasi-stable to stable state occurs at t = T.

The stable state : The transistor Q_1 is OFF and Q_2 is ON in the stable state. The stable state currents and voltages can be obtained as shown earlier for bistable multivibrator circuit. The Q_2 is in saturation hence for Q_2,

$$\therefore \quad \boxed{V_{B2} = V_{BE}(sat) = V_\sigma} \qquad \ldots(14)$$

and

$$\boxed{V_{C2} = V_{CE\ (sat)}} \qquad \ldots(15)$$

The Q_1 is OFF hence as current is zero we can write,

$$\boxed{V_{C1} = V_{CC}} \qquad \ldots (16)$$

The base voltage of Q_1 can be obtained by using Superposition principle as shown by equation (2) in case (ii) of example 3.1.

$$\boxed{V_{B1} = \frac{-V_{BB}\ R_1}{R_1 + R_2}\bigg|_{V_{C2}=0} + \frac{V_{C2}\ R_2}{R_1 + R_2}\bigg|_{V_{BB}=0} \simeq V_F} \qquad \ldots (17)$$

To have Q_1 OFF, $|V_F| \leq 0$ for silicon while $|V_F| \leq 0.1$ V for germanium transistor.

The quasi-stable state : When pulse is applied at t = 0, Q_2 becomes OFF and Q_1 becomes ON.

The voltages at V_{C1} and V_{B2} drop instantaneously by the amount I_1R_C where I_1 is current drawn by Q_1 when it starts conducting. Then Q_1 gets driven into saturation hence,

$$V_{B1} = V_\sigma \quad \ldots(18)$$

$$V_{C1} = V_{CE}(sat) \quad \ldots(19)$$

and

$$I_1 R_C = V_{CC} - V_{CE}(sat) \quad \ldots(20)$$

To calculate V_{C2}, consider the equivalent circuit for $0 < t < T$ as shown in the Fig. 3.16.

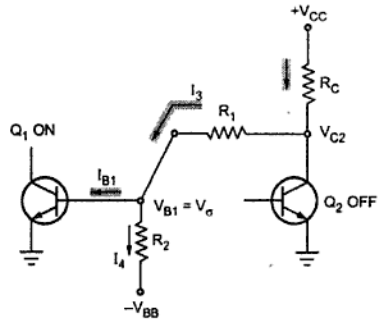


Fig. 3.16 Equivalent circuit in quasi-stable state

By using the superposition principle we can write,

$$V_{C2} = \left.\frac{V_{CC} R_1}{R_1 + R_C}\right|_{V_B = 0} + \left.\frac{V_\sigma R_C}{R_1 + R_C}\right|_{V_{CC} = 0} \quad \ldots (21)$$

As capacitor starts charging, the voltage at base of Q_2 rises exponentially as discussed earlier, towards V_{CC}. This continues till V_{B2} becomes equal to cut in voltage V_γ at $t = T$.

Waveforms for t > T : At $t = T$, reverse transition occurs. Thus Q_1 is cut-off and Q_2 starts conducting at $t = T^+$. Thus V_{C2} drops instantly to $V_{CE}(sat)$ and V_{B1} returns to V_F. The voltage V_{C1} rises abruptly as Q_1 becomes OFF. This rise is such that V_{C1} becomes almost equal to V_{CC}.

Now this sudden increase in V_{C1} is applied to base of Q_2 and Q_2 suddenly gets driven into saturation. Hence at $t = T^+$ an overshoot occurs at base of Q_2, in V_{B2}. This overshoot decreases exponentially as the capacitor C recharges because of base current.

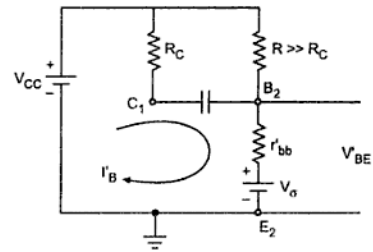


Fig. 3.17

Magnitude of the overshoot in V_{B2} : The equivalent circuit at $t = T^+$ is shown in the Fig. 3.17. In this circuit, the input circuit of Q_2 is replaced by base spreading resistance r'_{bb} in series with the base saturation voltage V_σ.

The base current at $t = T^+$ is denoted as I'_B while current through R is neglected as $R >> R_C$. From Fig. 3.17.

$$V'_{BE} = I'_B r'_{bb} + V_\sigma \quad \ldots (22)$$

$$V_{C1} = V_{CC} - I'_B R_C \quad \ldots (23)$$

Thus the **overshoot** at $t = T^+$ in the voltage V_{B2} is now can be denoted as δ and is given by,

$$\delta = V'_{BE} - V_\gamma = \text{Overshoot}$$

$$\therefore \quad \boxed{\delta = I'_B r'_{bb} + V_\sigma - V_\gamma} \quad \ldots (24)$$

While the overshoot in the collector voltage of Q_1 i.e. in V_{C1} is denoted as δ' and given by,

$$\delta' = V_{C1} - V_{CE}(sat)$$

$$\therefore \quad \boxed{\delta' = V_{CC} - I'_B R_C - V_{CE}(sat)} \quad \ldots (25)$$

But the voltage V_{C1} is applied to base of Q_2.

Key Point : *Hence the overshoots δ and δ' must be same.*

Equating (24) and (25) we get,

$$I'_B r'_{bb} + V_\sigma - V_\gamma = V_{CC} - I'_B R_C - V_{CE}(sat)$$

$$\therefore \quad I'_B (R_C + r'_{bb}) = V_{CC} - V_{CE}(sat) - V_\sigma + V_\gamma$$

$$\therefore \quad \boxed{I'_B = \frac{V_{CC} - V_{CE}(sat) - V_\sigma + V_\gamma}{R_C + r'_{bb}}} \quad \ldots (26)$$

After $t = T^+$, the V_{B2} decreases exponentially to its steady state value V_σ. The time constant with which it decays is given by,

$$\therefore \quad \boxed{\tau' = (R_C + r'_{bb})\, C} \quad \ldots (27)$$

Note that if V_{CC} is large compared with the junction voltages, then

$$\therefore \quad \boxed{I_B' \approx \frac{V_{CC}}{R_C}} \qquad \text{if } V_{CC} \text{ is large.} \qquad \ldots (28)$$

Similar to overshoot in V_{C1} and V_{B2}, there exists an undershoot in V_{C2} and V_{B1} at $t = T^+$ but these undershoots are very small and hence usually neglected and not shown in the waveforms.

The complete waveforms considering above discussion are shown in the Fig. 3.18.

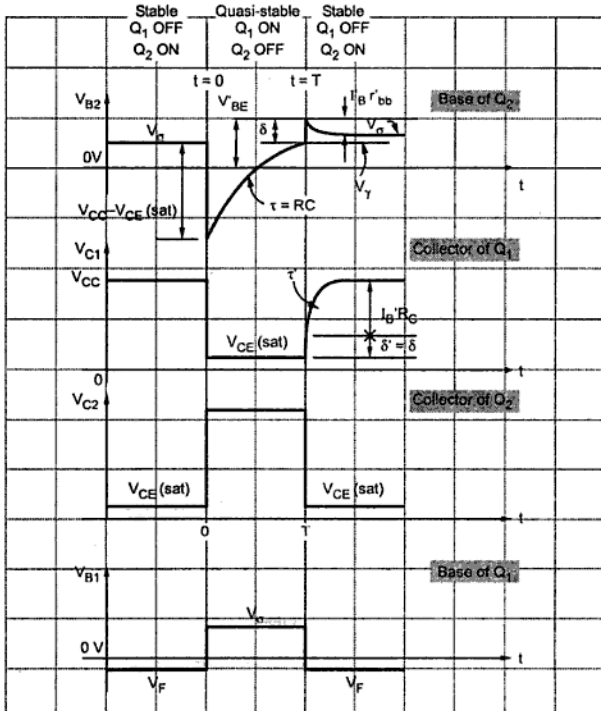


Fig. 3.18 Waveforms of collector coupled monostable multivibrator

The typical npn transistor junction voltages at 25 °C are given in Table 3.1. The table may be referred if the voltages are not given in the problem. All the voltages are in volts.

	V_{CE} (sat)	V_{BE} (sat) = V_σ	V_{BE} (active)	V_{BE} (cut-in) = V_γ	V_{BE} (cut-off)
Si	0.3	0.7	0.6	0.5	0.0
Ge	0.1	0.3	0.2	0.1	– 0.1

Table 3.1

Example 3.3 : *Calculate the component values of a monostable multivibrator using silicon npn transistors, developing an output pulse of 120 μsec duration. Assume* $(h_{fe})_{min} = 20$, $I_C(sat) = 6$ *mA,* $V_{CC} = 6$ *V and* $V_{BB} = -1.5$ *V. If* $r'_{bb} = 150\ \Omega$, *calculate the magnitude of the overshoot.*

Solution : Assume Q_2 ON and Q_1 in OFF condition.

$$\therefore \quad I_{C2} = I_C(sat) = 6 \text{ mA}$$

$$\text{Now} \quad I_{C2} = \frac{V_{CC} - V_{CE}(sat)}{R_C} \quad \ldots (1)$$

For the silicon npn transistors,

$$V_{CE}(sat) = 0.3 \text{ V}, \ V_{BE}(sat) = V_\sigma = 0.7 \text{ V}$$

$$V_{BE}(\text{cut-in}) = V_\gamma = 0.5 \text{ V}$$

$$\therefore \quad 6 = \frac{6 - 0.3}{R_C}$$

$$\therefore \quad R_C = 0.95 \text{ k}\Omega = 950\ \Omega$$

$$(I_{B2})sat = \frac{I_C(sat)}{(h_{fe})_{min}} = \frac{6}{20}$$

$$= 0.3 \text{ mA}$$

$$\therefore \quad (I_{B1})sat = 0.3 \text{ mA}$$

$$\text{Now} \quad I_{B2} = \frac{V_{CC} - V_{BE}(sat)}{R}$$

$$\therefore \quad 0.3 = \frac{6 - 0.7}{R}$$

$$\therefore \quad R = 17.67 \text{ k}\Omega$$

In quasi-stable state, Q_1 is ON and Q_2 is OFF.

$$T = 0.69 \text{ RC}$$

$$\therefore \quad 120 \times 10^{-6} = 0.69 \times 17.67 \times 10^3 \text{ C}$$

$$\therefore \quad C = 9.84 \text{ nF}$$

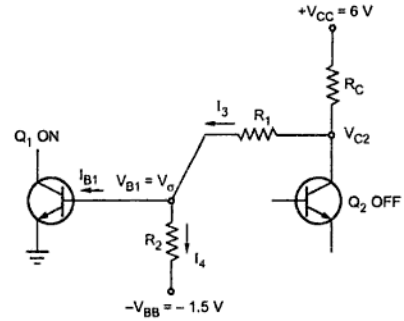


Fig. 3.19

Consider the equivalent circuit in quasi-stable state (See Fig. 3.19).

As Q_2 is OFF, $V_{C2} = V_{CC}$

$$\therefore \quad I_3 = \frac{V_{CC} - V_\sigma}{R_1} = \frac{6 - 0.7}{R_1} = \frac{5.3}{R_1} \qquad \ldots (2)$$

and $$I_4 = \frac{V_\sigma - V_{BB}}{R_2} = \frac{0.7 - (-1.5)}{R_2} = \frac{2.2}{R_2} \qquad \ldots (3)$$

Assume $$I_4 = (I_{B1})\text{sat} = 0.3 \text{ mA} \qquad \ldots (4)$$

$$\therefore \quad R_2 = \frac{2.2}{0.3} = 7.33 \text{ k}\Omega$$

and $$I_3 = I_4 + I_{B1} = 0.3 + 0.3 = 0.6 \text{ mA}$$

$$\therefore \quad R_1 = \frac{5.3}{0.6} = \mathbf{8.833 \text{ k}\Omega}$$

The speed-up capacitor C_1 can be chosen such that $R_1 C_1 = 1$ μsec hence

$$C_1 = \frac{1 \times 10^{-6}}{8.833 \times 10^3} = 113.21 \text{ pF}$$

Now $$I'_B = \frac{V_{CC} - V_{CE}(\text{sat}) - V_\sigma + V_\gamma}{R_C + r'_{bb}} = \frac{6 - 0.3 - 0.7 + 0.5}{950 + 150} = 5 \text{ mA}$$

$$\therefore \quad \delta = \text{Overshoot} = I'_B r'_{bb} + V_\sigma - V_\gamma$$

$$= 5 \times 10^{-3} \times 150 + 0.7 - 0.5$$

$$= \mathbf{0.95 \text{ V}}$$

3.4.3 Applications

The applications of monostable multivibrator are :

1) Used to produce rectangular waveform and hence can be used as gating circuit.

2) Used to introduce time delays as gate width is adjustable.

3) Used to generate uniform width pulses from a variable width input pulse train.

3.5 Emitter Coupled Monostable Multivibrator

The Fig. 3.20 shows emitter coupled monostable multivibrator.

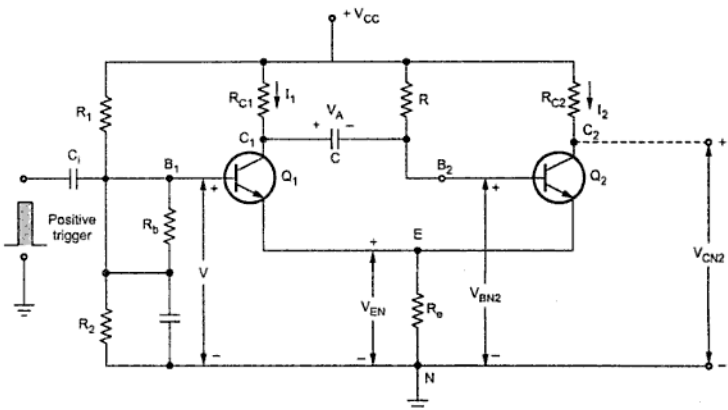


Fig. 3.20 Emitter coupled monostable multivibrator

The emitter terminals of both the transistors are coupled together hence called emitter coupled. The connection from collector C_2 to the base B_1 is absent. The feedback is provided through a common emitter resistance R_e. A negative supply is not required.

Key Point : *As collector C_2 is not involved in the regenerative loop, it is ideal to take output voltage from this terminal.*

The input trigger is connected to terminal B_1, which is also not connected to any other point. Thus trigger input source cannot load the circuit.

In collector coupled monoshot, I_1 controls the gate width T but it is not possible to maintain I_1 stable. But in the emitter coupled monoshot, I_1 can be stabilized with emitter resistance R_e. Hence perfect control of T with I_1 can be achieved. This is possible because when Q_2 goes OFF, Q_1 goes ON and operates with sufficient emitter resistance.

The I_1 inturn can be controlled by biasing voltage V and it is observed that T **varies linearily with V.**

Key Point : *Thus emitter coupled monoshot is used as a perfect gate wave generator whose gate width can be controlled easily and linearily with the help of an electric signal.*

3.5.1 Waveforms

The waveform at the emitters is more important in this monoshot. Consider the mode of operation with Q_1 cut-off and Q_2 in saturation in the stable state.

In the stable state Q_1 is OFF and Q_2 is ON. The Q_2 is in saturation. It derives base drive from V_{CC} and resistance R. Due to its emitter current, it produces a voltage V_{EN2} across the resistance R_e. This voltage is more than the base potential of Q_1 which ensures that Q_1 remains OFF.

When the positive trigger is applied to the base of Q_1, then V_{B1} becomes more than V_{EN2} which drives Q_1 into conduction. Due to this, the collector voltage of Q_1 drops by $I_1 R_{C1}$. This negative step is applied to the base of Q_2 which makes Q_2 OFF. The capacitor C now charges through R from V_{CC} through ON transistor Q_1. The ON Q_1 developes potential drop of V_{EN1} across R_e. This is the **quasi-stable state** with Q_1 ON and Q_2 OFF.

As the capacitor charges, the base B_2 of Q_2 becomes more positive. When the potential V_{BN2} becomes more than $V_{EN1} + V_\gamma$ then the transistor Q_2 starts conducting. Due to the regenerative feedback, Q_2 goes into saturation while Q_1 is cut-off. Thus the stable state with Q_1 OFF and Q_2 ON is achieved.

The waveforms are as shown in the Fig. 3.21.

Refer Fig. 3.21 on next page.

3.5.2 Extreme Limits of V

In stable state Q_1 must be OFF. Hence there is a limit V_{max} for bias voltage V to be applied to base of Q_1.

While when Q_1 is ON, then $I_{C1} R_{C1}$ drop must be large so as to cut-off Q_2. This puts a minimum limit V_{min} for bias voltage V.

Key Point : *The bias voltage V must be between V_{max} and V_{min}, for proper operation of the circuit.*

For Q_1 OFF in stable state, $V_{EN2} > V_{\gamma 1}$.

$$\therefore \quad \boxed{V_{max} = V_{EN2} + V_{\gamma 1}} \qquad \ldots (1)$$

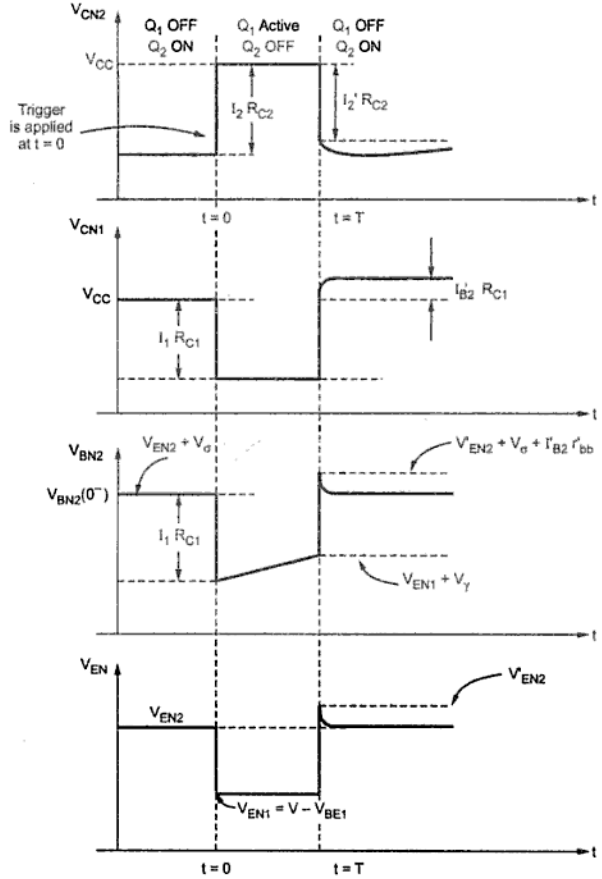


Fig. 3.21 Waveforms of emitter coupled monostable multivibrator

While for having minimum I_1 to cut-off Q_2 in quasi-stable state, V_{min} is given by,

$$V_{min} = (V_{EN1})_{min} + V_{BE1} \quad \text{... (2)}$$

This equation (2), further can be rearranged as,

$$V_{min} = V_{BE1} + \frac{V_{BN2}(0^-) - V_{\gamma 2} + (R_{C1}/R)(V_{CC} - V_{\gamma 2})}{1 + \left(\frac{R_{C1}}{R}\right) + \left(\frac{R_{C1}}{R_e}\right)[h_{FE}/(1+h_{FE})]} \quad \text{... (3)}$$

3.5.3 Gate Width of Emitter Coupled Monoshot

The expression of gate width can be derived using the basic relation,

$$V_C = V_f + (V_i - V_f)\, e^{-t/\tau} \quad \text{... (1)}$$

The voltage V_{BN2} just after trigger is applied is given by,

$$V_{BN2}(0^+) = V_{BN2}(0^-) - I_1 R_{C1} \quad \text{... (2)}$$

If Q_2 did not conduct, V_{BN2} would approach V_{CC}.

$\therefore$ v_{BN2} = Instantaneous voltage at B_2

$$\therefore \quad v_{BN2} = V_{CC} - [V_{CC} - V_{BN2}(0^-) + I_1 R_{C1}]\, e^{-t/\tau} \quad \text{... (3)}$$

where $\tau = C(R + R_{C1})$

At $t = T^-$, just before pulse ends,

$$v_{BN2} = V_{EN1} + V_{\gamma 2} \quad \text{... (4)}$$

Equating equations (3) and (4),

$$V_{EN1} + V_{\gamma 2} = V_{CC} - [V_{CC} - V_{BN2}(0^-) + I_1 R_{C1}]\, e^{-t/\tau} \quad \text{... } t = T$$

Solving for T, the gate width is obtained as,

$$T = \tau \ln \left\{ \frac{V_{CC} - V_{BN2}(0^-) + I_1 R_{C1}}{V_{CC} - V_{EN1} - V_{\gamma 2}} \right\} \quad \text{... (5)}$$

Key Point : *This time T varies linearily with the bias voltage V. Due to this feature, it can be used as voltage to time converter.*

3.6 Triggering of Monostable Multivibrator

The collector coupled monostable is triggered with the pulses of such polarity that the nonconducting transistor is brought out of cut-off. But as mentioned earlier in the triggering of bistable, this method has certain disadvantages. Hence in practice the pulses are selected of that polarity which turns the ON transistor OFF.

Key Point : *Thus for npn transistor circuit, negative pulses are selected while for pnp transistor circuit, positive pulses are selected.*

The triggering arrangement for collector coupled npn monostable multivibrator is shown in the Fig. 3.22.

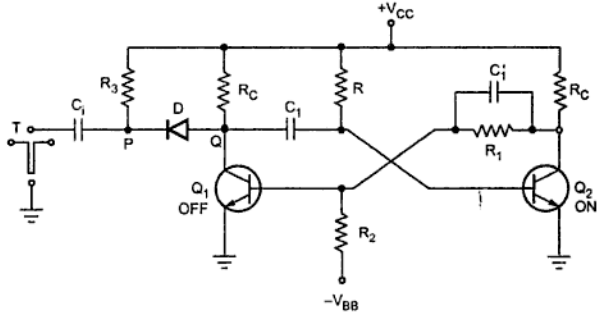


Fig. 3.22 Triggering of monostable multivibrator

The negative pulse is applied through input capacitor C_i and the diode D. It is known that the sensitivity of the npn circuit is more to the negative pulses, so as to make the ON transistor OFF. The normal stable state is Q_2 ON and Q_1 OFF.

The diode D is at zero bias as Q_1 is OFF and the points P and Q are equipotential. When negative pulse is applied, the diode D conducts and acts as short circuit. This passes the negative pulse to the base of Q_2 which is ON. This decreases Q_2 current and due to regenerative action Q_1 gets driven to saturation and Q_2 becomes OFF. This is quasi-stable state. The advantage of the circuit is that during quasi-stable state, due to drop across R_C, the diode D is maintained reverse biased and multivibrator cannot respond to any triggering signal until quasi-stable state is completed. During this state, C_1 charges through R and Q_1, towards V_{CC}. This rises the base voltage of Q_2. At one instant, this voltage becomes more than cut-in voltage of Q_2 and its starts conducting. Hence due to the regenerative action automatically Q_1 becomes OFF and Q_2 ON. Thus circuit returns back to its normal stable state.

Key Point : *The circuit is very effective when trigger input is a continuous waveform such as a sine wave instead of short trigger.*

3.7 Collector Coupled Astable Multivibrator

As mentioned earlier, the astable multivibrator has two states, both are quasi-stable. None of the states is stable. And without external trigger, multivibrator keeps on alternating the states. It cannot remain indefinitely in any of these two states.

The Fig. 3.23 shows the collector coupled astable multivibrator circuit.

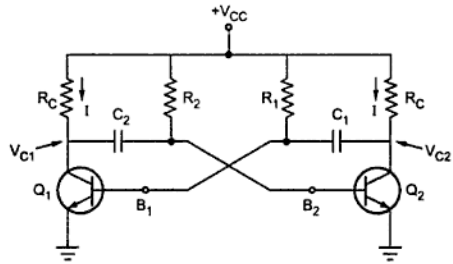


Fig. 3.23 Collector coupled astable multivibrator

The Q_1 and Q_2 are identical npn transistors. The two collector resistances are equal to R_C. The collector Q_1 is coupled to the base of Q_2 through capacitor C_2 while the collector of Q_2 is coupled to the base of Q_1 through capacitor C_1. The capacitive coupling is used between the stages, due to which neither transistor can remain permanently cut-off.

Key Point : *The circuit has two quasi-stable states and it makes periodic switching between these states, without any external trigger signal.*

At start, to understand the working, assume that the state is Q_2 ON and Q_1 OFF. The capacitor C_2 starts charging towards V_{CC} through path R_C, C_2 and ON Q_2. Thus finally voltage across C_2 becomes equal to V_{CC} with proper polarity.

At the same time capacitor C_1 which is charged to V_{CC} in the earlier state, starts discharging through path Q_2, V_{CC}, R_1, C_1. The paths for charging of C_2 and discharging of C_1 are shown in the Fig. 3.24 (a) and (b).

The base of Q_1 is at $-V_{CC}$ at the beginning. But as C_1 starts discharging, it becomes less and less negative i.e. becomes more positive. Finally it becomes equal to V_γ, the cut-in voltage of transistor Q_1. When it becomes just greater than V_γ, the transistor Q_1 starts conducting. So Q_1 becomes ON and at the same time Q_2 becomes OFF. The negative potential applied at B_2, due to charged C_2 ensures that Q_2 becomes indeed OFF.

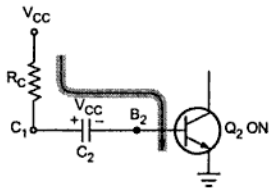


Fig. 3.24 (a)

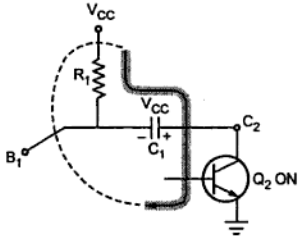


Fig. 3.24 (b)

When this happens, the capacitor C_1 starts charging again through R_C, C_1 and ON transistor Q_1. While C_2 starts discharging, through the path V_{CC}, R_2, C_2 and ON transistor Q_1. Both the paths are shown in the Fig. 3.25 (a) and (b).

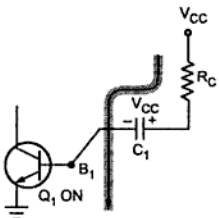


Fig. 3.25 (a)

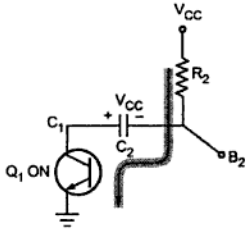


Fig. 3.25 (b)

As C_2 discharges, B_2 potential becomes less negative i.e. it increases towards positive. When V_{B2} becomes just greater than cut-in voltage V_γ of Q_2, the Q_2 starts conducting. Thus now Q_2 becomes ON and Q_1 OFF. Thus the changes in the two states is automatic and without any external triggering signal.

3.7.1 Waveforms of Astable Multivibrator

Let us see the waveforms at the collectors of Q_1 and Q_2. When Q_1 is OFF and Q_2 is ON, the C_1 discharges and voltage at B_1 i.e. V_{B1} increases. This increases exponentially with the time constant R_1C_1. This voltage was initially at $-V_{CC}$. When this voltage increases beyond cut-in voltage of Q_1, Q_1 starts conducting. When Q_1 is in saturation,

$\therefore$

$$V_{B1} = V_{BE}(sat)$$
$$V_{C1} = V_{CE}(sat)$$

and

$$V_{C2} = V_{CC}$$

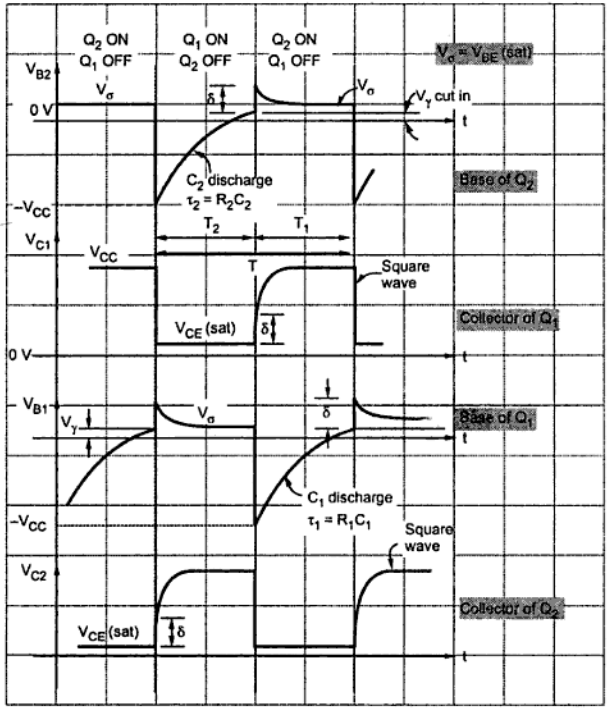


Fig. 3.26 Waveforms of collector coupled astable multivibrator

When Q_1 is ON and Q_2 is OFF, the C_2 discharges and voltage at B_2 i.e. V_{B2} increases. This increases exponentially with the time constant R_2C_2. This voltage was initially at $-V_{CC}$ in the previous state. When this voltage increases beyond cut-in voltage of Q_2, Q_2 conducts and goes in saturation.

$\therefore$ $V_{B2} = V_{BE}(sat),\ V_{C2} = V_{CE}(sat)$

and $V_{C1} = V_{CC}$

The waveforms are shown in the Fig. 3.26. See Fig. 3.26 on previous page.

The analytical expression for δ is same as derived earlier for monostable multivibrator given by equation (24). While the base current I_B' at the overshoot is given by equation (26).

Key Point : *For pnp transistors, polarity of V_{CC} gets reversed and all the waveforms are inverted compared to those shown in the Fig. 3.26.*

3.7.2 Expression for Time Period T

For deriving the expression for time period T which is $T_1 + T_2$, consider the waveform at the base of any transistor as shown in the Fig. 3.27.

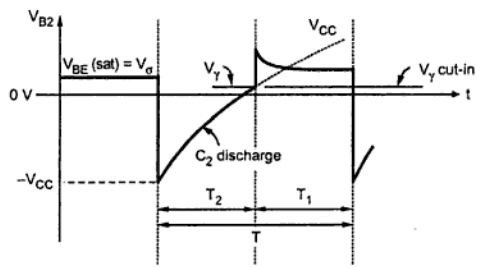


Fig. 3.27

The capacitor C_2 discharges exponentially and the voltage V_{B2} increases exponentially.

$$V_i = \text{Initial value of } V_{B2} = -V_{CC} \quad \ldots (1)$$

$$V_f = \text{Final value of } V_{B2} = +V_{CC} \quad \ldots (2)$$

Though it stops increasing beyond V_γ(cut-in) voltage, its rise is towards $+V_{CC}$, which is its final steady state value, with the time constant $\tau_2 = R_2C_2$.

For the capacitor we can write the basic equation as,

$$V_o = V_f - (V_f - V_i)\, e^{-t/\tau} \quad \ldots \text{(Basic equation)}$$

Here V_o means the base voltage,

$$\therefore \quad V_{B2} = V_{CC} - (V_{CC} - (-V_{CC}))\, e^{-t/R_2C_2} \quad \ldots (3)$$

$$\therefore \quad V_{B2} = V_{CC} - 2\, V_{CC}\, e^{-t/R_2C_2}$$

$$\therefore \quad V_{B2} = V_{CC}\,(1 - 2\, e^{-t/R_2C_2}) \quad \ldots(4)$$

We know that at switching time,

$$\boxed{t = T_2 \text{ and } V_{B2} = V_\gamma} \quad \ldots(5)$$

Substituting in equation (4),

$$V_\gamma = V_{CC}\,(1 - 2\, e^{-T_2/R_2C_2}) \quad \ldots (6)$$

The best approximation to obtain T_2 is, $V_\gamma = 0$ V

$$\therefore \quad 0 = V_{CC}\,(1 - 2\, e^{-T_2/R_2C_2})$$

$$\therefore \quad 1 - 2\, e^{-T_2/R_2C_2} = 0$$

$$\therefore \quad e^{-T_2/R_2C_2} = 0.5$$

$$\therefore \quad ln\,(e^{-T_2/R_2C_2}) = ln\,(0.5)$$

$$\therefore \quad \frac{-T_2}{R_2\, C_2} = -0.69$$

$$\therefore \quad \boxed{T_2 = 0.69\, R_2\, C_2} \quad \ldots(7)$$

Similarly we can write the equation at $t = T_1$ and find out the expression for T_1 which same as for T_2.

$$\therefore \quad \boxed{T_1 = 0.69\, R_1C_1} \quad \ldots(8)$$

$$\therefore \quad T = T_1 + T_2$$

$$\therefore \quad T = 0.69\,(R_1C_1 + R_2C_2) \quad \ldots (9)$$

if $R_1 = R_2 = R$ and $C_1 = C_2 = C$ then

$$\boxed{T = 0.69\,(2\, RC) = 1.38\, RC} \quad \ldots(10)$$

Key Point : *For this case, we get the square wave at the output which is symmetrical.*

3.7.3 Distortion and its Elimination

It can be seen that, in the collector waveforms shown in the Fig. 3.28, there is certain distortion present. Instead of exact square wave, we are getting the vertical rising edges little bit rounded. This is called **rounding**. For square wave output such a rounding is undesirable and must be eliminated.

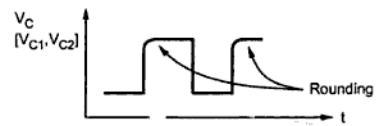


Fig. 3.28 Rounding in collector waveforms

Such a rounding can be eliminated to obtain the vertical edges square wave by adding two collector diodes and two resistors. The collector coupled astable multivibrator with collector diodes and auxiliary resistors is shown in the Fig. 3.29.

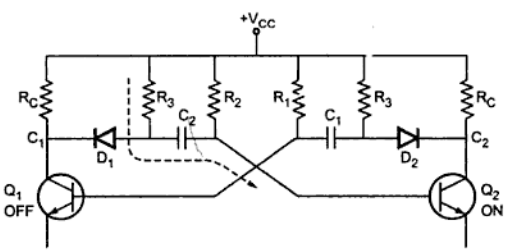


Fig. 3.29 Elimination of distortion

If Q_1 is OFF, then its collector voltage increases suddenly to V_{CC} thus making D_1 reverse biased. Thus the charging of C_2 now takes place through R_3 rather than R_C. As current does not flow through R_C, the collector voltage can rise suddenly to V_{CC} and the rounding at the collector completely gets eliminated. This is shown in the Fig. 3.30.

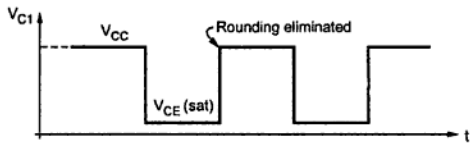


Fig. 3.30 Elimination of rounding

Example 3.4 : *If an astable multivibrator is used to generate square wave using the component values as $C_1 = C_2 = 100$ pF and $R_1 = R_2 = 10$ kΩ, calculate the pulse width, period and frequency of output.*

Solution : The components are,

$$C_1 = C_2 = C = 100 \text{ pF}$$

$$R_1 = R_2 = 10 \text{ k}\Omega$$

$$\therefore \quad T_1 = T_2 = 0.69 \text{ RC} = 0.69 \times 10 \times 10^3 \times 100 \times 10^{-12}$$

$$= \mathbf{0.69\ \mu sec}$$

$$\therefore \quad \text{Period} = T = T_1 + T_2 = 2 \times 0.69$$

$$= 1.38\ \mu\text{sec}$$

$$\therefore \quad f = \frac{1}{T} = \frac{1}{1.38}$$

$$= \mathbf{0.7246\ MHz}$$

3.7.4 Applications

The various applications of astable multivibrator are :

1) Used as a square wave generator, voltage to frequency converter etc.

2) Used as a clock for binary logic signals.

3) Used in the digital voltmeter and switched mode power supplies.

4) As an oscillator to generator wide range of audio and radio frequencies.

3.8 Emitter Coupled Astable Multivibrator

The Fig. 3.31 shows the emitter coupled astable multivibrator circuit, using n-p-n transistors.

It uses both n-p-n transistors, shown as Q_1 and Q_2. For the simplification of analysis, three different power supplies V_{BB}, V_{CC1} and V_{CC2} are shown in the circuit. The collector of Q_1 is connected to the base of Q_2. The capacitive coupling is used to connect emitters of

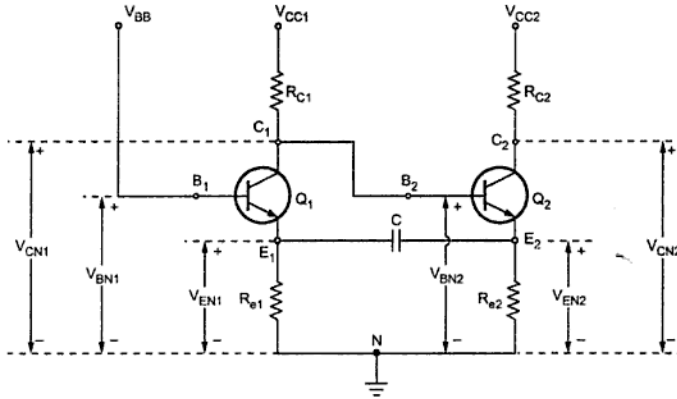


Fig. 3.31 Emitter coupled astable multivibrator

Q_1 and Q_2. Additional resistances R_{e1} and R_{e2} are used in the emitter leg of Q_1 and Q_2 respectively. The circuit has two quasi-stable states and it makes periodic switching between these states, without any external signal.

3.8.1 Operation and Mathematical Analysis

To understand the working, assume that the Q_1 switches between cut-off and saturation while Q_2 switches between cut-off and active region.

Assume that initially Q_1 is ON and Q_2 is OFF and the transition of states is going to occur at $t = t_1$.

So at $t = t_1^-$ i.e. just before the time of transition we can write,

$$V_{CN2}(t_1^-) = V_{CC2} \text{ as } Q_2 \text{ OFF} \quad \text{... (1)}$$

$$V_{EN1}(t_1^-) = V_{BB} - V_{BE}(\text{sat}) \text{ as } Q_1 \text{ saturation}$$

$$= V_{BB} - V_\sigma \quad \text{... (2)}$$

where V_σ = Base saturation voltage

$$V_{CN1}(t_1^-) = V_{BN2}(t_1^-) \text{ as } C_1 \text{ and } B_2 \text{ are joined}$$

$$= V_{EN1} + V_{CE}(\text{sat}) \quad \text{... (3)}$$

Using equation (2) in equation (3), $V_{CN1}(t_1^-) = V_{BB} - V_\sigma + V_{CE}(\text{sat})$ ... (4)

During the interval before $t = t_1$, the capacitor C charges from a fixed voltage of E_1 i.e. $V_{BB} - V_\sigma$ through resistor R_{e2} as shown in the Fig. 3.32.

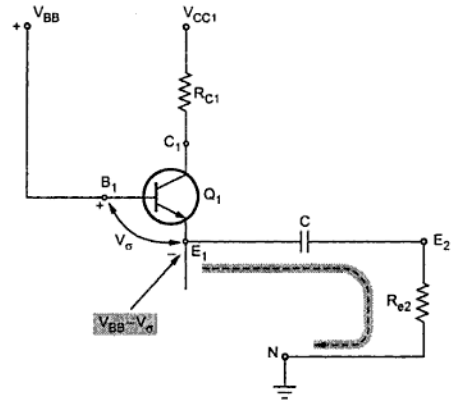


Fig. 3.32 Capacitor charging before $t = t_1$

As capacitor charges, all the voltages except V_{EN2} remain constant. Because as capacitor charges, the capacitor current decreases and V_{EN2} falls.

So finally at $t = t_1^-$ when V_{EN2} falls by cut-in voltage of Q_2 we get,

$$V_{EN2}(t_1^-) = V_{BN2} - V_\gamma \quad \ldots (5)$$

where V_γ = Cut-in voltage (V_{BE} cut-in) of the transistor

$$\therefore \quad V_{EN2}(t_1^-) = V_{CN1} - V_\gamma \quad \text{as} \quad V_{BN2} = V_{CN1}$$

$$\therefore \quad V_{EN2}(t_1^-) = V_{BB} - V_\sigma + V_{CE}(\text{sat}) - V_\gamma \quad \ldots (6)$$

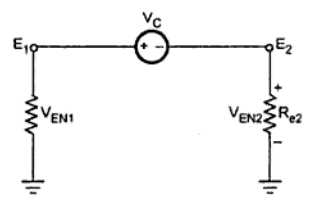


Fig. 3.33

Thus at $t = t_1$, the transition takes place and Q_2 starts conducting due to reduced voltage of E_2 with respect to B_2, because of which base-emitter junction of Q_2 becomes forward biased. Hence current through R_{e2} increases hence V_{EN2} increases.

Now the capacitor voltage cannot change instantaneously. So at $t = t_1$, it can be replaced by a voltage source as shown in the Fig. 3.33.

Thus as V_{EN2} increases, the capacitor voltage gets added to V_{EN2} and hence V_{EN1} also increases. This reduces the forward biasing of B-E junction of Q_1 and Q_1 comes out of saturation.

When Q_1 comes out of saturation, collector current decreases and hence V_{CN1} increases. But $V_{CN1} = V_{BN2}$ hence V_{BN2} increases. This further strengthens the forward biasing of B-E junction of Q_2 hence current in Q_2 increases. The design of the circuit is such that, this action is regenerative which drives Q_1 OFF and Q_2 into active region. Q_2 does not get driven to saturation.

Let V_{BE2} = Base emitter voltage of Q_2 in active region

I_{B2} = Base current of Q_2 in active region

I_{C2} = Collector current of Q_2 in active region

Hence just after transition i.e. at $t = t_1^+$ we can write,

$$V_{CN2}(t_1^+) = V_{CC2} - I_{C2} R_{C2} \quad \ldots (7)$$

$$V_{CN1}(t_1^+) = V_{BN2}(t_1^+) = V_{CC1} - I_{B2} R_{C1} \quad \ldots (8)$$

This is because the base current of Q_2 is supplied by the collector of Q_1.

$$V_{EN2}(t_1^+) = V_{BN2}(t_1^+) - V_{BE2}(t_1^+)$$

$$\therefore \quad V_{EN2}(t_1^+) = V_{CC1} - I_{B2} R_{C1} - V_{BE2} = V_{EN1}(t_1^+) \quad \ldots (9)$$

So at transition $t = t_1$, there is abrupt change in V_{EN2} of V_D say. The same is the instantaneous change in V_{EN1} because capacitor voltage cannot change instantaneously. These characteristics are indicated in the waveforms shown in the Fig. 3.34. See Fig. 3.34 on next page.

From the waveforms,

$$V_D = V_{EN1}(t_1^+) - V_{EN1}(t_1^-) = V_{EN2}(t_1^+) - V_{EN2}(t_1^-) \quad \ldots (10)$$

$$\therefore \quad V_{EN1}(t_1^+) = V_{EN2}(t_1^+) - V_{EN2}(t_1^-) + V_{EN1}(t_1^-) \quad \ldots (11)$$

Using equations (9), (6) and (2) we get,

$$V_{EN1}(t_1^+) = V_{CC1} - I_{B2} R_{C1} - V_{BE2} - V_{BB} + V_\sigma - V_{CE}(sat) + V_\gamma + V_{BB} - V_\sigma$$

$$\therefore \quad \boxed{V_{EN1}(t_1^+) = V_{CC1} - I_{B2} R_{C1} - V_{BE2} - V_{CE}(sat) + V_\gamma \approx V_1} \quad \ldots (12)$$

This is assumed to be say V_1.

As Q_2 is in the active region we can write,

$$I_{C2} = h_{FE} I_{B2} \quad \ldots (13)$$

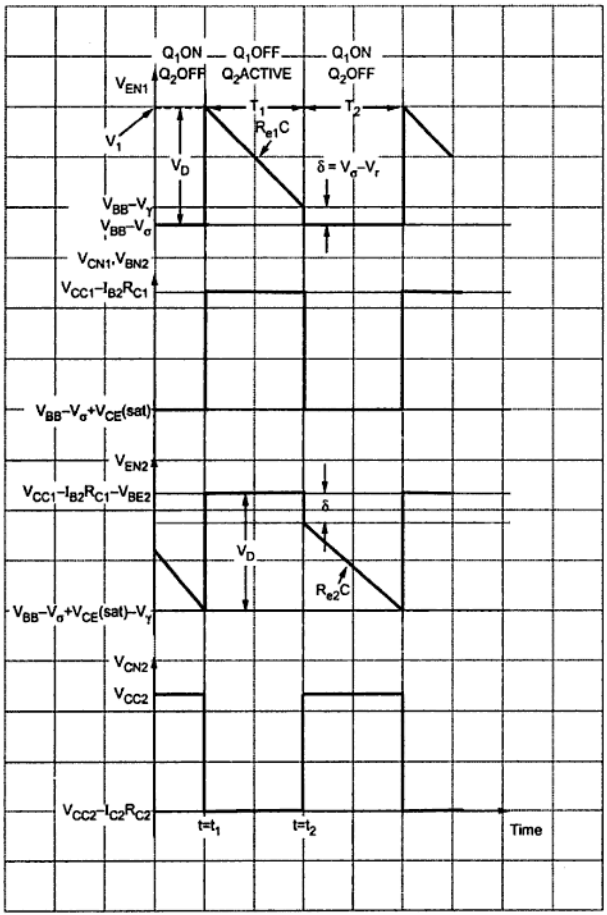


Fig. 3.34 Waveforms of emitter coupled astable multivibrator

To obtain I_{C2}

To obtain the expression for I_{C2}, neglect all the saturation voltages and all transistor junction voltages. Also neglect the drop $I_{B2} R_{C1}$ as I_{B2} is very very small as compared to V_{CC1}.

$$\therefore \quad V_{EN1}(t_1^+) = V_{EN2}(t_1^+) = V_{CC1} \qquad \text{... (14)}$$

Thus at $t = t_1^+$, the current through R_{e1} is

$$I_{e1} = \frac{V_{EN1}(t_1^+)}{R_{e1}} = \frac{V_{CC1}}{R_{e1}} \qquad \text{... (15)}$$

And the current in R_{e2} is,

$$I_{e2} = \frac{V_{EN2}(t_1^+)}{R_{e2}} = \frac{V_{CC1}}{R_{e2}} \qquad \text{... (16)}$$

The capacitor voltage cannot change instantaneously so at $t = t_1^+$ it acts as a short circuit. Q_1 is OFF and hence both I_{e1} and I_{e2} are supplied by Q_2 only as shown in the Fig. 3.35.

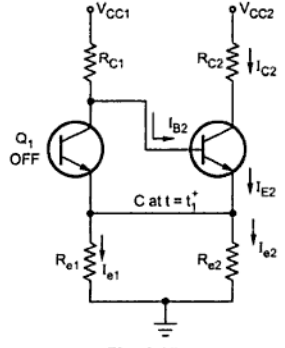


Fig. 3.35

It can be seen that at $t = t_1^+$ effectively both R_{e1} and R_{e2} appear in parallel hence we can write,

$$I_{C2} = I_{E2} = I_{e1} + I_{e2} = V_{CC1}\left[\frac{1}{R_{e1}} + \frac{1}{R_{e2}}\right]$$

$$\therefore \quad \boxed{I_{C2} = \frac{V_{CC1}}{R_e}} \qquad \text{where } R_e = R_{e1} \parallel R_{e2} \qquad \text{... (17)}$$

$$\therefore \quad \boxed{I_{B2} \simeq \frac{V_{CC1}}{h_{FE}\, R_e}} \qquad \ldots (18)$$

3.8.2 Expression for Time Period

As shown in the waveforms, the period T_1 ends at $t = t_2$. So at $t = t_2$, Q_1 will be ON and Q_2 will be OFF. This happens when B-E junction of Q_1 becomes forward biased. So emitter voltage of Q_1 must reduce by cut-in voltage with respect to base voltage of Q_1, to turn it ON.

$$\therefore \quad V_{EN1}\left(t_2^-\right) = V_{BB} - V_\gamma \qquad \ldots (19)$$

And as Q_1 goes into saturation, the V_{EN1} voltage goes on decreasing as base voltage of Q_1 is fixed. This drop in V_{EN1} at $t = t_2$ is equal to δ as shown in the waveforms. Similar drop will be therein V_{EN2} at $t = t_2$, because emitters are capacitively connected and capacitor voltage cannot change instantaneously.

After $t = t_2$ i.e. in the interval T_2, the conditions of the transistors and voltages is same as it was for $t < t_1$. Thus the cycle repeats and the circuit acts as an astable multivibrator.

It can be seen from the waveform that at $t = t_1$, there is rise in V_{EN1} and then V_{EN1} decreases as capacitor discharges from V_1 towards zero exponentially through R_{e1}. So discharge time constant is $R_{e1}\, C$. The voltage attained by the capacitor is $V_{BB} - V_\gamma$ at which Q_1 is ON again i.e. at T_1.

From the basic capacitor equation,

$$V_C = V_f - (V_f - V_i)\, e^{-t/T}$$

Here $V_C = V_{BB} - V_\gamma$, $t = T_1$, $V_f = 0$, $V_i = V_1$

$$\therefore \quad V_{BB} - V_\gamma = 0 - (0 - V_1)\, e^{-T_1/R_{e1}\, C}$$

$$\therefore \quad e^{-T_1/R_{e1}\, C} = \frac{V_{BB} - V_\gamma}{V_1}$$

$$\therefore \quad -\frac{T_1}{R_{e1}\, C} = ln\left(\frac{V_{BB} - V_\gamma}{V_1}\right)$$

$$\therefore \quad \frac{T_1}{R_{e1}\, C} = ln\left(\frac{V_1}{V_{BB} - V_\gamma}\right) \qquad \ldots \text{Absorbing negative sign}$$

$$\therefore \quad T_1 = R_{e1}\, C\, ln\left[\frac{V_1}{V_{BB} - V_\gamma}\right] \qquad \ldots (20)$$

Assuming that supply voltages are large compared to junction voltages and neglecting $I_{B2}\, R_{C1}$ as $I_{B2}\, R_{C1} << V_{CC1}$ we can obtain,

$$\therefore \quad \boxed{T_1 = R_{e1}\, C\, ln\left(\frac{V_{CC1}}{V_{BB}}\right)} \qquad \text{... (21)}$$

Similarly T_2 can be obtained with same approximations as,

$$\therefore \quad \boxed{T_2 = R_{e2}\, C\, ln\frac{V_{CC1}}{V_{BB}}} \qquad \text{... (22)}$$

$$\therefore \quad \boxed{T = T_1 + T_2 = (R_{e1} + R_{e2})\, C\, ln\left(\frac{V_{CC1}}{V_{BB}}\right)} \qquad \text{... (23)}$$

and

$$\boxed{f = \frac{1}{T} = \frac{1}{(R_{e1} + R_{e2})\, C\, ln\left(\frac{V_{CC1}}{V_{BB}}\right)}} \qquad \text{... (24)}$$

Key Point : *It can be observed that the frequency is not dependent on transistor parameters.*

And if V_{CC1} and V_{BB} are selected such that they are proportional to each other then the frequency can be made insensitive to supply voltages.

3.8.3 Practical Emitter Coupled Astable Multivibrator

Practically instead of using three supply voltages, only single supply voltage V_{CC} is used. The circuit is modified using additional resistances as shown in the Fig. 3.36.

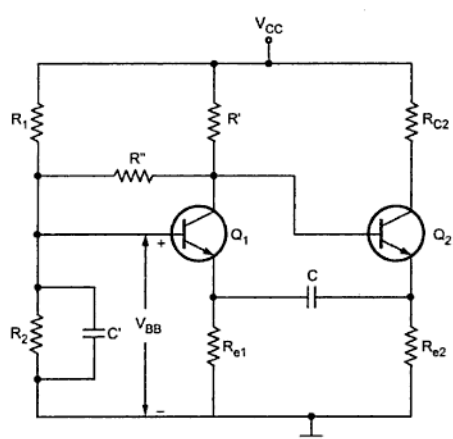


Fig. 3.36 Practical emitter coupled astable multivibrator

The voltage V_{BB} is obtained using potential divider of R_1 and R_2. So neglecting base current of Q_1 we can write,

$$V_{BB} = \frac{V_{CC}}{R_1 + R_2} \times R_2 \quad \text{... (25)}$$

The capacitor C′ is bypass capacitor and used to keep V_{BB} constant hence C′ will not appear any where in the mathematical analysis.

Using Thevenin's theorem it can be shown that the earlier circuit and modified circuit are electrically equivalent to each other with the relations,

$$V_{CC2} = V_{CC} \quad \text{... (26)}$$

$$R_{C1} = \frac{R' R''}{R' + R''} \quad \text{... (27)}$$

and

$$V_{CC1} = \frac{V_{CC} R''}{R' + R''} + \frac{V_{BB} R'}{R' + R''} \quad \text{... (28)}$$

Using the relations (8), (9) and (10) practical emitter coupled astable multivibrator can be designed.

3.8.4 Advantages of Emitter Coupled Astable Multivibrator

The advantages of emitter coupled astable multivibrator over collector coupled are,

1. No external triggering signal is required. It is self starting.
2. The output is taken at the collector of transistor Q_2. But collector of Q_2 is not connected to any other part of the circuit and hence it is not taking any part in the regenerative action of the circuit. Thus the collector of Q_2 can be used to drive heavy loads, without affecting the circuit performance.
3. The distortion in the output waveform due to transients is absent.
4. The input terminal is the base of transistor Q_1 which is isolated hence it is easy from synchronization point of view.
5. A single capacitor C controls the frequency hence it is easy to change the frequency by varying C. In collector coupled, it is necessary to change both C_1 and C_2 to change frequency without changing the relative values of T_1 and T_2.

3.8.5 Disadvantages of Emitter Coupled Astable Multivibrator

The disadvantages of emitter coupled astable multivibrators are,

1. The number of components required are more compared to the collector coupled circuit.
2. The design is complicated because quiescent points of Q_1 and Q_2 are required to be designed such that Q_1 switches between cut-off and saturation while Q_2 switches between cut-off and active region.

3. Emitter resistances R_{e1} and R_{e2} cannot differ much hence with single capacitor C, widely different T_1 and T_2 cannot be obtained.
4. As design is complicated and more components are required, it is costlier.

Example 3.5 : *In a practical emitter coupled astable multivibrator the various circuit parameters are,*

$V_{CC} = 30\ V, \quad R_2 = 2R_1 << R'', \quad C = 0.1\ \mu F$

$R_{C2} = 0.22\ k\Omega, \quad R' = R'' = 1.1\ k\Omega, \quad R_{e1} = R_{e2} = 3.3\ k\Omega$

Calculate a) The various voltage levels b) Frequency of oscillations.

Assume silicon transistors with $h_{FE} = 30$.

Solution : a) For a silicon transistor,

$$V_\gamma = 0.5\ V, \quad V_{BE2} = 0.6\ V, \quad V_\sigma = 0.7\ V, \quad V_{CE}(sat) = 0.3\ V$$

This is a practical circuit.

$$\therefore \quad V_{CC2} = V_{CC} = 30\ V$$

$$V_{BB} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{2}{3} \times 30 = 20\ V$$

and

$$V_{CC1} = \frac{R''}{R' + R''} V_{CC} + \frac{R'}{R' + R''} V_{BB} = \frac{1}{2} \times 30 + \frac{1}{2} \times 20$$

$$= 25\ V$$

$$R_{C1} = \frac{R'R''}{R' + R''} = 550\ \Omega$$

Assume that Q_1 saturates and Q_2 is in active region.

$$I_{C2} = \frac{V_{CC1}}{R_e} \quad \text{and} \quad R_e = R_{e1} \parallel R_{e2} = 1.65\ k\Omega$$

$$\therefore \quad I_{C2} = \frac{25}{1.65 \times 10^3} = 15.15\ mA$$

$$I_{B2} = \frac{I_{C2}}{h_{FE}} = \frac{15.15}{30} = 0.505\ mA$$

$$\therefore \quad I_{B2} R_{C1} = 0.505 \times 0.55 = 0.277\ V$$

and $$I_{C2} R_{C2} = 15.15 \times 0.22 = 3.33\ V$$

The highest level of V_{EN1} is V_1 given by,

$$V_1 = V_{CC1} - I_{B2} R_{C1} - V_{BE2} - V_{CE}(sat) + V_\gamma$$

$$= 25 - 0.277 - 0.6 - 0.3 + 0.5$$

$$= \mathbf{24.323\ V}$$

The lowest level of V_{EN1} is,

$$V_{EN1}(t_1^-) = V_{BB} - V_\sigma = 20 - 0.7 = \mathbf{19.3\ V}$$

$$V_{CN1}(t_1^-) = V_{BB} - V_\sigma + V_{CE}(sat) = 20 - 0.7 + 0.3 = \mathbf{19.6\ V}$$

$$V_{CN1}(t_1^+) = V_{CC1} - I_{B2} R_{C1} = 25 - 0.277 = \mathbf{24.723\ V}$$

$$\therefore V_{CN1} = V_{BN2}$$

$$V_{EN2}(t_1^-) = V_{BN2}(t_1^-) - V_\gamma = 19.6 - 0.5 = \mathbf{19.1\ V}$$

$$V_{EN2}(t_1^+) = V_{CC1} - I_{B2} R_{C1} - V_{BE2} = 25 - 0.277 - 0.6 = \mathbf{24.123\ V}$$

$$V_D = V_{EN2}(t_1^+) - V_{EN2}(t_1^-) = \mathbf{5.023\ V}$$

b) The frequency of oscillations,

$$f = \frac{1}{T} = \frac{1}{T_1 + T_2}$$

$$T_1 = R_{e1}\, C\, ln \frac{V_1}{V_{BB} - V_\gamma} = 3.3 \times 10^3 \times 0.1 \times 10^{-6}\, ln\left[\frac{24.323}{20 - 0.5}\right]$$

$$= 72.93\ \mu sec$$

and $T_2 = T_1$ as $R_{e1} = R_{e2}$

$\therefore$ $T = 2T_1 = 0.1458$ ms

$\therefore$ $f = \frac{1}{T} = \mathbf{6.8556\ kHz}$

3.9 Schmitt Trigger Circuit

The Fig. 3.37 shows an important bistable circuit. It looks like basic bistable configuration but it differs by the fact that **the coupling from collector of the transistor Q_2 to the input of the first stage is missing in this circuit.**

The emitter of the two transistors are connected to each other and grounded through the resistance R_E.

The feedback is obtained through the resistance R_E. This circuit is called **Schmitt trigger** circuit. There exists two stable states of the output of this circuit.

Key Point : *The resistance R_{C1} is kept enough smaller than R_{C2} so that regeneration cannot take place. So circuit can be used as an amplifier rather than as a binary.*

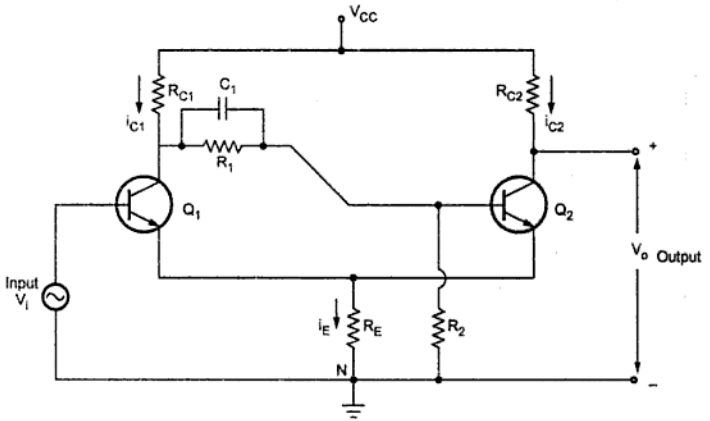


Fig. 3.37 Schmitt trigger circuit

3.9.1 Operation of the Circuit

Assume that a sinusoidal input voltage V_i is applied to the circuit. Let transistor Q_2 is conducting and is saturated. And as $V_i = 0$ at start, Q_1 is cut-off.

When Q_1 is OFF, it can be treated as open circuit thus circuit reduces as shown in the Fig. 3.38.

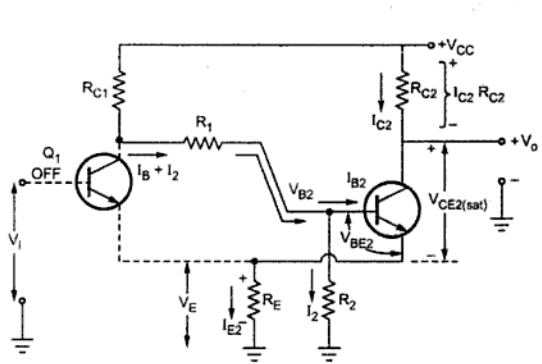


Fig. 3.38 D.C. conditions when Q_2 is ON

Now V_{B2} = Drop across R_2

This can be obtained by potential divider formed by R_{C1}, R_1 and R_2 across V_{CC}.

$$\therefore \quad V_{B2} = I_2 R_2$$

Thus current I_{C2} flows through Q_2 hence

$$\boxed{V_o = V_{CC} - I_{C2} R_2} \quad \ldots (1)$$

Key Point : *The drop $I_{E2} R_E$ raises emitter voltage of Q_1 and reverse biases the transistor Q_1.*

Now when V_i is increasing and to make Q_1 ON, it must increase to the level equal to cut-in voltage V_{BE1} of Q_1 plus the amount by which emitter voltage is raised i.e. V_E. So when V_i reaches to $V_{BE1} + V_E$, the Q_1 gets driven to active region. This input voltage level is called **upper threshold point** (UTP) of the Schmitt trigger. It is also called **input turn-on threshold** level.

As Q_1 is ON, i_{C1} start flowing. Due to drop across R_{C1} the base voltage of Q_2 reduces. This cumulatively reduces V_E which help Q_1 to conduct heavily and finally Q_1 gets driven into saturation. And simultaneously Q_2 is cut-off. At this point the output voltage is approximately V_{CC}. The cumulative action is very fast and switch over of output from its initial level of $V_{CC} - i_{C2} R_{C2}$ to V_{CC} is almost instantaneous. So we get fast rising output pulse when V_i reaches to UTP level. Then input looses the control over output and output remains in the stable state of V_{CC}. **This level will not change automatically.**

Key Point : *As Q_1 is ON, rapidly V_{BE2} reduces. This is called **regeneration** and this causes very rapid switchover from Q_2 ON to Q_1 ON and Q_2 OFF.*

When Q_1 is ON, Q_2 is OFF and acts as open circuit. This condition is shown in the Fig. 3.39.

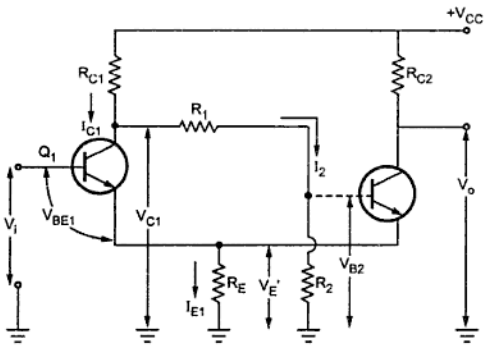


Fig. 3.39 D.C. conditions when Q_1 is ON

Now $V'_E = V_i - V_{BE1}$

$\therefore$ $I_{E1} = \frac{V'_E}{R_E} = \frac{V_i - V_{BE1}}{R_E}$ ... (2)

Key Point : *Thus the reduction is V_i, reduces I_{E1} and as $I_{C1} \simeq I_{E1}$, I_{C1} also reduces.*

The drop across R_{C1} is $I_{C1}R_{C1}$ neglecting I_2. Hence the collector voltage of Q_1 is,

$$V_{C1} = V_{CC} - I_{C1}R_{C1} \quad ...(3)$$

Thus I_{C1} reduces then V_{C1} increases, this directly controls V_{B2} of Q_2 which also increases. Thus when V_i starts decreasing and becomes equal to V_{B2}, then Q_2 again becomes ON. The level of V_i at which Q_2 again becomes ON is called **lower threshold point** (LTP) of the Schmitt trigger.

This is another stable state of the output and input looses control on output. The switchover from V_{CC} to $V_{CC} - i_{C2} R_{C2}$ is again instantaneous at LTP. So output remains at lower level, till V_i reaches to the UTP.

Key Point : *Thus as long as V_i reaches to either of the threshold level, there is no change in the output.*

The output has two stable states. So the circuit can be used as a **voltage comparator** to provide a change in output whenever the input exceeds a particular desired value.

The Fig. 3.40 shows the waveforms of the Schmitt trigger circuit.

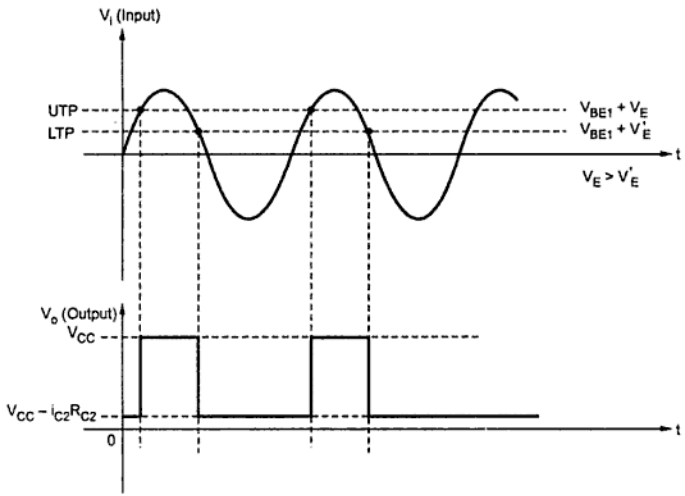


Fig. 3.40 Schmitt trigger waveforms

3.9.2 Hysteresis

The graph of output voltage against input voltage is called **transfer characteristics** of the Schmitt trigger. This is shown in the Fig. 3.41.

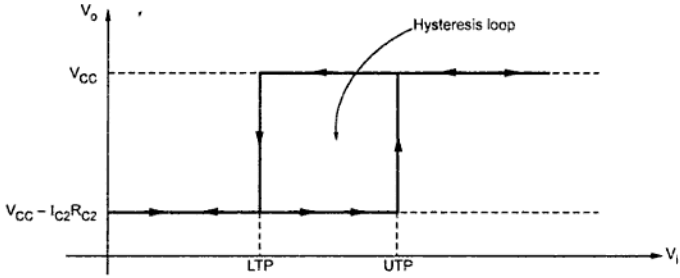


Fig. 3.41

It can be observed that once output changes its state, it remains there indefinitely until the input voltage crosses any of the threshold levels. So when output changes its state from low to high at UTP, it remains there till input crosses LTP and vice versa. This characteristics of Schmitt trigger is called **hysteresis**. It is also called **dead band** or **dead zone** as there is no change in output in this zone, though input changes. The loop of this characteristics is called **hysteresis loop**. The difference between UTP and LTP is called the width of hysteresis.

$\therefore$ $\boxed{W = \text{Width of hysteresis} = UTP - LTP}$

The amount of hysteresis can be changed by changing the values of R_{C1} and R_{C2}. While the UTP can be increased by increasing the value of R_E.

3.9.3 Applications

An important application of the Schmitt trigger is its use as an **amplitude comparator.** It identifies the moment at which any arbitrary waveform attains a particular reference level.

It can be used as a **squaring circuit**. Any arbitrary input can be converted to a square wave, using Schmitt trigger, by applied as arbitrary waveform to its input, such a square wave has an amplitude which is independent of the amplitude of the input waveform. And such an output has much faster leading and trailing edges than the input. Such an application is shown in the Fig. 3.42.

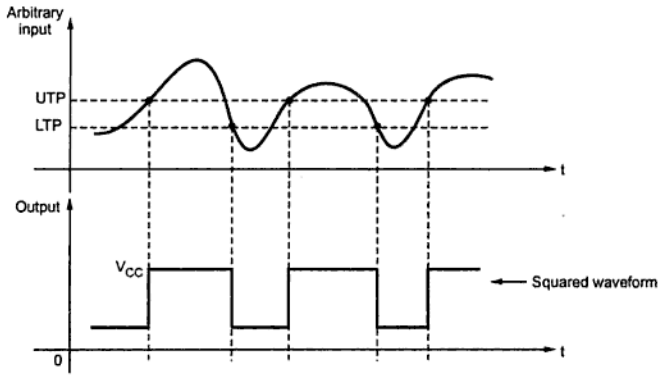


Fig. 3.42 Response of squaring circuit

The Schmitt trigger can be triggered between its two stable states by alternate positive and negative pulses. With this technique, Schmitt trigger can be used as flip-flop, which is its another application.

3.9.4 Function of C_1

The capacitor C_1 is a speedup capacitor. It improves the switching speed of the circuit. It can be observed that during switching, the change in collector voltage of Q_1 i.e. V_{C1} gets divided across R_1 and R_2 before it gets applied to the base of Q_2. The capacitor C_1 eliminates the potential division thus by whatever amount V_{C1} changes, by the same amount V_{B2} changes because of C_1. This increases the switching speed and thus C_1 acts as a **speed-up capacitor.**

3.9.5 Designing the Schmitt Trigger

The specified UTP must be equal to V_{B2} when Q_2 is ON.

$$\therefore \quad \boxed{V_{B2} = UTP} \qquad \ldots (4)$$

$$\therefore \quad V_E = V_i - V_{BE1} = V_{B2} - V_{BE2}$$

$$I_{E2} = I_{C2\,(on)}$$

$$\therefore \quad \boxed{R_E = \frac{V_E}{I_{E2}}} \qquad \ldots (5)$$

Now when Q_2 is ON, $V_{CE2\,(sat)} = 0.2$ V.

$$\therefore \quad I_{C2} R_{C2} = V_{CC} - V_E - V_{CE2\,(sat)}$$

$$\therefore \quad \boxed{R_{C2} = \frac{V_{CC} - V_E - V_{CE2\,(sat)}}{I_{C2\,(on)}}} \quad \ldots (6)$$

Now R_1 and R_2 must be smaller but must be larger than R_{C1}. For this,

$$i_2 = \frac{I_{E2}}{10}$$

$$\therefore \quad \boxed{R_2 = \frac{V_{B2}}{I_2}} \quad \ldots (7)$$

Now $I_{B2} = \frac{I_{C2}}{h_{fe\,(min)}}$ hence calculate $I_{B2} + I_2$.

$$\therefore \quad I_2 + I_{B2} = \frac{V_{CC} - V_{B2}}{R_{C1} + R_1}$$

$$\therefore \quad \boxed{R_{C1} + R_1 = \frac{V_{CC} - V_{B2}}{I_2 + I_{B2}}} \quad \ldots (8)$$

As V_i decreases towards LTP, Q_1 is still ON and Q_2 OFF till V_i reaches V_{B2}. The circuit is as shown in the Fig. 3.43. As V_i decreases, V_{B1} decreases and V_{B2} increases. The change of state occurs when,

$$V_i = V_{B2} = V_{B1}$$

$$\therefore \quad \boxed{V_i = \text{LTP} = V_{B2}} \quad \ldots (9)$$

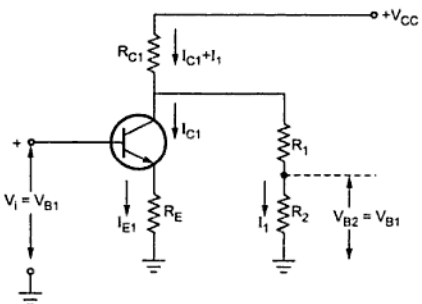


Fig. 3.43 For LTP, $V_i = V_{B2} = V_{B1}$

$$\therefore \quad I_1 = \frac{V_{B2}}{R_2}$$

$$\therefore \quad I_{C1} \approx I_{E1} = \frac{V_{B1} - V_{BE1}}{R_E}$$

$$\therefore \quad V_{CC} = R_{C1}(I_{C1} + I_1) + I_1(R_1 + R_2) \qquad \ldots(10)$$

Using equation (8) in equation (10),

$$\therefore \quad \boxed{R_{C1} = \frac{V_{CC} - I_1[R_1 + R_{C1} + R_2]}{I_{C1}}} \qquad \ldots (11)$$

$$\therefore \quad \boxed{R_1 = (R_1 + R_{C1}) - (R_{C1})} \qquad \ldots (12)$$

This completes the design.

3.10 Introduction to Blocking Oscillators

A special type of wave generator which is used to produce a single narrow pulse or train of pulses is called a **blocking oscillator.**

The two important elements of a blocking oscillator are, 1. An active device like transistor 2. A pulse transformer.

A pulse transformer is used to couple output of the transistor back to the input. The nature of such feedback through pulse transformer is controlled by relative winding polarities of a pulse transformer.

Key Point : *The properly controlled winding polarities produce a regenerative feedback.*

The circuit with such a regenerative feedback produces a single pulse or pulse train and called a **blocking oscillator.** If it is used to produce a single pulse, then it is called **monostable** operation of a blocking oscillator and if used to produce pulse train then it is called **astable** operation of a blocking oscillator.

Such a transformer coupled configuration of a blocking oscillator is important in many practical applications. These are concerned with the timing of some other circuits. These circuits are used in frequency dividers, counter circuits and for switching the other circuits on and off at the specific times.

Before discussing the blocking oscillator circuits let us study briefly the characteristics of a pulse transformer.

3.11 Pulse Transformer

A pulse transformer is basically a transformer which couples a source of pulses of electrical energy to the load; keeping the shape and other properties of pulses unchanged.

Key Point : *The voltage level of the pulse can be raised or lowered by designing the proper turns ratio for the pulse transformer.*

The characteristics of pulse transformers are,

1. Generally iron cored and small in size.
2. The leakage inductance is minimum.
3. The interwinding capacitance is low.
4. The cores have high permeability.
5. They have high magnetizing inductance

The pulse transformers are designed to handle fast waveforms like train of pulses and hence iron cored pulse transformers can be approximated to be **ideal transformers,** from analysis point of view.

The ideal pulse transformer model is shown in the Fig. 3.44.

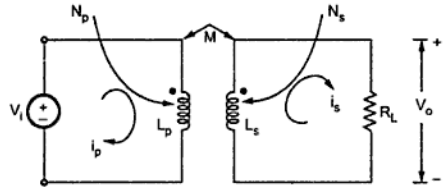


Fig. 3.44 Ideal pulse transformer model

As transformer is assumed to be an ideal, the primary, secondary and source resistances are neglected. All capacitances are also neglected. The core losses and nonlinearities in the magnetic circuit are also neglected.

Let L_p = Primary inductance

L_s = Secondary inductance

M = Mutual inductance

V_i = Source and V_o = Output response

R_L = Load resistance

N_p = Primary turns

N_s = Secondary turns

i_p = Primary current

i_s = Secondary current

The coefficient of coupling between primary and secondary is K. Its relation with transformer inductances is given by,

$$K = \frac{M}{\sqrt{L_p L_s}} \quad \ldots (1)$$

Key Point : *For an ideal transformer K = 1.*

Let $$n = \frac{N_s}{N_p} = \text{Transformation ratio}$$

Then for an ideal transformer, various ratios can be obtained as,

$$\frac{V_o}{V_i} = \frac{i_p}{i_s} = \frac{N_s}{N_p} = n = \sqrt{\frac{L_s}{L_p}} \quad \ldots (2)$$

Key Point : *The voltage and current ratios are inversely proportional to each other.*

3.11.1 Practical Equivalent Circuit

Adding the effects of various resistances and capacitances to an ideal transformer, a practical equivalent circuit of a pulse transformer can be obtained.

In the equivalent circuit, transformer windings are removed and various values and parameters on secondary side are reflected to the primary side.

So reflected output voltage on primary side is V_o/n where n is the transformation ratio, as given by equation (2). If R_L is the load resistance and R'_2 is secondary winding resistance then the total resistance R_2, reflected to primary side can be written as,

$$R_2 = \frac{R'_2 + R_L}{n^2}$$

The total effective shunt capacitance reflected on primary side is denoted as C. This capacitor C includes the transformer capacitance along with the reflected external shunt loading capacitance, which is dominant on the output side. The total **leakage inductance** is denoted as **series inductance** σ while the **magnetizing inductance** is denoted as **shunt inductance** L.

The resistance R_1 is the combined effect of primary winding resistance and the source impedance which is assumed to be resistive. Such an equivalent circuit of a pulse transformer, including resistances, inductances and total shunt capacitance is shown in the Fig. 3.45. All values are reflected on the primary side.

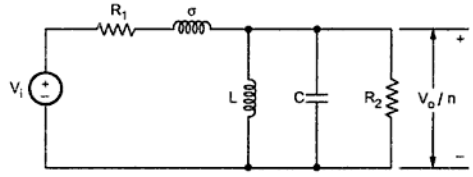


Fig. 3.45 Equivalent circuit of pulse transformer

Key Point : *Actually transformer capacitance is distributed capacitance but can be approximated as a single lumped capacitance, as indicated in an equivalent circuit.*

3.11.2 Pulse Response Characteristics

It is important that the transformer reproduces the shape of the input pulse as accurately as possible, at its secondary. The ideal input rectangular pulse cannot be obtained in practice. Due to the various inductances and capacitance, the pulse transformer output response is distorted. The output response can be obtained by solving the differential equations associated with an equivalent circuit of the pulse transformer. The transformers are designed such that the output response is of the type of damped oscillations. The rise time of such an output response sets the limit on the maximum pulse repetition rate, which can be handled by the pulse transformer. The rise time adds an error, distorting the output response. Hence **rise time is kept as small as possible.** The leakage inductance is kept to a minimum value. The distorted output response of a pulse transformer is shown in the Fig. 3.46.

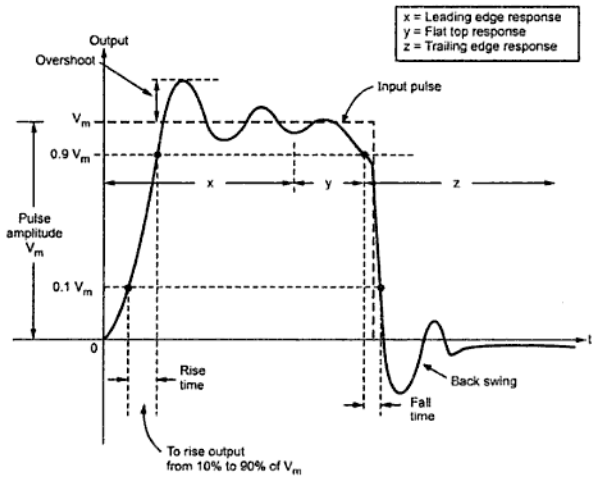


Fig. 3.46 Pulse transformer response

The total pulse characteristics can be divided into three sections :

i) Leading edge response : At start there is an overshoot and then the pulse settles down. The response till it settles down after the overshoot is called **leading edge response** denoted as x in the Fig. 3.46.

The **rise time** is an important parameter related to this part of the response. It is defined by the time required by the pulse to rise from 10 % of its amplitude to 90 % of its amplitude.

The other important parameter is an **overshoot**, which is the amount by which the output exceeds its amplitude, during first attempt.

ii) Trailing edge response : The response generally extends below the zero amplitude after the end of pulse width is called **back swing**. The portion of response from back wing till it settles down is trailing edge response denoted as z in the Fig. 3.46. This gives fall time characteristics.

iii) Flat top response : The portion of the response between the trailing edge and the leading edge is called **flat top response.**

The displacement of the pulse amplitude during its flat response is called **droop** or a **tilt.**

How to reduce pulse distortion :

The pulse distortion can be avoided by designing the pulse transformer with infinite magnetizing inductance L and zero σ and C values. This is possible by using high permeability material for the core. Hence primary turns are kept very small. Generally ferrite cores are used for the pulse transformers.

3.11.3 Applications of Pulse Transformer

The common use of iron cored pulse transformers is in the transmission and shaping of pulses which are having pulse width ranging between a fraction of a nanosecond to 25 μsec. The various applications of a pulse transformer are,

1. Commonly used in pulse generating circuits like blocking oscillators, which are discussed in this chapter.

   In such circuits it acts as a coupling element.

2. To change the amplitude and impedance level of a pulse.
3. For fast pulse signal transmission required in transmission lines.
4. To invert the polarity of the pulse.
5. To provide equal positive and negative pulses simultaneously, using centre-tapped winding.
6. To provide d.c. isolation between source and a load.
7. To differentiate a pulse.
8. For coupling the stages of pulse amplifiers.
9. Also used in digital signal transmission.

Let us study the use of pulse transformer in blocking oscillators.

3.12 Monostable Blocking Oscillator using Base Timing

A monostable blocking oscillator using base timing is also called a **triggered transistor blocking oscillator.**

The Fig. 3.47 shows the circuit diagram of a monostable blocking oscillator using base timing.

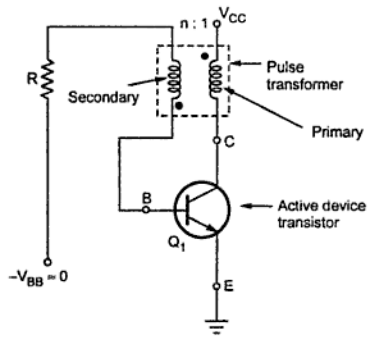


Fig. 3.47 Monostable blocking oscillator

One winding of the pulse transformer is in the collector circuit while the other is in the base circuit. The number of turns of transformer winding in base circuit is n times the number of turns of transformer winding in the collector circuit.

Key Point : *A pulse transformer core is made up of iron or ferrites but to avoid complexity of diagram, core is not indicated in the circuit diagram.*

A pulse transformer is basically a transformer which accepts the pulse at one winding and tries to produce a similar pulse at the other winding. It can produce inverted pulse, of that applied to one winding, if winding polarities are properly designed.

Key Point : *In a blocking oscillator, a pulse transformer is used to provide polarity inversion. The **polarity inversion** is indicated by the dots on the windings.*

A resistance R is used in series with the base of transistor, which controls the timing i.e. pulse duration. Hence the circuit is called **base timing blocking oscillator.** The pulse width can be varied in the range from nanoseconds to microseconds. The pulse width depends on resistance R, other pulse transformer parameters and the circuit parameters. To operate the circuit, a triggering signal is required to the collector, momentarily.

In the quiescent state, the transistor is off. The cut-in base-emitter voltage at room temperature for a germanium transistor is 0.1 V while for a silicon transistor it is 0.5 V. Thus if a small voltage pulse gets applied to the collector, then as the turns ratio of the pulse transform is n : 1, it can produce a large signal which is enough to start the operation of circuit. Such a small voltage pulse may be noise voltage or noise pulse. Thus

unintentionally, circuit may get triggered. In order to avoid such false triggering at increased temperatures, V_{BB} is applied to the base, keeping base-emitter junction reverse biased. But the magnitude of V_{BB} is of the order of few tenths of a volt and hence $|V_{BB}| < |V_{CC}|$.

Key Point : *Thus though V_{BB} is applied, there is no change in the circuit operation hence while discussing the operation of the circuit, V_{BB} can be neglected and resistance other end is assumed to be connected to ground.*

3.12.1 Operation and Mathematical Analysis of the Circuit

Let a triggering signal is applied momentarily to the collector of transistor Q_1 such that collector voltage level reduces suddenly. The pulse transformer winding polarities are designed such that the voltage applied at the primary (collector) produces inverted signal at the secondary (base). The phasing dots on the transformer indicate such a **voltage inversion.**

Key Point : *Thus base potential increases as collector potential decreases.*

When this voltage is more than the cut-in voltage of the transistor, it starts conducting drawing current from the supply. This increases the collector current. Due to this, drop across transformer winding in collector increases. This further lowers collector potential and increases base potential. This draws more collector current resulting further decrease in collector potential.

Key Point : *So if a.c. loop gain is greater than unity, regenerative action takes place and transistor gets driven into saturation from its off state.*

This cumulative action happens very quickly and time required for the transistor to enter saturation from its off state, can be ignored.

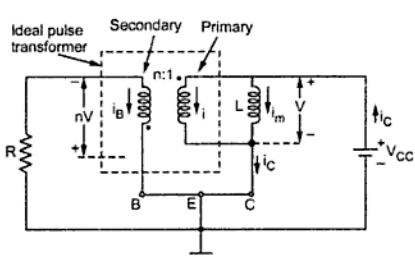


Fig. 3.48 Equivalent circuit

To obtain the equation of pulse width, consider the equivalent circuit of the pulse transformer neglecting resistances and shunt capacitance. The only important parameter is the shunt magnetizing inductance L. The transformer is ideal. The leakage inductance σ of the winding also can be neglected. Similarly for the transistor, the saturation voltage levels $V_{BE}(sat)$ and $V_{CE}(sat)$ are very small compared to V_{CC} and hence can be neglected. The equivalent circuit is shown in the Fig. 3.48.

Key Point : *For an ideal transformer sum of the ampere turns is a constant.*

All the ratios interms of transformation ratio n are valid for an ideal transformer. Thus,

$$\boxed{\frac{V_2}{V_1} = n = \frac{i}{i_B}} \quad \ldots (1)$$

where V_2 = Secondary voltage i.e. across winding in base circuit

V_1 = Primary voltage i.e. across winding in collector circuit

From the current ratio we can write,

$$i = n\, i_B \quad \ldots (2)$$

$$\therefore \quad \boxed{i - n\, i_B = 0} \quad \ldots (3)$$

As transistor is in saturation region, the voltage across primary collector winding of transformer is $V_1 = V = V_{CC}$. This is because transistor saturation voltage is neglected.

$$\therefore \quad \boxed{V_1 = V = V_{CC}} \quad \ldots (4)$$

According to transformation ratio,

$$\therefore \quad \boxed{V_2 = n\, V_1 = nV = n\, V_{CC}} \quad \ldots (5)$$

Key Point : *The polarities of V and nV are opposite to each other due to polarity inversion produced by pulse transformer.*

Applying KVL to the base circuit,

$$\boxed{i_B = \frac{nV}{R} = \frac{nV_{CC}}{R}} \quad \ldots (6)$$

Substituting in equation (2),

$$i = n \times \frac{nV_{CC}}{R} = \frac{n^2 V_{CC}}{R} \quad \ldots (7)$$

The voltage V across collector winding of transformer is also a voltage across magnetizing inductance L of transformer.

$$\therefore \quad V = L \frac{di_m}{dt}$$

$$\therefore \quad di_m = \frac{V}{L}\, dt$$

$$\therefore \quad \int di_m = \frac{V}{L} \int_0^t dt$$

$$\therefore \quad \boxed{i_m = \frac{V}{L} t = \frac{V_{CC} t}{L}} \qquad \ldots (8)$$

From the equivalent circuit we can write,

$$\boxed{i_C = i + i_m = \frac{n^2 V_{CC}}{R} + \frac{V_{CC} t}{L}} \qquad \ldots (9)$$

So at $t = 0^+$ i.e. just after the transistor enters into saturation the currents i_B and i_C are,

$$\boxed{i_B = \frac{nV_{CC}}{R} \text{ and } i_C = \frac{n^2 V_{CC}}{R} \quad \text{at } t = 0^+}$$

This operating point can be shown on the collector characteristics of the transistor as shown in the Fig. 3.49. It is denoted as point P.

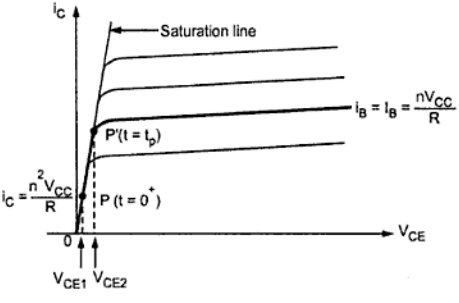


Fig. 3.49 Collector characteristics

Key Point : *For $t > 0$, it can be observed that i_B remains constant at $\frac{nV_{CC}}{R}$ while collector current increases from its value at $t = 0^+$ due to the term $\frac{V_{CC} t}{L}$.*

Thus on the collector characteristics, the point P moves along the constant i_B characteristics to P′ as shown in the Fig. 3.49. So operating point moves up the curve from P to P′. It can be noticed that the corresponding change in V_{CE} is from V_{CE1} to V_{CE2}. Due to increased V_{CE}, the transformer primary voltage drop reduces. Due to transformer action, the base voltage level also reduces. This reduces the base current. So transistor enters into active region from saturation region. This can be observed from the characteristics also that the point P′ is almost at knee point of the curve and after which the transistor active region starts. As base current reduces, the collector current reduces which further reduces transformer primary voltage level and again base current further reduces. As the loop gain exceeds unity in the active region, this action is **regenerative** and finally drives transistor into cut-off state from saturation. The time required for transistor to enter into cut-off from

point P′ is very small and the action is almost instantaneous. And hence at P′, collector current as well as base current reduces instantaneously to zero. And the pulse ends at P′, when the transistor comes out of saturation. The collector and base current waveforms are shown in the Fig. 3.50 (a) and (b).

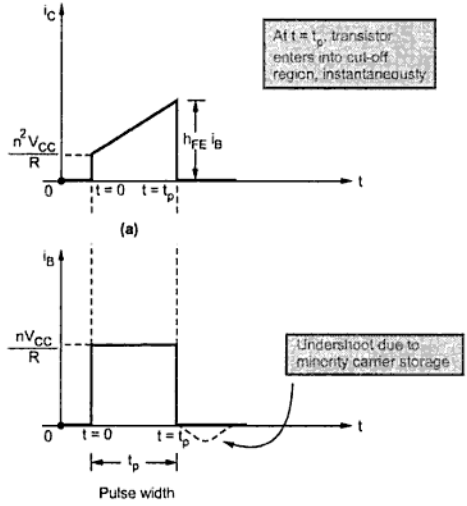


Fig. 3.50 Current waveforms

Key Point : *The collector current waveform is trapezoidal in nature while the base current waveform is constant.*

The time between t = 0 to t = t_p is pulse width t_p. At t = t_p, as transistor enters into cut-off, base current reduces to zero.

Key Point : *But due to minority carrier storage, i_B shows a small undershoot at t = t_p before it becomes zero as shown in the Fig. 3.50 (b).*

3.12.2 Expression for Pulse Width

At point P′ where pulse terminates we can write,

$$i_C = h_{FE}\, i_B \qquad \ldots (10)$$

Using equations (6) and (9) and using t = t_p,

$$\frac{n^2 V_{CC}}{R} + \frac{V_{CC}\, t_p}{L} = h_{FE}\, \frac{nV_{CC}}{R} \qquad \ldots (11)$$

$$\therefore \quad \frac{V_{CC}\, t_P}{L} = \frac{h_{FE}\, n V_{CC}}{R} - \frac{n^2 V_{CC}}{R}$$

$$\therefore \quad \frac{V_{CC}\, t_P}{L} = \frac{n V_{CC}}{R}(h_{FE} - n)$$

$$\therefore \quad \boxed{t_P = \frac{nL}{R}(h_{FE} - n) \approx \frac{n\, L h_{FE}}{R}} \qquad \ldots (12)$$

The value of n can be neglected compared to h_{FE}. Thus pulse width is linear function of h_{FE} which is temperature dependent. Also its values changes from transistor to transistor and hence pulse width gets affected due to transistor replacement. This is the biggest disadvantage of the circuit and hence base timing circuit is not used if stable pulse width is required. The circuit which makes pulse width insensitive to h_{FE} is emitter timing circuit, which is discussed in next section.

If output is required across a resistance R_L then R_L can be connected using three winding pulse transformer as shown in the Fig. 3.51. The R_L is connected across the third winding of the transformer which has n_1 number of turns.

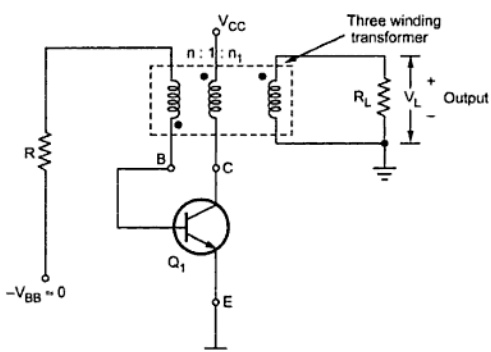


Fig. 3.51 Base timing circuit with R_L

3.13 Monostable Blocking Oscillator using Emitter Timing

This circuit is also called **triggered transistor blocking oscillator** using emitter timing. This uses a resistance in the emitter circuit which controls the pulse width. The pulse transformer used is a three winding transformer. One winding is in the collector circuit which is primary winding. The second winding is in the base circuit which has n times as many turns as the collector winding. A load resistance R_L is connected across third winding which has n_1 times as many turns as the collector winding. The resistance R_L acts as load and also helps in improving damping. The base and collector windings must

produce polarity inversion as indicated by dots while relative direction of third winding can be arbitrary. The circuit diagram of emitter timing circuit is shown in the Fig. 3.52.

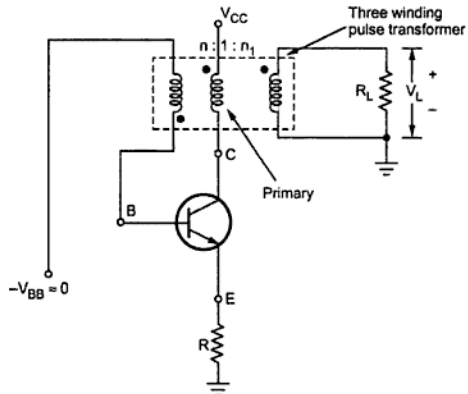


Fig. 3.52 Monostable blocking oscillator with emitter timing

The basic operation of the circuit is same as that of base timing circuit.

3.13.1 Mathematical Analysis

Assuming ideal transformer, neglecting leakage inductance, capacitance and winding resistances and neglecting transistor saturation voltages, the equivalent circuit can be shown as in the Fig. 3.53.

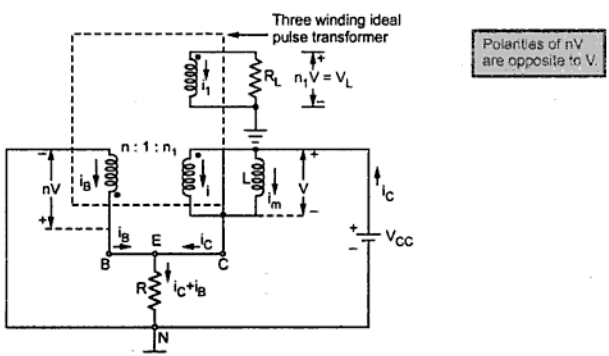


Fig. 3.53 Equivalent circuit of emitter timing monostable blocking oscillator

For simplicity of analysis, assume number of turns of primary of transformer which is in collector circuit be 1. Proportionally the number of turns of winding in base circuit is n and that of winding used to connect R_L is n_1.

Now V be the voltage across the primary collector winding, when transistor is in saturation. The corresponding voltage across secondary winding in base circuit is nV. And due to phase inversion, polarities of V and nV are opposite. The voltage across the resistance R_L is n_1V and the polarity is same as that of V.

Applying KVL to the outermost loop, including base and collector loops together we can write,

$$-V_{CC} + nV + V = 0$$

$$\therefore \quad \boxed{V = \frac{V_{CC}}{n+1}} \qquad \ldots (1)$$

Applying KVL to the base circuit

$$+ nV - (i_B + i_C) R = 0$$

$$\therefore \quad nV = (i_B + i_C) R \qquad \ldots (2)$$

$$\therefore \quad \boxed{i_C + i_B = i_E = \frac{nV}{R} = \frac{nV_{CC}}{(n+1)R}} \qquad \ldots (3)$$

The current i_E is the emitter current, coming out of the active device. It can be observed from equation (3) that the emitter current is constant.

It is known that sum of the ampere turns in an ideal transformer is always zero.

$$\therefore \quad \text{Ampere turns of primary} = i \times 1 = i$$

$$\text{Ampere turns of secondary} = i_B \times n = n\, i_B$$

$$\text{Ampere turns of tertiary} = i_1 \times n_1 = n_1 i_1$$

Key Point : *The signs of primary and tertiary are same while sign of secondary ampere turns is opposite to primary and tertiary ampere turns.*

$$\therefore \quad \boxed{i - n\, i_B + n_1\, i_1 = 0} \qquad \ldots (4)$$

From the load circuit loop,

$$V_L = n_1 V = - i_1 R_L \qquad \ldots (5)$$

Negative sign is due to assumption of opposite polarity of n_1V.

$$\therefore \quad \boxed{i_1 = -\frac{n_1 V}{R_L}} \qquad \ldots (6)$$

Substituting in equation (4),

$$i - n\, i_B - \frac{n_1^2\, V}{R_L} = 0 \qquad \ldots (7)$$

Applying KCL at the collector node,

$$i + i_m = i_C \text{ and } i_m = \frac{V\, t}{L} \text{ as derived earlier}$$

$$\therefore \quad \boxed{i = i_C - \frac{V\, t}{L}} \qquad \ldots (8)$$

Substituting in equation (7),

$$i_C - \frac{V\, t}{L} - n\, i_B - \frac{n_1^2\, V}{R_L} = 0 \qquad \ldots (9)$$

Solving equations (3) and (9) simultaneously, we get the individual expressions for i_C and i_B. Subtract equation (9) from equation (3), we get,

$$i_B + \frac{V\, t}{L} + n\, i_B + \frac{n_1^2\, V}{R_L} = \frac{nV_{CC}}{(n+1)R}$$

$$\therefore \quad (n+1)\, i_B = \frac{nV_{CC}}{(n+1)R} - \frac{V\, t}{L} - \frac{n_1^2\, V}{R_L} \qquad \ldots (10)$$

Substituting equation (1) in equation (10),

$$(n+1)\, i_B = \frac{nV_{CC}}{(n+1)R} - \frac{V_{CC}\, t}{(n+1)L} - \frac{n_1^2\, V_{CC}}{(n+1)R_L}$$

$$\therefore \quad \boxed{i_B = \frac{V_{CC}}{(n+1)^2}\left[\frac{n}{R} - \frac{t}{L} - \frac{n_1^2}{R_L}\right]} \qquad \ldots (11)$$

Substituting i_B in equation (9) or equation (3), i_C can be obtained as,

$$\boxed{i_C = \frac{V_{CC}}{(n+1)^2}\left[\frac{n^2}{R} + \frac{t}{L} + \frac{n_1^2}{R_L}\right]} \qquad \ldots (12)$$

It can be observed that due to presence of t in both the expressions for i_B and i_C, the i_B and i_C current waveforms are trapezoidal.

Key Point : *The slope of i_B is negative while slope of i_C is positive. The current i_E is constant during the pulse.*

These waveforms are shown in the Fig. 3.54. The voltage waveforms are also included in the Fig. 3.54.

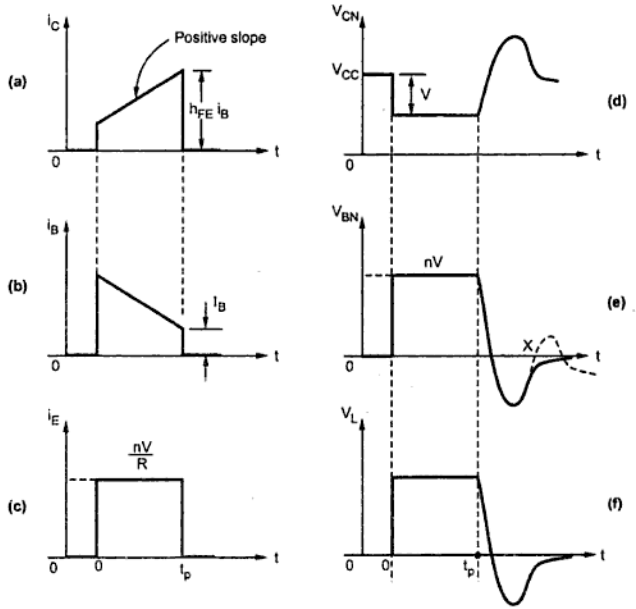


Fig. 3.54

3.13.2 Expression for Pulse Width

At $t = 0^+$, the current i_C is small and $i_C < h_{FE}\, i_B$. As time passes, the current i_C increases and the operating point P starts moving up on the saturation line of the collector characteristics. At the same time current i_B starts decreasing. Finally the point P gets settled at point P′ when $i_B = I_B$. At this point P′, the pulse ends. So time corresponding to this point P′ is $t = t_p$ and $i_C = h_{FE}\, I_B$. The movement of an operating point on the collector characteristics is already shown in the Fig. 3.49. The point P′ is at the knee point of the collector characteristics and at $t = t_p$ the transistor comes out of saturation and enters into active region. Due to increased V_{CE}, the voltage across primary decreases. This reduces the voltage across secondary winding by n times. Hence base current decreases. This further decreases i_C and so on. This regenerative action takes place very quickly at $t = t_p$ and transistor quickly becomes OFF from saturation. Hence the pulse ends at $t = t_p$.

So at $t = t_p$, $\quad i_C = h_{FE}\, i_B$ ... (13)

Substituting equation (11) and equation (12) into equation (13) and $t = t_p$,

$$\frac{V_{CC}}{(n+1)^2}\left[\frac{n^2}{R}+\frac{t_p}{L}+\frac{n_i^2}{R_L}\right] = \frac{V_{CC}}{(n+1)^2}\left[\frac{n}{R}-\frac{t_p}{L}-\frac{n_i^2}{R_L}\right]h_{FE}$$

$$\therefore \quad \frac{t_p}{L}+\frac{h_{FE}\,t_p}{L} = \frac{n}{R}h_{FE}-\frac{n^2}{R}-\frac{n_i^2}{R_L}h_{FE}-\frac{n_i^2}{R_L}$$

$$\therefore \quad \frac{(1+h_{FE})\,t_p}{L} = \frac{n}{R}(h_{FE}-n)-\frac{n_i^2}{R_L}(h_{FE}+1)$$

$$\therefore \quad \boxed{t_p = \frac{n\,L}{R}\frac{(h_{FE}-n)}{(h_{FE}+1)}-\frac{n_i^2\,L}{R_L}} \qquad \ldots (14)$$

This is the required pulse width expression.

Now usually $n << 1$ and $h_{FE} >> n$ hence

$$\frac{h_{FE}-n}{h_{FE}+1} \approx 1$$

$$\therefore \quad \boxed{t_p \approx \frac{n\,L}{R}-\frac{n_i^2\,L}{R_L}} \qquad \ldots (15)$$

It can be observed from this equation that the pulse width t_p is not dependent on the parameter h_{FE} and depends on the passive parameters like n, L, R and R_L.

Key Point : *Thus monostable blocking oscillator with emitter timing gives a stable pulse width.*

3.13.3 Limiting Value of R_L

Looking at equation (15) it can be seen that if $\frac{n_i^2\,L}{R_L}$ is greater than $\frac{n\,L}{R}$, the value of t_p becomes negative. The negative time is not possible in practice. Hence for positive t_p and regenerative action to take place in the circuit, R_L must satisfy certain condition.

From equation (14)

$$\frac{n_i^2\,L}{R_L} < \frac{n\,L}{R}\frac{(h_{FE}-n)}{(h_{FE}+1)}$$

$$\therefore \quad \boxed{R_L > \frac{n_i^2\,R}{n}\frac{h_{FE}+1}{h_{FE}-n}} \qquad \ldots (16)$$

This inequality assures that the loop gain exceeds unity which is necessary condition for regeneration to take place. And hence t_p cannot be negative.

3.13.4 Effect of Saturation Voltages on t_p

While deriving equation (14), it is assumed that the transistor saturation voltages are very small compared to V_{CC} and can be neglected. But the transistor saturation voltages $V_{CE}(sat)$ and $V_{BE}(sat)$ affect the pulse width t_p. The effect of these voltages is to multiply first term of the equation (14) by the factor F given by,

$$F = \frac{V_{CC} - V_{CE}(sat) - \left[\frac{V_{BE}(sat)}{n}\right]}{V_{CC} - V_{CE}(sat) + V_{BE}(sat)} \quad \ldots (17)$$

But if $V_{CC} >> V_{CE}(sat) + [V_{BE}(sat)/n]$ then equation (14) gets reduced to equation (15) and t_p becomes independent of supply voltage and h_{FE}.

Similarly, in the derivation of t_p the effect of base spreading resistance r'_{bb} is also neglected. If its effect is to be considered then in the resistance R, the small resistance $\frac{r'_{bb}}{(1+h_{FE})}$ must be added. But if R is large, more than 100 Ω then effect of the term $r'_{bb}/(1 + h_{FE})$ is negligibly small and hence can be neglected.

3.13.5 Recovery Considerations

The recovery considerations are to be obtained by examining the various waveforms after $t = t_p$. At $t = t_p$, the transistor currents become zero but magnetizing current i_m flowing through shunt inductance cannot be zero. This is because the current through an inductor cannot change instantaneously. So current i_m must continue to flow for $t > t_p$. As transistor is OFF, the only path for this current is through shunt capacitance C of the transformer, which we have neglected. The capacitor C is very small and current i_m decays very fast. Due to high rate of decay of i_m, a back e.m.f. is induced across L which inturn produces overshoots at collector, base and the load. Such overshoots are not desirable. These overshoots should not exceed the breakdown voltages of transistor. The overshoots at the collector, base and load are shown in the Fig. 3.54 (d), (e) and (f).

3.13.5.1 Necessity of Damping

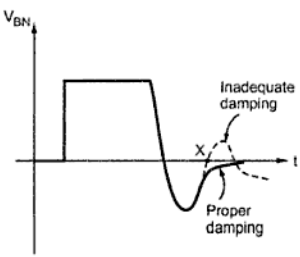


Fig. 3.55 Effect of damping

Consider the waveform of base voltage V_{BN} as shown in the Fig. 3.54 (e). Ideally the waveform should not exceed the zero value after $t > t_p$. This is shown by the solid curve in the Fig. 3.55. Such a waveform is possible only if the damping is sufficient.

But if the damping is not adequate then waveform shows a tendency to produce a backswing oscillation which exceeds zero base voltage level, at point X as shown in the Fig. 3.55.

Due to the proper damping, the back swing dies out in half a cycle. But if damping is insufficient, the base voltage level becomes positive at point X. This positive voltage level at the base, may drive the transistor into active region and due to regenerative action, the transistor may get driven into saturation. This starts the next pulse.

Key Point : *Thus the monostable circuit becomes astable or free running circuit, if damping is insufficient.*

In such a case, it produces train of pulses but shape of pulses is very much distorted. As the pulse transformer uses ferrite core, the core losses are low and if R_L is unable to provide proper damping then an external resistor must be shunted across the transformer in order to maintain monostable operation.

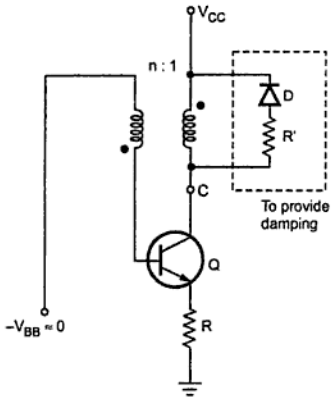


Fig. 3.56 Blocking oscillator with damping circuit

Thus it is necessary to add an external circuit which can provide sufficient damping, without loading the blocking oscillator during the pulse internal. A circuit using a resistance R′ and a series diode D is used to provide adequate damping. This circuit is connected across the primary winding of the pulse transformer. With an n-p-n transistor, the anode of the diode is connected towards collector side and cathode towards the supply side, with a resistance R′ in series with it. This direction of diode ensures that it does not conduct during the pulse interval and avoid loading the blocking oscillator during the pulse interval.

The external damping circuit is shown in the Fig. 3.56.

At the end of the pulse, the diode becomes forward biased due to the overshoot and hence energy stored in the magnetizing inductance L gets dissipated in resistance R′. The time constant with which energy gets dissipated is L/R′. Hence the sufficient damping is provided to suppress the transformer oscillations. The design of R′ is such that its value is smaller than the critical damping resistance. The time equal to four times the time constant is allowed to establish the quiescent condition so that next triggering can be applied to the oscillator. Hence the maximum frequency with which the circuit can be triggered is given by,

$$f_{max} = \frac{1}{4T} = \frac{1}{4\frac{L}{R'}} = \frac{R'}{4L} \quad \ldots (18)$$

where $T = 1 \text{ time constant} = \frac{L}{R'}$ ... (19)

3.13.6 Loading Considerations

From the equation derived for the pulse width of the circuit, it can be observed that the pulse width depends on the load resistance R_L which is connected across the tertiary winding. Instead of using R_L in tertiary winding, resistance R in emitter circuit may be used as load but the pulse width depends on resistance R.

Key Point : *Thus in either of the cases, the pulse width is load dependent.*

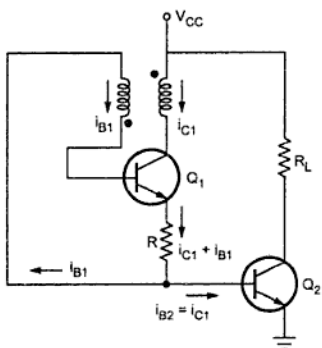


Fig. 3.57 Making pulse width load independent

There are certain applications of blocking oscillator in which load is variable. Example of such load is ferrite core memory where load depends on the number of cores to be excited. Hence load dependent pulse width is not desirable. Thus in practice a method is used to obtain pulse width which is load independent.

In such a method a load resistance R_L is connected using another transistor Q_2. The load resistance R_L is connected in the collector circuit of Q_2 as shown in the Fig. 3.57.

The base current of Q_2 is the collector current of Q_1.

The load R_L is switched ON and OFF through the transistor Q_2.

Applying KVL to collector of Q_1, loop through base emitter of Q_2, we get voltage across primary collector winding as,

$$V = V_{CC} - V_{BE2}(sat) \approx V_{CC} \quad \text{... (20)}$$

Similarly the load current can be obtained as,

$$I_L = \frac{V_{CC} - V_{CE2}(sat)}{R_L} \approx \frac{V_{CC}}{R_L} \quad \text{... (21)}$$

The load current flows for t = 0 to $t = t_p = \frac{nL}{R}$ and it is zero outside this interval.

3.13.7 Triggering Circuit for Monostable Blocking Oscillator

The Fig. 3.58 shows a popular triggering circuit which is used to trigger a blocking oscillator.

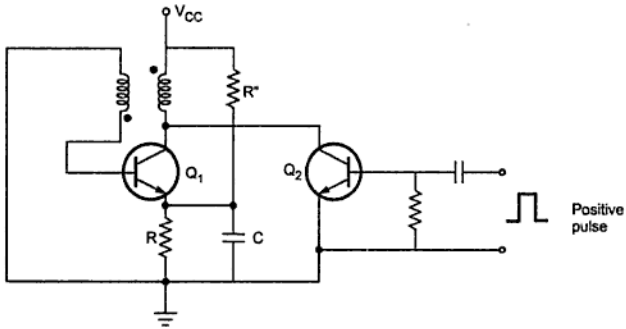


Fig. 3.58 Triggering circuit using transistor

It is necessary to **lower** the collector voltage of Q_1 momentarily by the triggering circuit. Hence momentarily a positive going pulse is applied to the base of Q_2. This drives Q_2 into saturation. The drop across Q_2 is zero when it is in saturation.

Key Point : *So Q_2 provides a short across the collector of Q_1.*

This monentarily brings the collector voltage of Q_1 to zero. Due to phase inversion, such a voltage gets induced in the secondary which makes the base of Q_1 positive, in such a way to bring it out of cut-off state. And thereafter normal working of monostable blocking oscillator starts. When pulse is removed from Q_2, Q_2 becomes off and acts as an open circuit. Thus normally it remains out of the circuit. So this triggering circuit is advantageous as there is no interaction of blocking oscillator with the triggering source.

Key Point : *The applied triggering pulse must have enough steep leading edge to ensure that the induced transformer voltage will bring Q_1 out of cut-off region.*

The resistance R'' is kept very large compared to R. Hence under quiescent conditions, the drop across R is maintained at about 0.5 V. This avoids the false triggering due to noise voltages and need of V_{BB} also gets avoided. A small capacitor C connected across R improves the rise time of the pulse, which is very important in monostable blocking oscillators.

Alternative method of triggering the blocking oscillator is to apply positive going pulse to the base of Q_1 through a diode or a negative going pulse to the collector of Q_1 through a diode. This is shown in the Fig. 3.59. The pulse is applied momentarily which makes diode forward biased. This lowers the collector voltage of Q_1 momentarily which inturn brings Q_1 out of the cut-off state. When circuit works, during the pulse formation, the

Now $\phi = BA$

$$\therefore \quad \frac{V_{CC}}{n+1} = NA \frac{dB}{dt}$$

$$\therefore \quad dt = \frac{(n+1) N A}{V_{CC}} dB$$

Integrating between the limits 0 to t_p we get

$$t_p = \frac{(n+1) N A B_m}{V_{CC}} \quad \ldots (24)$$

Key Point : *Thus the pulse duration now depends on the supply voltage and characteristics of the core and not on the transistor parameters. This is advantage of this method.*

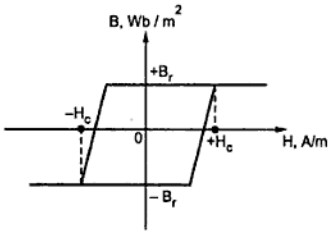


Fig. 3.63 Hysteresis loop of the core

One important property of the core along with the saturation is the hysteresis. The B-H loop for the core, showing the hysteresis is shown in the Fig. 3.63. At t = 0, when there is no current in the winding, the core flux density is at $- B_r$. When the blocking oscillator is triggered H increases and when it reaches to $+ H_C$, the core saturates with flux density as $+ B_r$. So net change in flux density is $2 B_r$. Hence t_p can be obtained from the equation (24) by substituting $B_m = 2 B_r$.

Once the core saturates, the dB/dt becomes zero and hence blocking oscillator cannot be triggered again. So to trigger the oscillator again, once the pulse ends, it is necessary to reset the flux density level back to $- B_r$. Otherwise retriggering of oscillator is impossible.

Key Point : *So after every pulse, the level of flux density must be resetted to $- B_r$.*

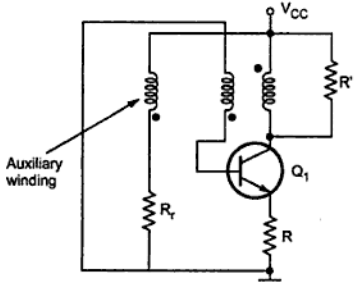


Fig. 3.64 Reset of flux density

This is possible by using a reset circuit. In this circuit an additional auxiliary winding in series with a resistance R_r is connected across the supply as shown in the Fig. 3.64.

When the transistor is in cut-off region then the current through the auxiliary reset winding is V_{CC}/R_r. This supplies the necessary opposite ampere turns H so that it becomes more negative than $- H_C$. At $H = - H_C$, the flux density becomes $- B_r$ and the oscillator can be once again triggered to obtain the pulse.

$$\therefore \quad i_C = n\, i_B + \frac{V\, t}{L} \qquad \ldots (4)$$

Applying KVL to outer loop,

$$V_{CC} - V - nV = 0$$

$$\therefore \quad V = \frac{V_{CC}}{n+1} \qquad \ldots (5)$$

Applying KVL to the base emitter loop,

$$i_C + i_B = \frac{n\, V}{R}$$

i.e. $$i_C + i_B = \frac{n\, V_{CC}}{(n+1)\, R} \qquad \ldots (6)$$

Solving equations (4) and (6) simultaneously,

$$i_C = \frac{V_{CC}}{(n+1)^2}\left[\frac{n^2}{R} + \frac{t}{L}\right]$$

and $$i_B = \frac{V_{CC}}{(n+1)^2}\left[\frac{n}{R} - \frac{t}{L}\right]$$

Hence during the pulse,

b) $$i_C = \frac{10}{(2+1)^2}\left[\frac{2^2}{1.5\times10^3} + \frac{t}{3\times10^{-3}}\right]$$

c) $\therefore$ i_C = **(0.002962 + 370.37 t) A**

and i_B = **(0.00148 − 370.37 t) A**

a) During the pulse, the amplitude at collector is

$$= V_{CC} - V \qquad \ldots \text{Neglecting saturation voltages}$$

$$= V_{CC} - \frac{V_{CC}}{n+1} = \frac{n}{n+1} V_{CC} = \mathbf{6.67\ V}$$

d) Using $i_C = h_{FE} i_B$ at $t = t_p$, the equation for t_p is,

$$t_p = \frac{n\, L}{R}\,\frac{h_{FE} - n}{h_{FE} + 1} = \frac{2\times3\times10^{-3}}{1.5\times10^3} \times \left[\frac{50-2}{50+1}\right]$$

$$= \mathbf{3.764\ \mu sec}$$

If saturation voltages are considered this t_p gets multiplied by the factor F given by,

$$F = \frac{V_{CC} - V_{CE}(sat) - \left[\dfrac{V_{BE}(sat)}{n}\right]}{V_{CC} - V_{CE}(sat) + V_{BE}(sat)}$$

So i_m at $t = t_p$ can be obtained as,

$$i_m = \frac{V_{CC}\, t_p}{(n+1)L} = I_o \qquad \ldots (1)$$

Let this current is denoted as I_o.

$$\therefore \quad \boxed{t_p = \frac{n\,L}{R}} \qquad \ldots \textbf{Derived earlier with } R_L = \infty$$

Substituting in equation (1),

$$\therefore \quad \boxed{I_o = \frac{n}{(n+1)} \frac{V_{CC}}{R}} \qquad \ldots (2)$$

Key Point : *Thus peak magnetizing current is not dependent on the magnetizing inductance L.*

At the end of the pulse, transistor Q is again cutoff and hence the current I_o must flow through the diode D.

Key Point : *Note that in this analysis, the shunt capacitance C of the pulse transformer plays an important role and cannot be neglected.*

Thus $i_m = I_o$ not only flows through 'D' but also through the shunt capacitance C. The equivalent circuit is shown in the Fig. 3.69 (a). In this circuit diode network D is replaced by its model with a battery of V_γ in series with the forward resistance R_f which is almost zero.

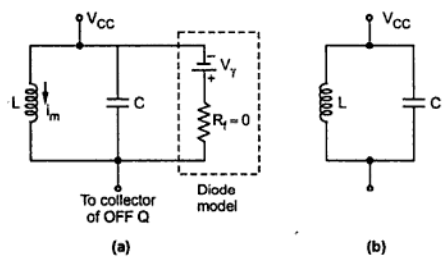


Fig. 3.69

Key Point : *Due to battery of V_γ, the collector voltage V_C increases by V_γ above V_{CC}.*

$$\therefore \quad \boxed{T = \text{Time period} = t_p + t_f + t_a} \qquad \ldots (6)$$

At $t = t_a$, the current i_m achieves some negative value denoted as I'_m as shown in the Fig. 3.70.

So at $t = T$, $i_m = I'_m$, we can **analyse LC circuit at the end of one quarter of a cycle.** At this time the capacitor electrostatic energy gets transformed into inductive electromagnetic energy. The inductor current is I'_m now while initial capacitor voltage is V_γ. So equating two energies at $t = t_a$.

$$\frac{1}{2} L [I'_m]^2 = \frac{1}{2} C [V_\gamma]^2$$

Solving $$\boxed{I'_m = V_\gamma \sqrt{\frac{C}{L}} \text{ at } t = t_a} \qquad \ldots (7)$$

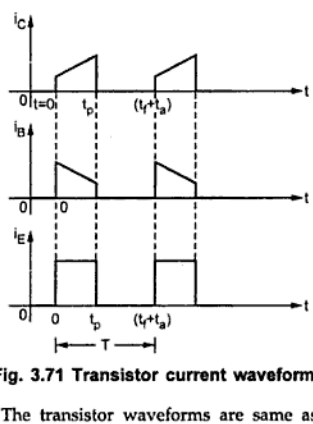


Fig. 3.71 Transistor current waveforms

This is magnetizing current at the end of one cycle of the output. So i_m is not zero when next cycle starts, this may cause some change in the expressions of t_p and t_f but as this error is practically very small, i_m can be assumed to be zero at the start of the next pulse.

It may also be noted that t_f is the time after t_p and t_a is time after t_f hence $T = t_p + t_f + t_a$.

Key Point : *The collector and base voltages are nearly rectangular and do not show any overshoots, as in case of monostable operation.*

The transistor current waveforms are shown in the Fig. 3.71.

The transistor waveforms are same as that of monostable circuit for $t = 0$ to $t = t_p$ while all the currents are zero for t_p to $t_f + t_a$ and then the cycle repeats.

3.15.3 Mark-Space Ratio and Duty Cycle

The ratio of time for which Q is ON to time for which Q is OFF is called **mark-space ratio. If this is unity, then the output is almost symmetrical square wave.**

The duty cycle is defined as the ratio of the ON time t_p to the time period T. Mathematically it is given by,

$$\boxed{D = \frac{t_p}{T}} \qquad \ldots (8)$$

If lower duty cycle is required then t_f must be increased with respect to t_p. This gives a pulse rather than a square wave. From the expressions for t_p and t_f we get,

$$\frac{t_p}{t_f} = \frac{(nL/R)}{\left[\frac{n}{n+1}\cdot\frac{L}{R}\cdot\frac{V_{CC}}{V_\gamma}\right]} = \frac{(n+1)V_\gamma}{V_{CC}} \quad \ldots (9)$$

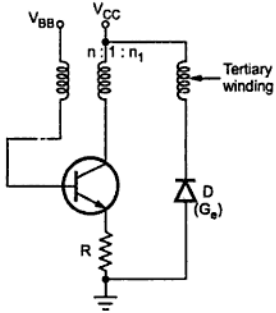


Fig. 3.72 High duty cycle astable blocking oscillator

For minimum duty cycle, V_γ should be minimum which is possible by using a single diode in a diode network D with $V_\gamma = 0.1$ V. Thus for a $V_{CC} = 25$ V and $n = 1$ we can get duty cycle of about [(2) (0.1)/25] = [1/125] which is very low. But such a low duty cycle operation is not stable because V_γ is temperature dependent. It changes at a rate – 2.5 mV/ ℃ and may cause error in very low duty cycle operation.

Key Point : *But high duty cycle operation can be obtained by using temperature compensated zener diode, which is very stable.*

Another way of obtaining high duty cycle stable operation is to place a germanium diode in series with a tertiary winding across the supply voltage. This is shown in the Fig. 3.72.

The important advantage of the astable blocking oscillator is that for high duty cycle operation also, the **power dissipation of the transistor is very low.** This is because when transistor is in saturation though current is high, saturation voltages are almost zero. While when output voltage is high the transistor currents are very low.

Example 3.7 : *A diode controlled astable blocking oscillator has the following parameters :*

$L = 5$ mH, $C = 90$ pF, $V_{CC} = 10$ V, $R = 470\ \Omega$, $V_\gamma = 6$ V, $n = 1$ and $V_{BB} = 0.5$ V.

Calculate : a) The period and duty cycle of the free oscillations.

b) The peak voltages and currents.

c) The current in magnetizing inductance at the end of one cycle.

Neglect saturation junction voltages.

Solution :

a) $T = t_p + t_f + t_a$

Now $t_p = \frac{nL}{R} = \frac{1\times5\times10^{-3}}{470} = 10.6383\ \mu\text{sec}$

$$t_f = \frac{n}{n+1}\frac{L}{R}\frac{V_{CC}}{V_\gamma} = \frac{1}{2}\times\frac{5\times10^{-3}}{470}\times\frac{10}{6} = 8.865\ \mu\text{sec}$$

$$t_a = 1.57\sqrt{LC} = 1.57\sqrt{5\times10^{-3}\times90\times10^{-12}} = 1.053\ \mu\text{sec}$$

$$T = \mathbf{20.5564\ \mu sec}$$

$$\therefore \quad f = \frac{1}{T} = 48.6464\ \text{kHz}$$

$$\text{Duty cycle} = \frac{t_p}{T} = \frac{10.6383}{20.5564} = \mathbf{0.5175}$$

So duty cycle is **51.75 %** which is very close to 50 % giving an indication that Q ON and OFF times are equal and the output is almost symmetrical square wave.

b) The collector voltage varies from $V_{CC} - V$ to $V_{CC} + V_\gamma$.

Now $$V = \frac{V_{CC}}{n+1} = \frac{10}{2} = 5\ \text{V}$$

$\therefore$ V_C varies from 10 – 5 i.e. + 5 V to 10 + 6 = 16 V.

The base voltage varies from nV to $-n\,V_\gamma$ i.e. + 5 V to – 6 V.

The emitter current is constant given by,

$$i_E = \frac{nV}{R} = \frac{1\times5}{470} = 10.638\ \text{mA}$$

$$i_B = \frac{V_{CC}}{(n+1)^2}\left[\frac{n}{R} - \frac{t}{L}\right]$$

So $$i_{B\,max} = i_B|_{t=0} = \frac{10\times1}{(2)^2\times470} = 5.31\ \text{mA}$$

$$i_B\left(t = t_p\right) = \frac{10}{(2)^2}\left[\frac{1}{470} - \frac{10.63\times10^{-6}}{5\times10^{-3}}\right] = 4.148\ \mu\text{A} \approx 0\text{A}$$

$$i_C = \frac{V_{CC}}{(n+1)^2}\left[\frac{n^2}{R} + \frac{t}{L}\right]$$

$\therefore$ $$i_C\left(t = t_p\right) = \frac{10}{(2)^2}\left[\frac{1}{470} + \frac{t_p}{5\times10^{-3}}\right] = \mathbf{10.638\ mA}$$

$$I_0 = \text{Peak magnetizing current} = \frac{n\,V_{CC}}{(n+1)\,R}$$

$$= \frac{10}{2\times470} = \mathbf{10.638\ mA}$$

c) I'_m which is the magnetizing current at the end of one cycle is given by

$$I'_m = V_\gamma \sqrt{\frac{C}{L}} = 6 \sqrt{\frac{90\times10^{-3}}{5\times10^{-3}}} = 0.804 \text{ mA}$$

Example 3.8 : *Design a free running blocking oscillator using diode control with,* $V_{CC} = 30\ V,\ V_{BB} = 1\ V, f = 20\ kHz$, *duty cycle* $= \frac{1}{10}$

The peak of the pulse at the collector is 10 V and the peak emitter current is 5 mA. Find the values of n, V_γ, *R and L. Make reasonable assumptions.*

Solution :

$$f = 20 \text{ kHz} \quad \text{hence} \quad T = \frac{1}{f} = 50\times10^{-6} \text{ sec}$$

Now $T = t_p + t_f + t_a = t_p + t_f$ .... Neglecting t_a

$\therefore\ 50\times10^{-6} = t_p + t_f$

Now Duty cycle $= \frac{t_p}{T} = \frac{1}{10}$

$\therefore\ t_p = \frac{T}{10} = 5\times10^{-6}$ sec

$\therefore\ t_f = 50\times10^{-6} - 5\times10^{-6} = 45\times10^{-6}$ sec

$$i_{E\,(max)} = \frac{nV}{R}$$

$\therefore\ \frac{nV}{R} = 5\times10^{-3}$ ... (1)

$$t_p = \frac{nL}{R}$$

$\therefore\ \frac{nL}{R} = 5\times10^{-6}$ ... (2)

Dividing equations (1) and (2), V = 1000 L ... (3)

And $V = \frac{V_{CC}}{n+1} = \frac{30}{n+1}$ ... (4)

The collector voltage pulse extends from $V_{CC} - V$ to $V_{CC} + V_\gamma$.

$\therefore$ Peak of the pulse $= [V_{CC} + V_\gamma] - [V_{CC} - V] = V + V_\gamma$

$\therefore\ V + V_\gamma = 10$ (Given) ... (5)

and $t_f = \frac{n}{n+1} \frac{L}{R} \frac{V_{CC}}{V_\gamma} = 45\times10^{-6}$ ... (6)

$$\therefore \quad \frac{nL}{R}\frac{V_{CC}}{(n+1)}\frac{1}{V_\gamma} = 45\times10^{-6}$$

$$5\times10^{-6}\times\frac{V}{V_\gamma} = 45\times10^{-6}$$

Using equation (5), $5\times10^{-6}\times\frac{(10-V_\gamma)}{V_\gamma} = 45\times10^{-6}$

$$10-V_\gamma = 9\ V_\gamma$$

$$V_\gamma = 1\ V$$

$$V = 10-V_\gamma = 9\ V$$

Using equation (4), $n = \mathbf{2.3333}$

Using equation (3), $L = \mathbf{9\ mH}$

Using equation (2), $R = \mathbf{4.2\ k\Omega}$

The designed circuit can be shown as in the Fig. 3.73.

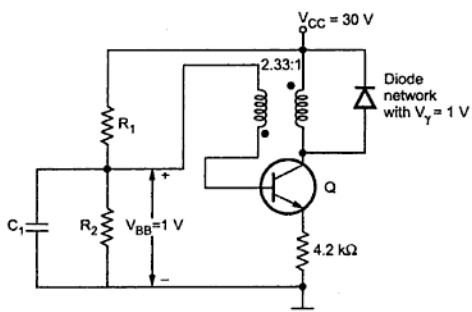


Fig. 3.73

Neglecting base current,

$$V_{BB} = \frac{V_{CC}\,R_2}{R_1+R_2}$$

$$\therefore \quad 1 = \frac{30\ R_2}{R_1+R_2}$$

$$\therefore \quad R_1 = 29\ R_2$$

So let $R_2 = 1\ k\Omega$

$R_1 = 29\ k\Omega$

This is required potential divider components.

3.16 RC Controlled Transistorized Astable Blocking Oscillator

A diode network can be replaced by RC network to obtain RC controlled astable blocking oscillator. Such RC network can be added in the emitter circuit of a monostable blocking oscillator or in the base circuit of a monostable blocking oscillator. The Fig. 3.74 (a) shows R_1 C_1 section added in emitter circuit while the Fig. 3.74 (b) shows R_1 C_1 section added in base circuit of a basic monostable oscillator circuit, to get astable blocking oscillator.

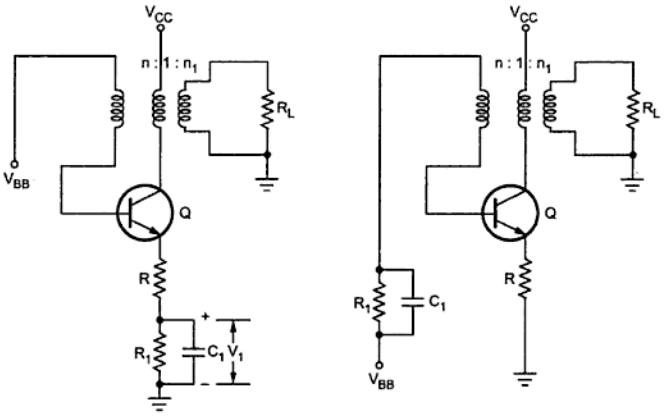


Fig. 3.74 RC controlled astable blocking oscillator

Key Point : *In this circuit, another change is the polarity of* V_{BB}, *which is reversed as compared to one which is used in monostable circuit.*

3.16.1 Operation of Circuit with R_1C_1 in Emitter

To understand the operation, let us assume that the capacitor C_1 is initially charged to v_1 with the polarities as shown in the Fig. 3.74 (a).

Let V_γ = Cut-in voltage of B-E junction of Q

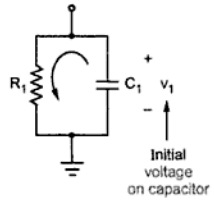


Fig. 3.75

As V_{BB} is positive, it can be seen that for transistor to be ON $V_{BB} - V_\gamma > v_1$. But assume that initially $v_1 > V_{BB} - V_\gamma$, hence B-E junction of a is reverse biased and transistor is cut-off.

Now the capacitor C_1 discharges through resistance R_1 as shown in the Fig. 3.75. Thus v_1 starts decreasing.

When v_1 becomes less than $V_{BB} - V_\gamma$, B-E junction of transistor Q becomes forward biased and the transistor Q gets driven into active region. This starts the regenerative action, same as in the monostable circuit and transistor Q gets driven immediately into the saturation region.

When Q is in saturation, pulse formation starts. During this time, capacitor C_1 starts charging again.

Key Point : *At the end of the pulse, the capacitor gets charged to* V_1 *which is greater than initial voltage* v_1.

The transistor is now off and capacitor starts discharging through R_1. Thus transistor Q remains OFF till the voltage of C_1 attains a value just less than $V_{BB} - V_\gamma$, where Q enters again into active region. The time required by capacitor C_1 to discharge from V_1 to $V_{BB} - V_\gamma$ is off time of transistor Q and denoted as t_f.

The discharge equation of a capacitor is,

$$\boxed{V_C = V_i \; e^{-t/RC}}$$

where V_C = Capacitor voltage while discharging

V_i = Initial voltage from which discharge starts

Thus for our circuit, $V_C = V_{BB} - V_\gamma$, $V_i = V_1$ and $t = t_f$

$$\therefore \quad V_{BB} - V_\gamma = V_1 \; e^{-t_f / R_1 C_1}$$

$$\therefore \quad e^{-t_f / R_1 C_1} = \frac{V_{BB} - V_\gamma}{V_1}$$

$$\therefore \quad -t_f / R_1 C_1 = ln \left[\frac{V_{BB} - V_\gamma}{V_1} \right]$$

$$\therefore \quad t_f = -R_1 C_1 \; ln \left[\frac{V_{BB} - V_\gamma}{V_1} \right]$$

Absorbing negative sign inside logarithmic term,

$$\boxed{t_f = R_1 C_1 \; ln \left[\frac{V_1}{V_{BB} - V_\gamma} \right]} \qquad ...(1)$$

Thus the period of the RC controlled astable blocking oscillator is given by,

$$T = t_p + t_f \qquad \ldots(2)$$

The value of t_p can be obtained from an equivalent circuit as shown in the Fig. 3.76.

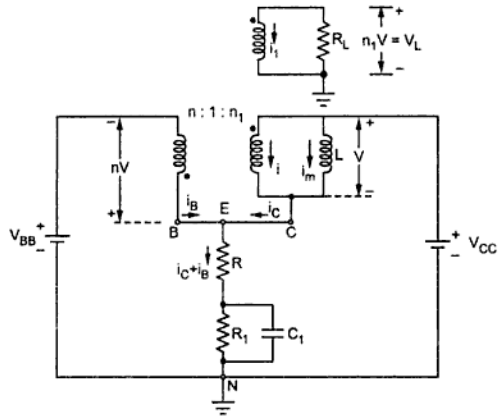


Fig. 3.76 Equivalent circuit of RC controlled astable blocking oscillator

The circuit is similar to the equivalent circuit of monostable blocking oscillator with V_{BB}, R_1 and C_1 as additional parameters.

Applying KVL to various loops and assuming $h_{FE} >> 1$, $R_1 >> R$ and neglecting saturation voltages we get,

$$\frac{t_p}{L} - \frac{n}{R} e^{-t_p/RC_1} = -\frac{n_1^2}{R_L} \qquad \ldots(3)$$

The equation is to be solved for t_p, but it consists of the terms of t_p as well as exponential terms with t_p. Such an equation is called **transcendental equation** in t_p which can not be solved analytically.

Key Point : *The equation is to be solved graphically to obtain* t_p.

But equation can be used for designing the value of L, if required, t_p is specified and other parameters are known.

The exponential term can be expressed in power series form as,

$$e^{-x} \approx 1 - x \qquad \ldots\ldots \text{if } x << 1$$

It can be observed that initial capacitor voltage level is less than the level V_1 attained at $t = t_p$. And t_f is the time taken by the capacitor voltage to discharge to the level $V_{BB} - V_\gamma$. The total time period $T = t_p + t_f$.

Key Point : *The astable blocking oscillator with RC circuit in base behaves similarly but the expression for t_p and V_1 are very difficult to deal with, as compared to the RC circuit in emitter.*

3.16.2 Limitations of Low Duty Cycle

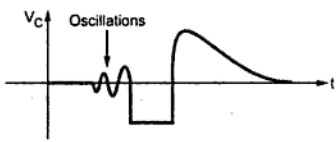


Fig. 3.78 Oscillations due to low duty cycle

If RC controlled astable blocking oscillator is adjusted to give low duty cycle, it suffers from certain limitations.

In low duty cycle operation, the voltage v_1 across the capacitor discharges very slowly. Due to this, pulse at the collector has **distorted waveform**. There are certain oscillations created just before the pulse starts, as shown in the Fig. 3.78.

The reason for these oscillations is slow rate at which capacitor voltage discharges. Due to this slow rate, initially transistor comes out of off state gradually. During this, the loop gain increases from zero. This increase in gain is due to the transistor characteristics. When it becomes greater than unity, the circuit begins to oscillate. But oscillations do not grow in amplitude due to nonlinearity of the transistor near cut-off region.

In active region, the loop gain further increases, increasing the amplitude of oscillations. The voltage v_1 keeps on decreasing. This drives the transistor to the saturation region. In the saturation region the gain suddenly reduces, limiting the oscillations and the pulse starts. But due to this, the pulse waveform is distorted, with oscillations just before the starting of the pulse.

Key Point : *Such a distortion is absent if capacitor voltage v_1 falls very rapidly. This does not give transistor any time to change its again and the oscillations get suppressed.*

The range of duty cycle for which such oscillations appear is corresponding to the **ratio t_f / t_p greater than about 200.**

Similarly such low duty cycle operation also suffered from the problem of instability, due to fluctuations in t_f. This is due to the fact that after every cycle, the loop gain does not change by the same amount. And thus small change in v_1 causes a large change in t_f.

3.16.3 Comparison of Astable Blocking Oscillator Circuits

The diode controlled and RC controlled astable blocking oscillators can be compared from their advantages and limitations. The **diode controlled circuit** has following characteristics including advantages and limitations.

This negative V_{B1} ensures that the transistor Q_1 is indeed OFF.

$$I_1 = \frac{V_{CC}}{R_C} = \frac{5}{1}$$

$$= 5 \text{ mA}$$

$$I_2 = -\frac{V_{BB}}{R_1 + R_2} = \frac{-(-5)}{5+25}$$

$$= 0.167 \text{ mA}$$

$$\therefore \quad I_{C2} = I_1 - I_2 = 5 - 0.167$$

$$= 4.833 \text{ mA}$$

$$\therefore \quad (I_{B2})_{min} = \frac{I_{C2}}{(h_{fe})_{min}} = \frac{4.833}{20}$$

$$= \mathbf{0.2416 \text{ mA}}$$

To calculate actual I_{B2}, consider the equivalent circuit as shown in the Fig. 3.79(b).

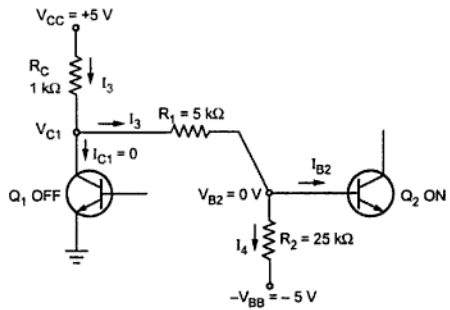


Fig. 3.79(b)

$$I_3 = \frac{V_{CC}}{R_1 + R_C} = \frac{5}{5+1}$$

$$= 0.833 \text{ mA}$$

$$I_4 = \frac{V_{B2} - V_{BB}}{R_2} = \frac{-(-5)}{25}$$

$$= 0.2 \text{ mA}$$

Thevenin's equivalent is shown in the Fig. 3.79(d).

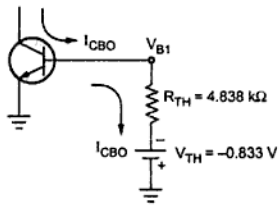


Fig. 3.79(d)

For Q_1 OFF, which is npn silicon transistor

$$V_{BE} \leq 0 \text{ V}$$

For (I_{CBO})max, V_{BE}(cut-off) = V_{B1} = 0 V

$$\therefore \quad (I_{CBO})\,\text{max} = \frac{V_{B1} - V_{TH}}{R_{TH}}$$

$$= \frac{0-(-0.833)}{4.838\times10^{3}}$$

$$= \mathbf{0.1722\ mA}$$

$\therefore I_{CBO}$ maximum is 172.21 μA, upto which circuit will function satisfactorily.

Example 3.10 : *The self biased bistable multivibrator uses n-p-n silicon transistors having worst case (maximum) values of $V_{CE}(sat)$ = 0.4 V, $V_{BE}(sat)$ = 0.8 V, and zero base to emitter voltage for cut-off. The circuit parameters are V_{CC} = 20 V, R_C = 4.7 kΩ, R_1 = 30 Ω, R_2 = 15 kΩ ane R_E = 390 Ω.*

a) Find the stable state currents and voltages.

b) Find the minimum value of h_{fe} required to give the values in part (a).

c) As the temperature is increased, what is the maximum value to which I_{CBO} can increase before the condition is reached when neither transistor is OFF.

Solution : The circuit of self biased binary is shown in the Fig. 3.80.

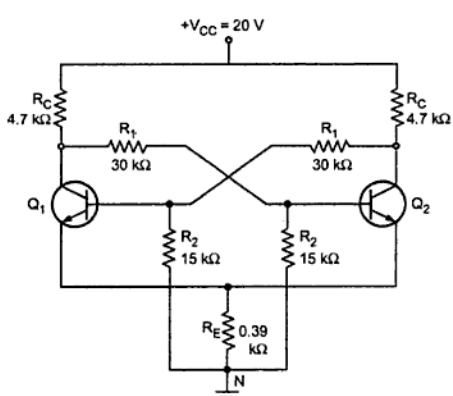


Fig. 3.80

Assume Q_1 is OFF and Q_2 is ON. As Q_2 is in saturation,

$$V_{CE}(sat) = V_{CE2} = 0.4 \text{ V}$$

$$V_{BE}(sat) = V_{BE2} = 0.8 \text{ V}$$

a) Calculation for the stable state currents and voltages

Draw equivalent circuit from base of Q_1 to collector of Q_2.

Another equivalent circuit from collector of Q_1 to base of Q_2 is shown in the Fig. 3.81.

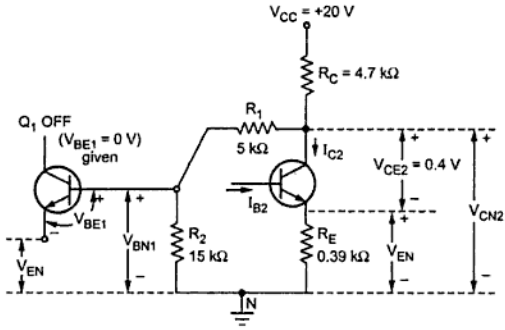


Fig. 3.81

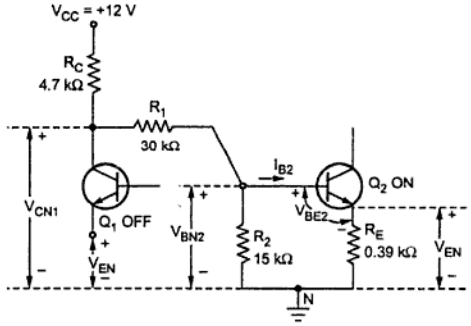


Fig. 3.82

And $$R_{TH} = (R_2) \parallel (R_1 + R_2) = \frac{15 \times 34.7}{(15 + 34.7)}$$

$$= 10.473 \text{ k}\Omega$$

Hence Thevenin's equivalent of ON Q_2 is,

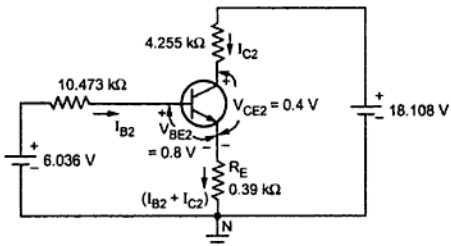


Fig. 3.84

Applying KVL to base-emitter loop,

$$- I_{B2} (10.473) - 0.8 - 0.39 (I_{B2} + I_{C2}) + 6.036 = 0$$

$$\therefore \quad 0.863 I_{B2} + 0.39 I_{C2} = 5.236$$

$$\therefore \quad I_{B2} + 0.0359 I_{C2} = 0.482 \qquad \text{Now multiply by 0.39,}$$

$$\therefore \quad 0.39 I_{B2} + 0.014 I_{C2} = 0.1879 \qquad \ldots(1)$$

Applying KVL to collector emitter loop,

$$- I_{C2} (4.255) - 0.4 - 0.39 (I_{B2} + I_{C2}) + 18.108 = 0$$

$$\therefore \quad - 0.39 I_{B2} - 4.645 I_{C2} = - 17.708 \qquad \ldots (2)$$

Adding equations (1) and (2) we get,

$$- 4.631 I_{C2} = - 17.5201$$

$$\therefore \quad I_{C2} = 3.783 \text{ mA}$$

and $$I_{B2} = 0.346 \text{ mA}$$

From this, the various voltages can be obtained as,

$$V_{EN} = (I_{B2} + I_{C2}) R_E = 1.61 \text{ V}$$

$$V_{CN2} = V_{CE2} + V_{EN} = 0.4 + 1.61 = 2.01 \text{ V}$$

$$V_{BN2} = V_{BE2} + V_{EN} = 0.8 + 1.61 = 2.41 \text{ V}$$

$$V_{BN1} = V_{CN2} \times \frac{R_2}{R_1 + R_2} = 2.01 \times \frac{15}{45} = 0.67 \text{ V}$$

$$V_{BE1} = V_{BN1} - V_{EN} = 0.67 - 1.61 = -0.94 \text{ V}$$

For cut-off, V_{BE1} required is 0 V given, but actually it is still less i.e. – 0.94 V. This ensures Q_1 is indeed OFF.

$$V_{CN1} = \frac{V_{CC} R_1}{(R_C + R_1)} + \frac{V_{BN2} R_C}{(R_C + R_1)} \quad \text{...Using Superposition}$$

$$= \frac{20 \times 30}{(4.7 + 30)} + \frac{2.41 \times 4.7}{(4.7 + 30)} = 17.617 \text{ V}$$

Thus the stable state result is,

$I_{C1} = 0$ mA	$I_{C2} = 3.783$ mA	$I_{B1} = 0$ mA	$I_{B2} = 0.346$ mA	
$V_{CN1} = 17.617$ V	$V_{CN2} = 2.01$ V	$V_{BN1} = 0.67$ V	$V_{BN2} = 2.41$ V	and $V_{EN} = 1.61$ V

b) To find $(h_{fe})_{min}$

For the ON transistor Q_2,

$I_{C2} = 3.783$ mA, $I_{B2} = 0.346$ mA

$$\therefore \quad (h_{fe})_{min} = \frac{I_{C2}}{I_{B2}} = \frac{3.783}{0.346}$$

$$= 10.933 \approx \mathbf{11}$$

c) Calculation of $(I_{CBO})max$

To calculate (I_{CBO})max consider the circuit shown in the Fig. 3.85.

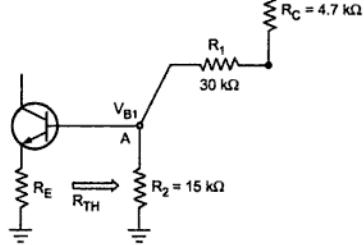


Fig. 3.85

Obtain the Thevenin's equivalent across terminal A and ground. The Thevenin's voltage is $V_A = V_{B1}$ with respect to ground which is calculated earlier.

$$\therefore \quad V_{TH} = V_{B1} = 0.67 \text{ V}$$

Looking into terminals A and ground,

$$R_{TH} = (R_1 + R_C) \parallel R_2 = (34.7) \parallel 15 = \frac{34.7 \times 15}{34.7 + 15}$$

$$= 10.472 \text{ k}\Omega$$

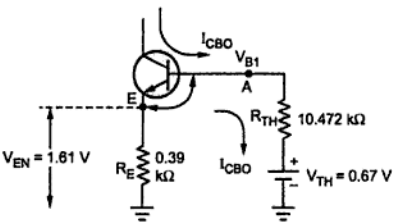


Fig. 3.86

Hence Thevenin's equivalent is :

To find (I_{CBO})max,

V_{BE}(cut-off) = 0 V

and $V_{EN} = 1.61$ V

...Calculated earlier

As $V_{BE} = 0$, base must be also at same potential as emitter with respect to ground.

$$\therefore \quad V_{B1} = V_{EN} = 1.61 \text{ V} \qquad \text{for } (I_{CBO})\text{max},$$

$$\therefore \quad (I_{CBO})\text{max} = \frac{V_{B1} - V_{TH}}{R_{TH}} = \frac{1.61 - 0.67}{10.472 \times 10^3}$$

$$= 89.76 \ \mu\text{A}$$

This is the maximum I_{CBO}.

Example 3.11 : *A collector coupled monostable multivibrator using npn silicon transistors has the following parameters :*

$V_{CC} = 12$ V, $V_B = 3$ V, $R_C = 2$ kΩ, $R_1 = R_2 = R = 20$ kΩ

$h_{fe} = 30$, $r'_{bb} = 200\ \Omega$ *and* $C = 1000$ *pF. Neglect* I_{CBO}.

i) Calculate and plot to the scale the waveshapes at each base and collector.

ii) Find the width of the output pulse.

Solution : For the npn silicon transistors,

$$V_{CE}(\text{sat}) = 0.3 \text{ V and } V_{BE}(\text{sat}) = 0.7 \text{ V} = V_\sigma$$

While $V_{BE}(\text{cut-in}) = 0.5 \text{ V} = V_\gamma$ ...Referring Table 3.1

$$I'_B = \frac{V_{CC} - V_{CE}(\text{sat}) - V_\sigma + V_\gamma}{R_C + r'_{bb}} = \frac{12 - 0.3 - 0.7 + 0.5}{2000 + 200}$$

$$= 5.227 \text{ mA}$$

Hence the overshoot in base voltage of Q_2 is :

$$\delta = I'_B r'_{bb} + V_\sigma - V_\gamma$$
$$= 5.227 \times 10^{-3} \times 200 + 0.7 - 0.5$$
$$= 1.2454 \text{ V}$$
$$V_{C1} = V_{CC} - I'_B R_C = 12 - 5.227 \times 2$$
$$= 1.546 \text{ V}$$

These are the values of various voltages just after circuit returns back to stable state i.e at t = T.

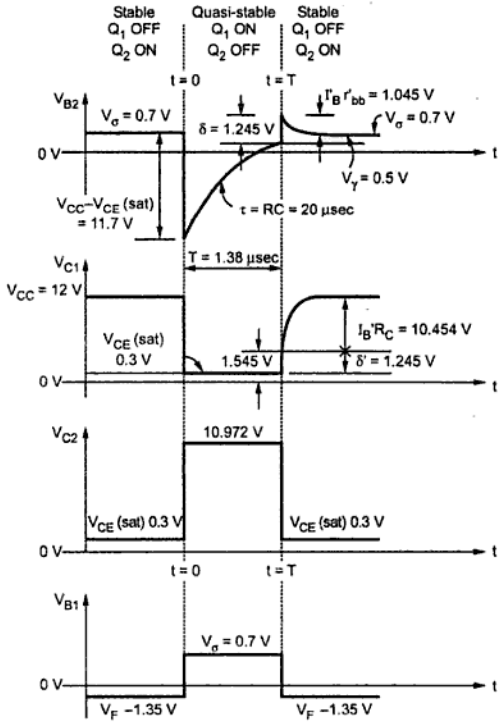


Fig. 3.87

Consider the circuit shown in the Fig. 3.88.

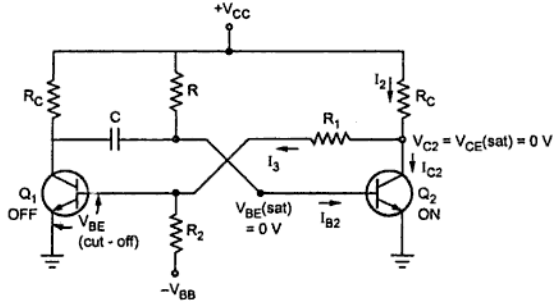


Fig. 3.88

Now $V_{C2} = V_{CC} - I_2 R_C$

$\therefore \quad R_C = \frac{V_{CC} - V_{C2}}{I_2} = \frac{V_{CC} - V_{C2}}{I_3 + I_{C2}}$

Neglecting I_3 and $V_{C2} = V_{CE}(sat) = 0$ V

$\therefore \quad R_C = \frac{6-0}{I_{C2}} = \frac{6}{2}$

$= 3\ k\Omega$

$(I_{B2})_{min} = \frac{I_C}{(h_{fe})_{min}}$

$= \frac{2}{20} = 0.1$ mA

$\therefore \quad I_{B2} = 1.5 \times 0.1 = 0.15$ mA

Current through R is nothing but I_{B2}.

$\therefore \quad I_{B2} = \frac{V_{CC} - V_{BE}(sat)}{R}$

$\therefore \quad 0.15 = \frac{6}{R}$

$\therefore \quad R = \mathbf{40\ k\Omega}$

Now $T = 0.69\ RC$

$\therefore \quad 3000 \times 10^{-6} = 0.69 \times 40 \times 10^{3}\ C$

$\therefore \quad C = 0.108\ \mu F$

As Q_1 is OFF, $I_{B1} = 0$ A

$\therefore$ Current through R_1, $R_2 = I_3$

$$\therefore \quad I_3 = \frac{V_{C2} - (-V_{BB})}{R_1 + R_2} = \frac{V_{BB}}{R_1 + R_2} \quad \ldots (1)$$

$$\text{Also} \quad I_3 = \frac{V_{C2} - V_{BE}\,(\text{cut-off})}{R_1} = \frac{0-(-1)}{R_1} \quad \ldots (2)$$

$$\therefore \quad \frac{V_{BB}}{R_1 + R_2} = \frac{1}{R_1} \quad \ldots (3)$$

As $R_1 = R_2$, $\quad \frac{V_{BB}}{2R_1} = \frac{1}{R_1}$

$\therefore \quad V_{BB} = 2$ V

Under quasi-stable state, Q_1 is ON and Q_2 is OFF. The circuit becomes,

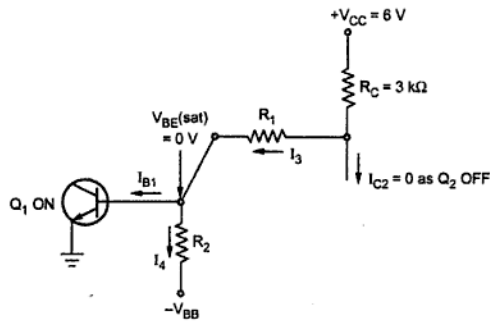


Fig. 3.89

$$I_{B1} = 0.15 \text{ mA in saturation}$$

$$I_3 = \frac{V_{CC} - V_{BE}(\text{sat})}{R_1 + R_C} = \frac{6}{R_1 + 3} \quad \ldots(4)$$

and $$I_4 = \frac{V_{BE}(\text{sat}) - (-V_{BB})}{R_2}$$

$$= \frac{0-(-2)}{R_2} = \frac{2}{R_2} \quad \ldots(5)$$

$$I_{B1} = I_3 - I_4$$

$$= \frac{6}{R_1 + 3} - \frac{2}{R_2} \quad \ldots(6)$$

But $R_1 = R_2 = R'$

$$\therefore \quad 0.15 = \frac{6}{3+R} - \frac{2}{R'}$$

$$\therefore \quad R'(3 + R)0.15 = 6\,R' - 2\,(3 + R')$$

$$\therefore \quad 0.45\,R' + 0.15\,R'^2 = 6R' - 6 - 2\,R'$$

$$\therefore \quad 0.15\,R'^2 - 3.55\,R' + 6 = 0$$

$$\therefore \quad R' = \frac{3.55 \pm \sqrt{(3.55)^2 - 4 \times 0.15 \times 6}}{2 \times 0.15}$$

$$= 21.83,\ 1.831$$

To keep I_3 small so that assumption that I_3 is small in stable state is valid, R' should be large.

$$\therefore \quad R_1 = R_2 = \mathbf{21.83\ k\Omega}$$

Thus all the resistances are known.

Example 3.13 : *A collector coupled monostable multivibrator has the waveform shown in the Fig. 3.90, at the collector of Q_1. The base-spreading resistance of the npn germanium transistors used is 200 Ω. Draw the waveform at the base of Q_2 and calculate R_C.*

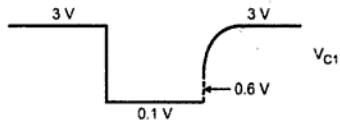


Fig. 3.90

Solution : Assume Q_1 is normally OFF and Q_2 is ON.

The given waveform is at collector of Q_1 i.e. V_{C1}.

$$\therefore \quad V_{CE}(sat) = 0.1\ V \text{ and } V_{CC} = 3\ V$$

The overshoot in $V_{C1} = \delta' = 0.6 - 0.1$

$$= 0.5\ V$$

$$\delta = \delta' = 0.5\ V$$

For germanium, $V_{BE}(sat) = V_\sigma = 0.3$ V

$V_{BE}(cut\text{-}in) = V_\gamma = 0.1$ V

$r'_{bb} = 200\ \Omega$

Now $\delta = I'_B r'_{bb} + V_\sigma - V_\gamma$

$\therefore \quad 0.5 = 200\, I'_B + 0.3 - 0.1$

$\therefore \quad I'_B = 1.5$ mA

While $\delta' = V_{CC} - I'_B R_C - V_{CE}(sat)$

$\therefore \quad 0.5 = 3 - 1.5\times10^{-3} \times R_C - 0.1$

$\therefore \quad R_C = \dfrac{3-0.1-0.5}{1.5\times10^{-3}} = \mathbf{1.6\ k\Omega}$

The waveform at base of Q_2 is shown in the Fig. 3.91.

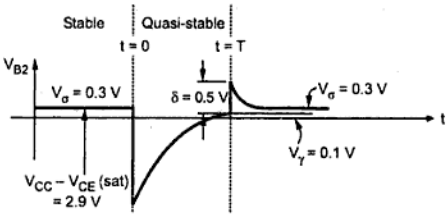


Fig. 3.91

Example 3.14 : *Design an astable multivibrator to meet the following specifications :*

$V_{CC} = 10\ V, \quad I_C = 2\ mA, \quad h_{fe} = 30$

The output should be a square wave of 1 kHz with 60 % duty cycle.

Solution : The duty cycle is given as 60 % i.e. 0.6.

$\therefore \quad \text{Duty cycle} = \dfrac{T_2}{T_1 + T_2}$

$\therefore \quad 0.6 = \dfrac{T_2}{T_1 + T_2}$

$\therefore \quad 0.6\,(T_1 + T_2) = T_2$

$\therefore \quad T_1 = 0.66\, T_2 \qquad \ldots (1)$

$$\therefore \quad 2\times10^{-3} = \frac{10-0.3}{R_C}$$

$$\therefore \quad R_C = 4.85\ k\Omega$$

Now $I_{B2} = 1.5\ (I_{B2})_{min}$

$$= 1.5\ \frac{I_{C2}}{(h_{fe})_{min}} = 1.5\times\frac{2}{30}$$

$$= 0.1\ mA$$

Now $$I_{B2} = \frac{V_{CC}-V_{B2}}{R_2}$$

$$\therefore \quad 0.1\times10^{-3} = \frac{10-0.7}{R_2}$$

$$\therefore \quad R_2 = \mathbf{93\ k\Omega}$$

Now assume $C_1 = C_2 = C$

$$\therefore \quad T_1 = 0.69\ R_1C_1 \text{ and } T_2 = 0.69\ R_2C_2$$

$$\therefore \quad T_2 = 0.69\ R_2\ C$$

$$\therefore \quad 0.6\times10^{-3} = 0.69\times93\times10^{3}\ C$$

$$\therefore \quad C = \mathbf{9.39\ nF}$$

$$\therefore \quad T_1 = 0.69\ R_1\ C$$

$$\therefore \quad 0.4\times10^{-3} = 0.69\ R_1\times9.35\times10^{-9}$$

$$\therefore \quad R_1 = \mathbf{62\ k\Omega}$$

Example 3.15 : *Design a Schmitt trigger circuit to have V_{CC} = 12 V, UTP = 5 V, LTP = 3 V and I_C = 2 mA using two silicon NPN transistors with $h_{FE\ (min)}$ = 100 and $I_2 = 0.1\ I_{C2}$.*

Solution : UTP = 5 V, LTP = 3 V, V_{CC} = 12 V

$$V_i = V_{B2} = \text{UTP} = 5\ \text{V when } Q_2 \text{ is ON.}$$

$$\therefore \quad V_E = V_i - V_{BE1} = V_{B2} - V_{BE2} = 5 - 0.7 = 4.3\ V$$

Let $I_{C2} = I_{E2} = 1\ mA$ ... In ON state

$$\therefore \quad R_E = \frac{V_E}{I_{E2}} = \frac{4.3}{1\times10^{-3}} = \mathbf{4.3\ k\Omega}$$

Now $I_{C2}\ R_{C2} = V_{CC} - V_E - V_{CE2}(sat)$ ... Let $V_{CE2}(sat) = 0.2\ V$

$$1\times10^{-3}R_{C2} = 12 - 4.3 - 0.2$$

$\therefore \quad R_{C2} = \mathbf{7.5\ k\Omega}$

Now $\quad I_2 = 0.1\, I_{C2} = \frac{1}{10} \times 1 \times 10^{-3} = 1 \times 10^{-4}$ A

$\therefore \quad R_2 = \frac{V_{B2}}{I_2} = \frac{5}{1 \times 10^{-4}} = \mathbf{50\ k\Omega}$

$I_{B2} = \frac{I_{C2}}{h_{fe(min)}} = \frac{1 \times 10^{-3}}{100} = 10\ \mu A$

$\therefore \quad I_2 + I_{B2} = \frac{V_{CC} - V_{B2}}{R_{C1} + R_1}$

$\therefore \quad R_{C1} + R_1 = \frac{12 - 5}{1 \times 10^{-4} + 10 \times 10^{-6}} = 63.6363 \times 10^3$ ...(1)

Now $\quad V_{B2} = V_{B1} = \text{LTP} = 3$ V and Q_1 is ON.

$I_1 = \frac{V_{B2}}{R_2} = \frac{3}{50 \times 10^3} = 60\ \mu A$

and $\quad I_{C1} \approx I_{E1} = \frac{V_{B1} - V_{BE1}}{R_E} = \frac{3 - 0.7}{4.3 \times 10^3} = 5.348 \times 10^{-4}$ A

$\therefore \quad V_{CC} = R_{C1}[I_{C1} + I_1] + I_1(R_1 + R_2)$ ...(2)

Using equation (1) in equation (2),

$\therefore \quad V_{CC} = I_{C1}R_{C1} + I_1(R_C + R_1) + I_1R_2$

$\therefore \quad 12 = 5.348 \times 10^{-4} R_{C1} + 60 \times 10^{-6} \times 63.6363 \times 10^3 + 60 \times 10^{-6} \times 50 \times 10^3$

$\therefore \quad R_{C1} = \mathbf{9.6892\ k\Omega}$

$\therefore \quad R_1 = 63.6363 \times 10^3 - 9.6892 \times 10^3 = \mathbf{53.947\ k\Omega}$

Thus when Q_2 is ON,

$V_o = V_{CC} - I_{C2(on)}R_{C2} = 12 - 1 \times 10^{-3} \times 7.5 \times 10^3 = 4.5$ V

And when Q_2 is OFF,

$V_o = V_{CC} = 12$ V

$$\therefore \quad (I_{B2})_{min} = \frac{I_{C2}}{(h_{fe})_{min}} = \frac{5.3501}{20} = \mathbf{0.2675\ mA}$$

Now find actual I_{B2} and verify $I_{B2} > (I_{B2})_{min}$.

Consider the equivalent circuit from collector of Q_1 to base of Q_2, as shown in the Fig. 3.94 (b).

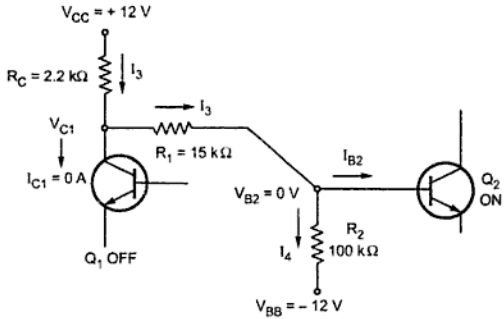


Fig. 3.94 (b)

$$\therefore \quad I_3 = \frac{V_{CC}}{R_C + R_1} = \frac{12}{(2.2+15)\times 10^3}$$

$$= 0.6976\ \text{mA} \qquad \ldots V_{B2} = 0\ \text{V}$$

$$\therefore \quad I_4 = \frac{V_{B2} - V_{BB}}{R_2} = \frac{0-(-12)}{100\times 10^3}$$

$$= 0.12\ \text{mA}$$

$$\therefore \quad I_{B2} = I_3 - I_4 = \mathbf{0.5776\ mA}$$

As $I_{B2} > (I_{B2})_{min}$, the transistor Q_2 is ON and is in saturation.

$$\therefore \quad V_{C1} = V_{CC} - I_3 R_C = 12 - 0.6976 \times 10^{-3} \times 2.2 \times 10^3 = \mathbf{10.4652\ V}$$

Hence the stable state currents and voltages are,

I_{C1} = 0 A	I_{C2} = 5.3501 A	I_{B1} = 0 A	I_{B2} = 0.5776 mA
V_{C1} = 10.4652 V	V_{C2} = 0 V	V_{B1} = − 1.5652 V	V_{B2} = 0 V

Case ii) $V_{CE}(sat) = 0.15$ V, $V_{BE}(sat) = 0.7$ V

For the transistor Q_2, as emitter is ground, $V_{C2} = 0.15$ V and $V_{B2} = 0.7$ V.

Referring to the Fig. 3.94 (a), we write equations to obtain stable state currents and voltages.

Now V_{B1} is due to V_{BB} and V_{C2} hence using Superposition principle,

$$V_{B1} = -V_{BB}\left(\frac{R_1}{R_1+R_2}\right)\Bigg|_{V_{C2}=0V} + V_{C2}\left(\frac{R_2}{R_1+R_2}\right)\Bigg|_{V_{BB}=0V}$$

$$= -12\left[\frac{15}{15+100}\right] + 0.15\left[\frac{100}{15+100}\right] = \mathbf{-1.4348\ V}$$

As V_{B1} is less than V_{BE} (cut-off), the transistor Q_1 is indeed OFF.

$$I_1 = \frac{V_{CC}-V_{C2}}{R_C} = \frac{12-0.15}{2.2\times10^3} = 5.3863\ \text{mA}$$

$$I_2 = \frac{V_{C2}-V_{BB}}{R_1+R_2} = \frac{0.15-(-12)}{(15+100)\times10^3} = 0.1056\ \text{mA}$$

$$\therefore \quad I_{C2} = I_1 - I_2 = \mathbf{5.2806\ mA}$$

$$(I_{B2})_{min} = \frac{I_{C2}}{h_{fe}} = \frac{5.2806}{20} = \mathbf{0.264\ mA}$$

To calculate I_{B2}, consider the Fig. 3.94 (b).

$$I_3 = \frac{V_{CC}-V_{B2}}{R_C+R_1} = \frac{12-0.7}{(2.2+15)\times10^3} = 0.6569\ \text{mA}$$

$$I_4 = \frac{V_{B2}-V_{BB}}{R_2} = \frac{0.7-(-12)}{100\times10^3} = 0.127\ \text{mA}$$

$$\therefore \quad I_{B2} = I_3 - I_4 = \mathbf{0.53\ mA}$$

As $I_{B2} > (I_{B2})_{min}$, the transistor Q_2 is ON.

$$\therefore \quad V_{C1} = V_{CC} - I_3 R_C = 12 - 0.6569 \times 10^{-3} \times 2.2 \times 10^3 = \mathbf{10.5548\ V}$$

Hence the stable state currents and voltages are,

$I_{C1} = 0$ A	$I_{C2} = 5.2806$ mA	$I_{B1} = 0$ A	$I_{B2} = 0.53$ mA
$V_{C1} = 10.5548$ V	$V_{C2} = 0.2$ V	$V_{B1} = -1.4348$ V	$V_{B2} = 0.7$ V

base and collector. (b) Repeat part, (a) taking junction voltages into account, and assume $r'_{bb} = 100\ \Omega$ (Ans. : $R_E = 30\ \Omega$, $R_C = 540\ \Omega$, $R = R_1 = R_2 = 5.31\ k\Omega$)

27. Design a collector coupled astable multivibrator for the following specifications :
Output voltage 10 V peak; $I_{C\ (on)} = 1$ mA; $h_{FE\ (min)} = 100$; $I_{CBO} = 0$; output to be a positive pulse, the duration, of which is 20 μsec, the time between pulses to be 10 μsec.
28. Find the pulse width period and frequency of output of a astable multivibrator given $R_1 = R_2$ and 100 kΩ and $C_1 = C_2 = 0.1\ \mu F$. **(Ans. :** Pulse width = 6.9 ms, T = 13.8 ms, f = 72.4638 Hz)
29. Calculate the stable state currents and voltages for the bistable multivibrator having $V_{CC} = 12$ V, $V_{BB} = -12$ V, $R_{C1} = R_{C2} = 2.2\ k\Omega$, $R_1 = R_2 = 15\ k\Omega$, $R_3 = R_4 = 100\ k\Omega$. Assume that a transistor having a minimum h_{fe} of 20.
30. Design a fixed bias binary, given the following specifications.
$V_{CC} = V_{BB} = 12$ V, $h_{fe}(min) = 20$ and $I_C(sat) = 4$ mA.
Assume n-p-n silicon transistors.
31. Draw and explain the operation of emitter coupled astable multivibrator circuit.
32. Draw and explain the waveforms of emitter coupled astable multivibrator circuit.
33. Derive the expression for the frequency of the emitter coupled astable multivibrator circuit.
34. Draw and explain the operation of Schmitt trigger circuit.
35. Draw the transfer characteristics of Schmitt trigger and explain what is hysteresis.
36. State the applications of Schmitt trigger circuit.
37. With circuit diagram and waveforms explain the operation of Schmitt trigger using two transistors for a sinusodial input.
38. Design a Schmitt trigger circuit for $V_{CC} = 10$ V; UTP = 5 V; LTP = 3 V.
Assume $h_{FE\ min} = 100$ and $I_{C\ (on)} = 1$ mA.
39. Sketch the output waveform of a Schmitt trigger circuit for sine wave input of 12 V peak-to-peak if UTP = 5 V and LTP = 3 V.
40. What is blocking oscillator ? What are its applications ?
41. What is pulse transformer ? Explain its equivalent circuit.
42. Write a note on pulse transformer.
43. Draw an output pulse response of a transformer and explain its characteristics.
44. State the applications of pulse transformer.
45. Draw and explain the operation of base timing blocking oscillator.
46. What are the applicatons of blocking oscillators ?
47. Obtain the pulse width expression for the base timing blocking oscillator.
48. Draw the circuit diagram of a free running blocking oscillator.
49. What are disadvantages of base timing monostable blocking oscillator?
50. Draw and explain the operation of emitter timing monostable blocking oscillator. Draw neat waveforms.

4 High Frequency Amplifiers

4.1 Introduction

At low frequencies we have assumed that the response of transistor to changes of input voltage or current is instantaneous and hence we have neglected the effect of shunt capacitances in the transistor. But this is not in case of high frequencies.

At low frequencies we analyze transistor using h-parameters. But for high frequency analysis the h-parameter model is not suitable for following reasons.

- The values of h-parameters are not constant at high frequencies. Therefore, it is necessary to analyze transistor at each and every frequency, which is impracticable.
- At high frequency h-parameters become complex in nature.

Due to above reasons hybrid π model is used for high frequency analysis of the transistor. This model gives a resonable compromise between accuracy and simplicity to do high frequency analysis of the transistor.

4.2 Hybrid - π Common Emitter Transconductance Model

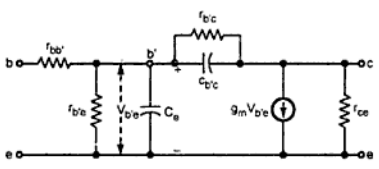


Fig. 4.1 (a) Hybrid-π model for a transistors in the CE configuration

We know that, common emitter circuit is most important practical configuration and hence we have chosen this circuit for the analysis of transistor using hybrid-π model. Fig. 4.1 (a) shows the hybrid-π model for a transistor in the CE configuration. For this model, all parameters (resistances and capacitances) in the model are assumed to be independent of frequency. But they may vary with the quiescent operating point.

4.2.1 Elements in the Hybrid - π Model

$C_{b'e}$ and $C_{b'c}$: We know that, forward biased PN junction exhibits a capacitive effect called the diffusion capacitance. This capacitive effect of normally forward biased base-emitter junction of the transistor is represented by $C_{b'e}$ or C_e in the hybrid-π model. Thus the diffusion capacitance C_e connected between B' and E represents the excess minority carrier storage in the base.

The reverse bias PN junction exhibits a capacitive effect called the transition capacitance. This capacitive effect of normally reverse biased collector base junction of the transistor is represented by $C_{b'c}$ or C_C in the hybrid-π model.

$r_{bb'}$: The internal node b' is physically not accessible bulk node B represents external base terminal. The bulk resistance between external base terminal and internal node B' is represented as $r_{bb'}$, as shown in the Fig. 4.1 (b). This resistance is called as **base spreading resistance.**

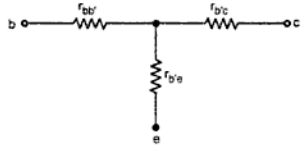


Fig. 4.1 (b) Virtual base

$r_{b'e}$: The resistance $r_{b'e}$ is that portion of the base emitter which may be thought of as being "in series with" the collector junction. This establishes a virtual base B' for the junction capacitances to be connected to instead of b. This is illustrated in Fig. 4.1 (b).

$r_{b'c}$: We know that, due to Early effect, the varying voltages across the collector to emitter junction results in base-width modulation. A change in the effective base width causes the emitter current to change. This feedback effect between output and input is taken into account by connecting $g_{b'c}$ or $r_{b'c}$ between b' and c.

g_m : Due to the small changes in voltage $V_{b'e}$ across the emitter junction, there is excess-minority carrier concentration injected into the base which is proportional to the $V_{b'e}$. Therefore, resulting small signal collector current, with collector shorted to the emitter is also proportional to the $V_{b'e}$. This effect accounts for the current generator $g_m V_{b'e}$ in Fig. 4.1 (a).

g_m is called transconductance and it is given as

$$g_m = \frac{\Delta I_c}{\Delta V_{b'e}} \text{ at a constant } V_{CE}$$

r_{ce} : The r_{ce} is the output resistance. It is also the result of the early effect.

4.2.2 Hybrid - π Parameter Values

Table 4.1 shows the typical values for hybrid-π parameters at room temperature and for I_c = 1.3 mA.

Parameter	Meaning	Value
g_m	Mutual conductance of transistor	50 mA/V
$r_{bb'}$	Base spreading resistance	100 Ω
$r_{b'e}$ or	Resistance between B' and E	1 kΩ
$g_{b'e}$	Conductance between B' and E	1 m mho
$r_{b'c}$ or	Resistance of reverse biased P-N junction between base and collector	4 MΩ
$g_{b'c}$	Conductance of reverse biased P-N junction between base and collector	0.25×10^{-6} mho
r_{ce} or	Output resistance between C and E	80 kΩ
g_{ce}	Conductance between C and E	12.5×10^{-6} mho
C_e	Junction capacitance between B and E	100 pF
C_C	Junction capacitance between base and collector	3 pF

Table 4.1

4.3 Determination of Hybrid-π Conductances

Let us see how we can obtain all the resistive components in the hybrid-π model from the h-parameters in the CE configuration.

4.3.1 Transistor Transconductance g_m

Let us consider, a p-n-p transistor in the CE configuration with V_{CC} bias in the collector circuit as shown Fig. 4.2.

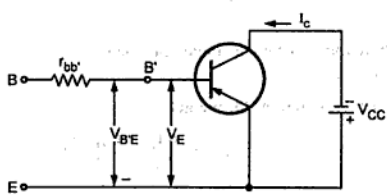


Fig. 4.2 Pertaining to the derivation of g_m

The transconductance is nothing but the ratio of change in the collector current due to small changes in the voltage $V_{B'E}$ across the emitter junction. It is given as

$$g_m = \left.\frac{\partial I_c}{\partial V_{B'E}}\right|_{V_{CE}} \quad \ldots (1)$$

We know that, the collector current in active region is given as

$$I_c = I_{CO} - \alpha I_E$$

and therefore

$$\partial I_c = \alpha \partial I_e \quad \because I_{CO} = \text{Constant}$$

Substituting value of ∂I_C in equation (1) we get,

$$g_m \equiv \alpha \frac{\partial I_E}{\partial V_{B'E}} \equiv \alpha \frac{\partial I_E}{\partial V_E} \quad \because V_E = V_{B'E} \quad \ldots (2)$$

The emitter diode resistance, r_e is given as

$$r_e = \frac{\partial V_E}{\partial I_E}$$

$$\frac{1}{r_e} = \frac{\partial V_E}{\partial I_E}$$

Substituting r_e in place of $\partial I_e / \partial V_E$ we get,

$$g_m = \frac{\alpha}{r_e} \quad \ldots (3)$$

The emitter diode is a forward biased diode and its dynamic resistance is given as

$$r_e = \frac{V_T}{I_E} \quad \ldots (4)$$

where V_T is the "volt equivalent of temperature", defined by

$$V_T = \frac{kT}{q}$$

where k is the Boltzmann constant in joules per degree kelvin (1.38×10^{-23} J/°K) is the electronic charge (1.6×10^{-19} C).

Substituting value of r_e in equation (3) we get,

$$g_m = \frac{\alpha I_E}{V_T} = \frac{I_{CO} - I_C}{V_T} \quad \because I_c = I_{CO} - \alpha I_E$$

For pnp transistor I_c is negative. For an npn transistor I_c is positive, but the foregoing analysis (with $V_E = +V_{BE}$) leads to $g_m = (I_c - I_{CO}) / V_T$.

Hence, for either type of transistor, g_m is positive.

$$\therefore \quad g_m = \frac{I_c - I_{CO}}{V_T} \qquad \because I_c >> I_{CO} \qquad \ldots (5)$$

Substituting value of V_T in equation (5) we get

$$g_m = \frac{I_c\, q}{k\, T} = \frac{I_c \times 1.6 \times 10^{-19}}{1.38 \times 10^{-23}\, T}$$

$$= \frac{11600\, I_c}{T} \qquad \ldots (6)$$

From equation (6) we can say that transconductance g_m is directly proportional to collector current and inversely proportional to temperature.

At room temperature, 300 °K

$$g_m = \frac{1160\, I_c}{300} = \frac{I_c}{26 \times 10^{-3}}$$

$$= \frac{I_c\,|\text{mA}|}{26} \qquad \ldots (7)$$

For I_c = 1.3 mA, g_m = 0.05 mho or 50 mA/V. For I_c = 7.8 mA, g_m = 0.3 mho or 300 mA/V. These values are much larger than the transconductances obtained with FETs.

4.3.2 The Input Conductance $g_{b'e}$

Fig. 4.3 (a) and (b) shows the hybrid-π model and the h-parameter model for CE configuration at low frequency, respectively. At low frequency, all capacitors are negligible and hence not drawn in Fig. 4.3 (a).

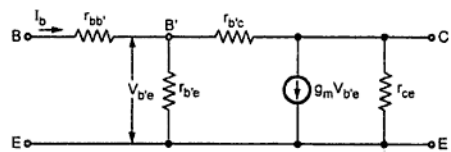


Fig. 4.3 (a) Hybrid-π model for CE configuration at low frequency

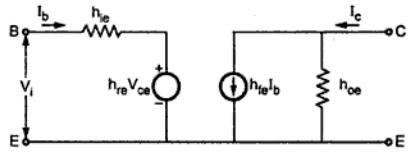


Fig. 4.3 (b) h-parameter model for CE configuration at low frequency

First consider the h-parameter model for CE configuration (Fig. 4.3 (b)). Applying KCL to the output circuit we get,

$$dzI_c = h_{fe} I_b + h_{oe} V_{ce}$$

Making $V_{ce} = 0$, ie. output short circuit, the short circuit current gain h_{fe} is defined as

$$h_{fe} = \frac{I_c}{I_b} \qquad \ldots (8)$$

Now, consider the hybrid-π model for CE configuration. Looking at Table 4.1 we have $r_{b'c} = 4\ M\Omega >> r_{b'e}$. Hence I_b flows into $r_{b'e}$ and $V_{b'e} = I_b\ r_{b'e}$. Similarly, as $r_{b'c}$ is very large $I_c = g_m V_{b'e}$.

$$\therefore \quad I_c = g_m\ V_{b'e}$$

$$= g_m\ I_b\ r_{b'e} \qquad \because\ V_{b'e} = I_b\ r_{b'e}.$$

$$\therefore \quad \frac{I_c}{I_b} = g_m\ r_{b'e} \qquad \ldots (9)$$

Substituting value of I_c/I_b in equation (8) we get

$$h_{fe} = g_m\ r_{b'e}$$

or

$$r_{b'e} = \frac{h_{fe}}{g_m} \quad \text{or} \quad g_{b'e} = \frac{g_m}{h_{fe}} \qquad \ldots (10)$$

From equation (5) we know that $g_m = I_c / V_T$

$$\therefore \quad r_{b'e} = \frac{h_{fe}\ V_T}{|I_c|}$$

or

$$g_{b'e} = \frac{|I_c|}{V_T\ h_{fe}} \qquad \ldots (11)$$

Looking at equation (11), we can say that, over the range of currents for which h_{fe} remains fairly constant, $r_{b'e}$ is directly proportional to temperature and inversely proportional to collector current.

4.3.3 The Feedback Conductance $g_{b'c}$

Let us consider h-parameter model for CE configuration with input open circuit ($I_b = 0$), V_i given as

$$V_i = h_{re} V_{ce} \quad \ldots (12)$$

Now consider the hybrid-π model for CE configuration as shown in Fig. 4.4.

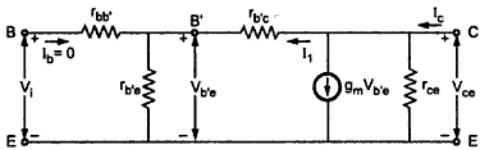


Fig. 4.4

With $I_b = 0$, V_{ce} can be given as

$$V_{ce} = I_1 (r_{b'c} + r_{b'e})$$

$$\therefore \quad I_1 = \frac{V_{ce}}{r_{b'c} + r_{b'e}} \quad \ldots (13)$$

The voltage between B' and E, $V_{b'e}$ can be given as

$$V_{b'e} = I_1 r_{b'e}$$

$$\therefore \quad V_{b'e} = r_{b'e} \frac{V_{ce}}{r_{b'c} + r_{b'e}} \quad \ldots (14)$$

With

$$I_b = 0$$

$$V_i = V_{b'e}$$

$$= \frac{r_{b'e} V_{ce}}{r_{b'c} + r_{b'e}}$$

Substituting value of V_i in equation (12) we get,

$$h_{re} V_{ce} = \frac{r_{b'e} V_{ce}}{r_{b'c} + r_{b'e}}$$

$$\therefore \quad h_{re} = \frac{r_{b'e}}{r_{b'c} + r_{b'e}}$$

$$\therefore \quad r_{b'e} = h_{re} r_{b'c} + h_{re} r_{b'e}$$

$$\therefore \quad (1 - h_{re}) r_{b'e} = h_{re} r_{b'c}$$

$$\therefore \quad r_{b'c} = \left(\frac{1 - h_{re}}{h_{re}}\right) r_{b'e}$$

$$= \frac{r_{b'e}}{h_{re}} \qquad \because 1 - h_{re} \approx 1 \qquad \ldots (15)$$

$$\therefore \quad g_{b'c} = \frac{h_{re}}{r_{b'e}} = h_{re}\, g_{b'e}$$

Substituting the value of $r_{b'e}$ from equation (11) we get,

$$r_{b'c} = \frac{h_{fe} V_T}{|I_c|\, h_{re}}$$

$$\therefore \quad g_{b'c} = \frac{|I_c|\, h_{re}}{h_{fe} V_T} \qquad \ldots (16)$$

4.3.4 The Base Spreading Resistance $r_{bb'}$

Let us consider h-parameter model for CE configuration. The input resistance with output shorted ($V_{ce} = 0$) is h_{ie}. With hybrid-π model input resistance with output shorted is $r_{bb'} + r_{b'e}$

$$\therefore \quad h_{ie} = r_{bb'} + r_{b'e}$$

$$\therefore \quad r_{bb'} = h_{ie} - r_{b'e} \qquad \ldots (17)$$

Substituting value of $r_{b'e}$ from equation (11) we get,

$$r_{bb'} = h_{ie} - \frac{h_{fe} V_T}{I_c} \qquad \ldots (18)$$

4.3.5 The Output Resistance g_{ce}

Using h-parameters the output conductance is given as

$$h_{oe} = \frac{I_c}{V_{ce}} \qquad \ldots (19)$$

Now, consider hybrid-π model for CE configuration, shown in Fig. 4.4. Applying KCL to the output circuit we get

$$I_c = \frac{V_{ce}}{r_{ce}} + g_m V_{b'e} + I_1$$

Substituting value of I_1 from equation (13) we get,

$$I_c = \frac{V_{ce}}{r_{ce}} + g_m V_{b'e} + \frac{V_{ce}}{r_{b'c} + r_{b'e}}$$

Substituting value of $V_{b'e}$ from equation (14) we get,

$$I_c = \frac{V_{ce}}{r_{ce}} + g_m \left(\frac{r_{b'e} V_{ce}}{r_{b'c} + r_{b'e}} \right) + \frac{V_{ce}}{r_{b'c} + r_{b'e}}$$

Dividing both sides by V_{ce} we get

$$\frac{I_c}{V_{ce}} = \frac{1}{r_{ce}} + \frac{g_m r_{b'e}}{r_{b'c} + r_{b'e}} + \frac{1}{r_{b'c} + r_{b'e}}$$

$$= \frac{1}{r_{ce}} + \frac{h_{fe}}{r_{b'c} + r_{b'e}} + \frac{1}{r_{b'c} + r_{b'e}} \quad \because h_{fe} = g_m r_{b'e} \text{ (eq. 10)}$$

$$= \frac{1}{r_{ce}} + \frac{(h_{fe} + 1)}{r_{b'c} + r_{b'e}} \quad \ldots (20)$$

$$= \frac{1}{r_{ce}} + \frac{h_{fe}}{r_{b'c} + r_{b'e}} \quad \because h_{fe} >> 1 \quad \ldots (21)$$

Substituting value of $\frac{I_c}{V_{ce}}$ in equation (19) we get

$$h_{oe} = \frac{1}{r_{ce}} + \frac{h_{fe}}{r_{b'c} + r_{b'e}} \quad \ldots (22)$$

$$= \frac{1}{r_{ce}} + \frac{h_{fe}}{r_{b'c}} \quad \because r_{b'c} >> r_{b'e} \quad \ldots (23)$$

$\therefore \quad h_{oe} = g_{ce} + g_{b'c} h_{fe}$

$\therefore \quad \frac{1}{r_{ce}} = g_{ce} = h_{oe} - g_{b'c} h_{fe} \quad \ldots (24)$

4.3.6 Summary

The Table 4.2 summarizes the relation between hybrid-π and h-parameters

Sr. No.	Parameter relation
1.	$g_m = \frac{I_c}{V_T}$
2.	$r_{b'e} = \frac{h_{fe}}{g_m}$
3.	$r_{bb'} = h_{ie} - r_{b'e}$
4.	$r_{b'c} = \frac{r_{b'e}}{h_{re}}$
5.	$g_{ce} = \frac{1}{r_{ce}} = h_{oe} - g_{b'c} h_{fe}$

Table 4.2 Relation between hybrid-π and h-parameters

4.4 Hybrid-π Capacitances

We have seen that the hybrid-π model for transistor includes two capacitances : Transition capacitance and diffusion capacitance. The transition capacitance $C_c = C_{b'c}$ is measured as a CB output capacitance with input open ($I_E = 0$), and is usually specified by manufacturers as C_{ob}. The diffusion capacitance is represented by $C_{b'e}$ or C_e in the hybrid-π model. It is the summation of the emitter diffusion capacitance C_{De} and the emitter junction capacitance C_{Te}. For a forward biased emitter junction, C_{De} is usually much larger than C_{Te} and hence

$$C_e = C_{De} + C_{Te} \approx C_{De}$$

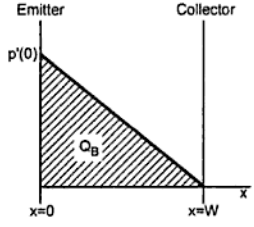


Fig. 4.5

Let us see how C_{De} is proportional to the emitter bias current I_E and independent of temperature.

The Fig. 4.5 shows the minority carrier charge distribution in the base region. It gives the injected hole concentration vs distance in the base region of a p-n-p transistor.

The base width W is assumed to be small compared with the diffusion length L_B of the minority carriers. Since the collector junction is reversed-biased, the injected charge concentration p′ at the collector junction is zero. If $W << L_B$, the p′ varies almost linearly from the value p′(0) at the emitter to zero at the collector, as shown in the Fig. 4.5. The stored base charge Q_B can be given as

$$Q_B = \frac{1}{2} P'(0) A W q \quad \ldots (1)$$

where $\frac{1}{2} p'(0)$ is the average concentration

A is the base cross-sectional area

WA is the volume of the base and

q is the electronic charge

The diffusion current is given by

$$I = - Aq D_B \frac{dp'}{dx}$$

$$= Aq D_B \frac{p'(0)}{W} \quad \ldots (2)$$

Combining equations (1) and (2) we get

$$Q_B = \frac{IW^2}{2D_B} \quad \ldots(3)$$

The static emitter diffusion capacitance C_{De} is defined as the rate of change of Q_B with respect to emitter voltage V. Therefore,

$$C_{De} = \frac{dQ_B}{dV} = \frac{W^2}{2D_B}\frac{dI}{dV}$$

$$= \frac{W^2}{2D_B}\frac{I}{r_e} \quad \ldots(4)$$

where $r_e = dV/dI = V_T/I_E$ is the emitter junction incremental resistance.

$$\therefore \quad C_{De} = \frac{W^2 I_E}{2D_B V_T}$$

$$= g_m \frac{W^2}{2D_B} \quad \ldots(5)$$

The above equation indicates that the diffusion capacitance is proportional to the emitter bias current I_E.

Experimentally, C_e is determined from a measurement of f_T, the frequency at which the CE short-circuit current gain drops to unity. It is given as

$$C_e \approx \frac{g_m}{2\pi f_T} \quad \ldots(6)$$

4.5 Validity of Hybrid-π Model

Assuming that V_{BE} changes so slowly with time that the minority-carrier charge distribution in the base region is always triangular, as shown in the Fig. 4.5.

In such case, the slope of minority carrier charge distribution curve at x = 0 is the same as at x = W and hence collector current remains equal to the emitter current. Hence the hybrid-π model is valid under dynamic condition only when the rate of change of V_{BE} is so small that the base increment current I_b is small in comparison with the collector incremental current I_c. It is proved that the elements of Fig. 4.1 (a) are frequency independent provided that

$$2\pi f \frac{W^2}{6D_B} << 1 \quad \ldots(1)$$

From equation (5) of section 4.4 we have,

$$\frac{W^2}{6D_B} = \frac{C_e}{3g_m}$$

and from equation (6) of section 4.4 we have,

$$\frac{W^2}{6 D_B} = \frac{C_e}{3 g_m} = \frac{1}{6\pi f_T}$$

Thus equation (1) becomes

$$2\pi f \times \frac{1}{6\pi f_T} << 1$$

$$\therefore \quad f << 3 f_T \qquad \ldots(2)$$

The equation (2) shows that the hybrid-π model is valid for frequencies upto approximately $f_T/3$.

4.6 Variation of Hybrid Parameters with $|I_c|$, $|V_{CE}|$ and Temperature

In previous two sections we have derived expressions for the hybrid-π conductances and capacitances interms of the low-frequency h-parameters and other transistor parameters, such as base width or the diffusion constant for minority carriers in the base.

The hybrid parameters are dependent on the magnitudes of I_c and V_{CE} and the temperature. The Table 4.3 summarizes the dependence of hybrid parameters such as g_m, $r_{bb'}$, $r_{b'e}$, c_e, c_C, h_{fe} and h_{ie} on the collector current magnitude $|I_c|$, the collector to emitter voltage magnitude $|V_{CE}|$, and the temperature.

Parameter	Variation with Increasing		
	$\|I_c\|$	$\|V_{CE}\|$	T
g_m	Increases-proportional to $\|I_c\|$	Independent	Decreases - inversely proportional to T i.e. 1/T
$r_{bb'}$	Decreases - due to conductivity modulation of the base		Increases - due to decrease in conductivity as a result of decrease in the mobility of majority and minority carriers.
$r_{b'e}$	Decreases - inversely proportional to $\|I_c\|$ i.e. $1/\|I_c\|$	Increases	Increases

C_e	Increases - proportional to $\|I_c\|$	Decreases	
C_c	Independent	Decreases	Independent
h_{fe}	Increases for smaller values of $\|I_c\|$ and decreases with higher values of $\|I_c\|$	Increases - due to the increase of transistor α as a result of decrease of the base width and the reduction in recombination	Increases
h_{ie}	Decreases - inversely proportional to $\|I_c\|$ i.e. $1/\|I_c\|$	Increases	Increases

Table 4.3 Dependence of hybrid parameters upon current voltage and temperature

Note : No entry in Table 4.3 means that the parameter varies with $|I_c|$, $|V_{CE}|$, or temperature in a complicated fashion.

4.7 High Frequency Analysis of CE Amplifier

4.7.1 CE Short-Circuit Current Gain

Consider a single stage CE transistor amplifier with load resistor R_L, as shown in the Fig. 4.6.

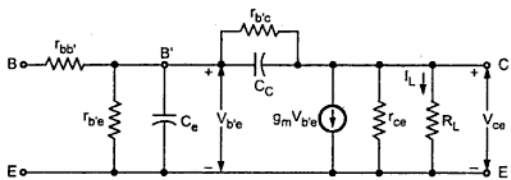


Fig. 4.6 The hybrid-π circuit for a single transistor with a resistive load R_L

For the analysis of short circuit current gain we have to assume $R_L = 0$. With $R_L = 0$, i.e. output short circuited r_{ce} becomes zero, $r_{b'e}$, C_e and $C_{b'c}$ appear in parallel.

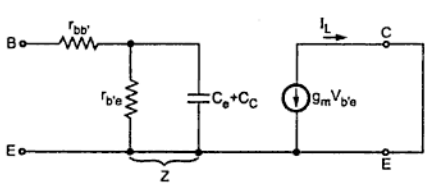


Fig. 4.7 Simplified hybrid-π model for short circuit CE transistor

When C_C ($C_{b'c}$) appears between base and emitter, it is known as **Miller capacitance** (C_M). Its admittance is given as

$$j\omega C_M = \frac{i_{C_{b'C}}}{V_{b'e}} j\omega C_{b'c} (1 + g_m R_L)$$

Hence, the Miller capacitance is $C_M = C_{b'c} (1 + g_m R_L)$

Here, $R_L = 0$

$\therefore \quad C_M = C_{b'c} (C_C)$

As $r_{b'c} >> r_{b'e}$, $r_{b'c}$ is neglected. With these approximation we get simplified hybrid-π model for short circuit CE transistor, as shown in the Fig. 4.7.

Parallel combination of $r_{b'c}$, and $(C_e + C_C)$ is given as

$$Z = \frac{r_{b'c} \times \frac{1}{j\omega(C_e + C_C)}}{r_{b'e} + \frac{1}{j\omega(C_e + C_C)}}$$

$$= \frac{r_{b'e}}{1 + j\omega r_{b'e} (C_e + C_C)} \quad \ldots (1)$$

This simplifies hybrid-π model as shown in the Fig. 4.8.

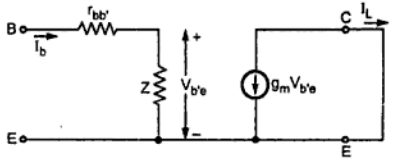


Fig. 4.8 Further simplified hybrid-π model

Look at Fig. 4.8 we can write $V_{b'e} = I_b Z$

$\therefore \quad Z = \frac{V_{b'e}}{I_b} \quad \ldots (2)$

The current gain for the circuit shown in Fig. 4.8 can be given as

$$A_i = \frac{I_L}{I_b} = \frac{-g_m V_{b'e}}{I_b} \quad \because I_L = -g_m V_{b'e}$$

Substituting value of $V_{b'e} / I_b$ from equation (2) we get,

$$A_i = -g_m Z$$

$$= \frac{-g_m r_{b'e}}{1 + j\omega r_{b'e} (C_e + C_C)} \quad \ldots (3)$$

From equation (10) of section 4.3 we know that $h_{fe} = g_m r_{b'e}$.

$\therefore \quad A_i = \frac{-h_{fe}}{1 + j\omega r_{b'e} (C_e + C_C)} \quad \ldots (4)$

$$\therefore \quad f_T = \frac{g_m}{2\pi (C_e + C_C)} \quad \ldots (12)$$

Since $C_e >> C_C$ we can write

$$f_T = \frac{g_m}{2\pi C_e} \quad \ldots (13)$$

Example 4.1 : *At I_C = 1 mA and V_{CE} = 10 V, a certain transistor data shows $C_C = C_{b'c}$ = 3 pF, h_{fe} = 200 and ω_T = – 500 M rad/sec. Calculate g_m, $r_{b'e}$, $C_e = C_{b'e}$ and ω_β.*

Solution : i) $$g_m = \frac{I_C}{V_T} = \frac{1\text{ mA}}{26\text{ mV}}$$

$$= 38.46\text{ mA/V}$$

ii) $$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{200}{38.46 \times 10^{-3}}$$

$$= 5.20\text{ k}\Omega$$

iii) $$(C_e + C_C) = \frac{g_m}{2\pi f_T} = \frac{g_m}{\omega_T} = \frac{38.46 \times 10^{-3}}{500 \times 10^6}$$

$$(C_e + C_C) = 76.92\text{ pF}$$

$$\therefore \quad C_{b'e} = C_e = 76.92\text{ pF} - 3\text{ pF} = 73.92\text{ pF}$$

iv) We know that,

$$f_T = h_{fe}\, f_\beta$$

$$\therefore \quad 2\pi f_T = h_{fe}\, 2\pi f_\beta$$

$$\therefore \quad \omega_T = h_{fe}\, \omega_\beta$$

$$\omega_\beta = \frac{\omega_T}{h_{fe}} = \frac{500 \times 10^6}{200}$$

$$= 2.5\text{ M rad/sec}$$

Example 4.2 : *Short circuit CE current gain of transistor is 25 at a frequency of 2 MHz if f_β = 200 kHz calculate i) f_T ii) h_{fe} iii) Find $|A_i|$ at frequency of 10 MHz and 100 MHz.*

Solution : i) $$f_T = |A_i| \times f = 25 \times 2 \times 10^6$$

$$= 50\text{ MHz}$$

ii) $$h_{fe} = \frac{f_T}{f_\beta} = \frac{50\text{ MHz}}{200\text{ kHz}} = 250\text{ kHz}$$

iii) $$|A_i| = \frac{h_{fe}}{\sqrt{1+\left(\frac{f}{f_\beta}\right)^2}}$$

At $f = 10$ MHz

$$|A_i| = \frac{250}{\sqrt{1+\left(\frac{10\times10^6}{200\times10^3}\right)^2}} = 5$$

At $f = 100$ MHz

$$|A_i| = \frac{250}{\sqrt{1+\left(\frac{100\times10^6}{200\times10^3}\right)^2}} = 0.5$$

4.7.2 Current Gain with Resistive Load

Consider a single stage CE transistor amplifier with load resistance R_L, as shown in the Fig. 4.10.

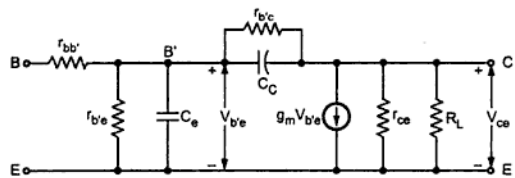


Fig. 4.10 The hybrid-π model for a single transistor with resistive load

In the output circuit r_{ce} is in parallel with R_L. For high frequency amplifiers R_L is small as compared to r_{ce} and hence we can neglect r_{ce}. Using Miller's theorem, we can split $r_{b'c}$ and C_C to simplify the analysis.

Fig. 4.11 shows the simplified hybrid-π model for a single transistor with resistive load.

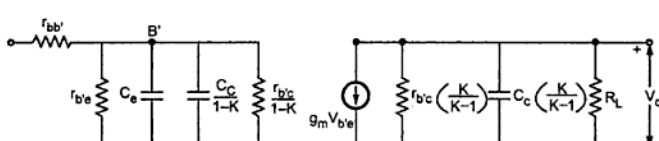


Fig. 4.11 Simplified hybrid-π model for a single transistor with resistive load

Further simplification of input circuit

Amplifier gain K is given as

$$K = \frac{V_o}{V_{b'e}}$$

where $V_o = -g_m V_{b'e} R_L$

$\therefore$ $K = -g_m R_L$

Assuming $R_L = 2\ K$ and $g_m = 50\ mA/V$

we get $K = -100$

and

$$\frac{r_{b'c}}{1-K} = \frac{4\ M\Omega}{1-(-100)} \text{ (Referring Table 4.1)}$$

$$\approx 40\ K$$

The value $r_{b'c}/(1 - K) >> r_{b'e}$ (1 K) and hence $r_{b'c}/(1 - K)$ which is in parallel with $r_{b'e}$ can be neglected.

C_C also resolved by Miller's theorem.

$\therefore$ $$\frac{\frac{1}{j\omega C_C}}{1-K} = \frac{1}{j\omega C_C (1 + g_m R_L)}$$

$\therefore$ $$\frac{C_C}{1-K} = C = C_C (1 + g_m R_L) \quad \ldots (14)$$

As C_e and C are in parallel, the total equivalent capacitance is given as

$$C_{eq} = C_e + C_C (1 + g_m R_L) \quad \ldots (15)$$

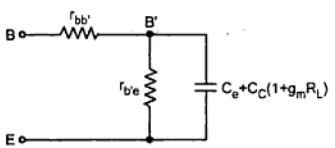


Fig. 4.12

From equation (15) we can say that input capacitance is increased. $C_C (1 + g_m R_L)$ is called **Miller capacitance** (C_M). With these approximations input circuit becomes, as shown in Fig. 4.12.

Further simplification for output circuit

At output circuit value of C_C can be calculated as

$$\frac{\frac{1}{j\omega C_C}}{\frac{K-1}{K}} \approx \frac{1}{j\omega C_C} \quad \because K = -100$$

$$\therefore \quad C_C\left(\frac{K}{K-1}\right) \approx C_C$$

Looking at Fig. 4.11 we can see that there are two independent time constants, one associated with the input circuit and one associated with the output circuit. As input capacitance $[C_e + C_C (1 + g_m R_L)]$ is very high in comparison with output capacitance $[C_C]$. As a results, output time constant is negligible in comparison with the input time constant and may be ignored.

$$r_{b'c}\left(\frac{K}{K-1}\right) \approx r_{b'c} \quad \because K = -100$$

$$\approx 4\ M\Omega$$

This value of $r_{b'c}$ is very high in comparison with load resistance R_L which is parallel with $r_{b'c}$. Hence $r_{b'c}$ can be ignored.

Fig. 4.13 shows the further simplified hybrid-π model of single transistor in CE configuration with load resistance.

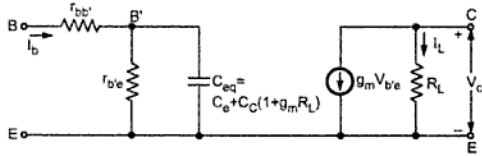


Fig. 4.13 Further simplified hybrid-π model for CE with R_L

Parallel combination of $r_{b'c}$ and C_{eq} is given as

$$Z = \frac{r_{b'e} \times \frac{1}{j\omega C_{eq}}}{r_{b'e} + \frac{1}{j\omega C_{eq}}}$$

$$= \frac{r_{b'e}}{1 + j\omega r_{b'e} C_{eq}} \quad \ldots (16)$$

where $$\frac{I_b}{I_s} = \frac{R_s}{R_s + r_{bb'} + Z}$$

$$\therefore \quad A_{is} = \frac{-g_m Z R_s}{R_s + r_{bb'} + Z} \qquad \ldots (22)$$

where $$Z = \frac{r_{b'e}}{1 + j\,\omega r_{b'e} C_{eq}}$$

At low frequency we can neglect the capacitance and hence Z is given as

$$Z = r_{b'e}$$

Then A_{is}, at low frequency $$= \frac{I_L}{I_s} = \frac{-g_m r_{b'e} R_s}{R_s + r_{bb'} + r_{b'e}}$$

$$\therefore \quad A_{is(low)} = \frac{-h_{fe} R_s}{R_s + r_{bb'} + r_{b'e}} \quad \because h_{fe} = g_m r_{b'e} \text{ (Refer eq. 10 of section 4.3.2)} \qquad \ldots(23)$$

$$= \frac{-h_{fe} R_s}{R_s + h_{ie}} \quad \because h_{ie} = r_{bb'} + r_{b'e} \text{ (Refer eq. 17 of section 4.3.4)} \qquad \ldots (24)$$

It is important to note that the $A_{is\,(low)}$ independent of R_L.

4.7.4 Voltage Gain Including Source Resistance

Fig. 4.17 shows the equivalent circuit with source resistance, assuming voltage source.

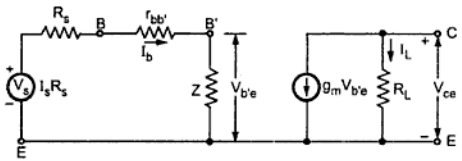


Fig. 4.17 Equivalent circuit assuming voltage source

$$A_{vs} = \frac{V_o}{V_s} = \frac{I_L R_L}{I_s R_s} = \frac{-g_m Z R_s}{R_s + r_{bb'} + Z} \times \frac{R_L}{R_s}$$

$$= \frac{-g_m Z R_L}{R_s + r_{bb'} + Z} \qquad \ldots (25)$$

At low frequency $$A_{vs\,low} = \frac{I_L}{I_s}\frac{R_L}{R_s} = \frac{-h_{fe} R_s}{R_s + h_{ie}} \times \frac{R_L}{R_s}$$

$$= \frac{-h_{fe} R_L}{R_s + h_{ie}} \quad \ldots (26)$$

It is important to note that the $A_{vs\ low}$ increases linearly with R_L.

4.7.5 The Cut-off Frequency Including Source Resistance

$$A_{is\ high} = \frac{A_{is\ high}}{1 + j\left(\frac{f}{f_H}\right)}$$

$$A_{vs\ high} = \frac{A_{vs\ high}}{1 + j\left(\frac{f}{f_H}\right)}$$

where, $$f_H = \frac{1}{2\pi R_{eq} C_{eq}} \quad \ldots (27)$$

where, $$R_{eq} = r_{b'e} \parallel (r_{bb'} + R_s)$$

and $$C_{eq} = C_e + C_C [1 + g_m R_L]$$

It is important to note that f_H increases as the load resistance is decreased because C is a linear function of R_L. At $R_L = 0$, the 3 dB frequency is finite. It is given as

For $R_L = 0$:

$$f_H = \frac{1}{2\pi R(C_e + C_C)}$$

$$= \frac{f_T}{g_m R} \quad \because \quad f_T = \frac{g_m}{2\pi(C_e + C_C)} \text{ (Refer eq. 12 of section 4.7.1.3)}$$

$$= \frac{h_{fe} f_\beta}{g_m R} \quad \because \quad f_T = h_{fe} f_\beta \text{ (Refer eq. 11 of section 4.7.1.3)}$$

$$= \frac{f_\beta}{g_{b'e} R} \quad \because \quad g_{b'e} = \frac{g_m}{h_{fe}} \text{ (Refer eq. 10 of section 4.3.2)}$$

4.8 Gain Bandwidth Product

4.8.1 Gain Bandwidth Product for Voltage

The gain bandwidth product for voltage gain is given as

$$|A_{vs\ low}\ f_H| = |A_{vso}\ f_H| = \frac{-h_{fe} R_L}{R_s + h_{ie}} \times \frac{1}{2\pi R_{eq} C_{eq}}$$

$$= \frac{-h_{fe} R_L}{R_s + h_{ie}} \times \frac{1}{2\pi C_{eq} \left[\frac{r_{b'e} (r_{bb'} + R_s)}{r_{b'e} + r_{bb'} + R_s}\right]}$$

$$= \frac{-h_{fe} R_L}{R_s + h_{ie}} \times \frac{1}{2\pi C_{eq} \left[\frac{r_{b'e} (r_{bb'} + R_s)}{(R_s + h_{ie})}\right]}$$

$\because \quad h_{ie} = r_{b'e} + r_{bb'}$

$$= \frac{-h_{fe} R_L}{2\pi C_{eq} r_{b'e} (r_{bb'} + R_s)}$$

$$= \frac{-g_m r_{b'e} R_L}{2\pi C_{eq} r_{b'e} (r_{bb'} + R_s)} \qquad \because h_{fe} = g_m r_{b'e}$$

$$= \frac{-g_m R_L}{2\pi C_{eq} (r_{bb'} + R_s)} \qquad \ldots (1)$$

This equation can be further simplified as follows.

$$|A_{vso} \times f_H| = \frac{g_m}{2\pi[C_e + C_C [1 + g_m R_L]]} \times \frac{R_L}{R_s + r_{bb'}}$$

$\because \quad C_{eq} = C_e + C_C (1 + g_m R_L)$

$$= \frac{g_m}{2\pi[C_e + C_C + g_m R_L]} \times \frac{R_L}{R_s + r_{bb'}} \qquad \because g_m R_L >> 1$$

$$= \frac{R_L}{R_s + r_{bb'}} \times \frac{2\pi f_T C_e}{2\pi[C_e + C_C (2\pi f_T C_e) R_L]}$$

$\because \quad g_m = 2\pi f_T C_e$

$$= \frac{R_L}{R_s + r_{bb'}} \times \frac{2\pi C_e f_T}{2\pi C_e [1 + 2\pi f_T C_C R_L]}$$

$$= \frac{R_L}{R_s + r_{bb'}} \times \frac{f_T}{1 + 2\pi f_T C_C R_L}$$

$\therefore \quad |A_{vso} \times f_H| = \frac{R_L}{R_s + r_{bb'}} \times \frac{f_T}{1 + 2\pi f_T C_C R_L} \qquad \ldots (2)$

4.8.2 Gain Bandwidth Product for Current

The gain bandwidth product for current gain is given as

$$|A_{is\,low} \times f_H| = |A_{iso} \times f_H| = \frac{-h_{fe} R_s}{R_s + h_{ie}} \times \frac{1}{2\pi R_{eq} C_{eq}}$$

By similar analysis with replacement of $-h_{fe} R_s$ instead of $-h_{fe} R_L$ we get,

$$|A_{iso} \times f_H| = \frac{g_m R_s}{2\pi C (R_s + r_{bb'})} = \frac{f_T}{1 + 2\pi f_T C_C R_L} \cdot \frac{R_s}{R_s + r_{bb'}} \quad \ldots (3)$$

The quantities f_H, A_{iso} and A_{vso} which characterize the transistor stage, depend on both R_L and R_s. The dependence between R_s and R_L with quantities f_H, A_{iso} and A_{vso} is shown in Fig. 4.18.

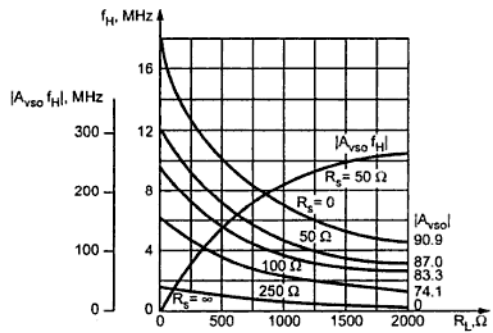


Fig. 4.18

Here f_H is plotted as a function of R_L upto R_L = 2000 Ω, for several values of R_s. The curve R_s = 0, corresponds to ideal voltage source drive. The voltage gain ranges from zero at R_L = 0 to 90.9 at R_L = 2000 Ω. The bottom curve with R_s = ∞ corresponds to ideal current source drive. Looking at the same curve we can say that voltage gain is zero for all R_L if R_s = ∞. For any R_L the bandwidth is highest for lowest R_s. The voltage gain bandwidth product increases with increasing R_L and decreases with increasing R_s. Therefore, we can say that the gain bandwidth product is not constant, but it depends on values of R_L and R_s.

$$\therefore \quad f_H = \frac{1}{2\pi[r_{b'e} \,||\, (r_{bb'} + R_s)]\,[C_e + C_C]}$$

$$= \frac{1}{2\times\pi\times[1\,K \,||\, (100 + 1\,K)]\,[100\,pF + 3\,pF]} = \mathbf{2.95\ MHz}$$

We have

$$A_{vs\,low} = \frac{-h_{fe}\,R_L}{R_s + h_{ie}}$$

$$= 0 \qquad \because R_L = 0$$

We have,

$$A_{is\,low} = \frac{-g_m\,r_{b'e}\,R_s}{R_s + r_{bb'} + r_{b'e}} = \frac{-50\times10^{-3}\times1\times10^3\times1\times10^3}{1\times10^3 + 100 + 1\times10^3} = \mathbf{-23.8}$$

ii) For R_L = 1 K

We have,

$$f_H = \frac{1}{2\pi R_{eq}\,C_{eq}}$$

where $R_{eq} = r_{b'e} \,||\, (r_{bb'} + R_s)$

And $C_{eq} = C_e + C_C\,[1 + g_m\,R_L]$

Typical values : $r_{b'e}$ = 1 K, $r_{bb'}$ = 100 Ω , C_e = 100 pF,

C_C = 3 pF, g_m = 50 mA/V

$$f_H = \frac{1}{2\pi\,[r_{b'e} \,||\, (r_{bb'} + R_s)]\,[C_e + C_C\,(1 + g_m\,R_L)]}$$

$$= \frac{1}{2\times\pi\times[1\,K \,||\, (100 + 1\,K)]\,[100\,pF + 3\,pF\,(1 + 50\times10^{-3}\times1\times10^3)]}$$

$$= \mathbf{1.2\ MHz}$$

We have,

$$A_{is\,low} = \frac{-g_m\,r_{b'e}\,R_s}{R_s + r_{bb'} + r_{b'e}}$$

$$= \frac{-50\times10^{-3}\times1\times10^3\times1\times10^3}{1\times10^3 + 100 + 1\times10^3}$$

$$= \mathbf{-23.8}$$

We know that, the low frequency gain of an emitter follower is close to unity : $K \approx 1$ and hence $1 - K = 0$. Looking at Fig. 4.20 with $1 - K = 0$, we have the input time constant $\tau_i \approx (R_s + r_{bb'}) C_C$ and the output time constant is proportional to C_L. Since we have assumed that the load is highly capacitive, $\tau_o >> \tau_i$ and hence we can determine the upper 3 dB frequency considering only output circuit.

With K = 1,

$$V_e = \frac{g_m V_{b'e}}{1/R_L + j\omega C_L} = \frac{g_m R_L (V_i' - V_e)}{1 + j\omega C_L R_L} \quad \ldots(3)$$

$$= \frac{g_m R_L V_i'}{1 + j\omega C_L R_L} - \frac{g_m R_L V_e}{1 + j\omega C_L R_L}$$

$$V_e \left(\frac{(1 + j\omega C_L R_L) + g_m R_L}{1 + j\omega C_L R_L} \right) = \frac{g_m R_L V_i'}{1 + j\omega C_L R_L}$$

$$\therefore \quad K = \frac{V_e}{V_i'} = \frac{g_m R_L}{1 + g_m R_L} \frac{1}{1 + j f / f_H} = \frac{K_o}{1 + jf / f_H} \quad \ldots(4)$$

where $K_o = \frac{g_m R_L}{1 + g_m R_L} \simeq 1$ $\quad \because g_m R_L >> 1 \ldots (5)$

and $$\boxed{f_H \equiv \frac{1 + g_m R_L}{2\pi C_L R_L} \approx \frac{g_m}{2\pi C_L} = \frac{f_T C_e}{C_L}} \quad \ldots (6)$$

where $f_T = \frac{g_m}{2\pi C_e}$ (from equation 13 of section 4.7.1.3)

Since $f_H = \frac{1}{2\pi \tau_o}$ and $\tau_o = C_L / g_m$, the condition

$\tau_o >> \tau_i$ requires

$$C_L >> g_m (R_s + r_{bb'}) C_C \quad \ldots(7)$$

If $R_s = 50\ \Omega$, $r_{bb'} = 100\ \Omega$, $C_C = 3$ pF and $g_m = 50$ mA/V

We have,

$C_L >> 50 \times 10^{-3} (50 + 100) \times 3 \times 10^{-12} = 23$ pF

Since the input impedance between terminals B′ and C is very large compared with $R_s + r_{bb'}$, the overall voltage gain $A_{vs} \equiv V_e / V_s = K$

Bettor Approximation for f_H

The circuit shown in the Fig. 4.19 (b) is redrawn as shown in the Fig. 4.21. The circuit connections are shown to make them suitable for the derivation of f_H.

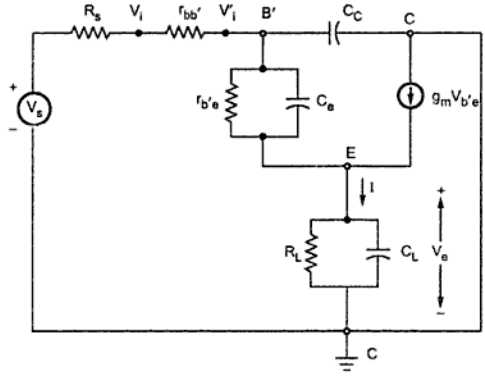


Fig. 4.21 Equivalent circuit of the emitter follower

Looking at Fig. 4.21 we have

$$V_e = IZ_L = \frac{1}{1/RL + j\omega C_L} = I\,\frac{R_L}{1+j\omega C_L R_L}$$

$$= [g_m(V'_i - V_e) + (V'_i - V_e)(g_{b'e} + j\omega C_e)]\frac{R_L}{1+j\omega C_L R_L}$$

$$\therefore \quad V_e = (V'_i - V_e) + (g_m + g_{b'e} + j\omega C_e)]\frac{R_L}{1+j\omega C_L R_L}$$

$$= (V'_i - V_e)[g + j\omega C_e]\frac{R_L}{1+j\omega C_L R_L} \qquad \text{where } g = g_m + g_{b'e}$$

$$\therefore \quad V_e\left[1 + (g+j\omega C_e)\frac{R_L}{1+j\omega C_L R_L}\right] = V'_i(g+j\omega C_e)\frac{R_L}{1+j\omega C_L R_L}$$

$$\therefore \quad K = \frac{V_e}{V'_i} = \frac{(g+j\omega C_e)\dfrac{R_L}{1+j\omega C_L R_L}}{1+(g+j\omega C_e)\dfrac{R_L}{1+j\omega C_L R_L}}$$

$$= \frac{(g+j\omega C_e)R_L}{1 + j\omega C_L R_L + (g+j\omega C_e)R_L}$$

Solution : From the equivalent circuit shown in Fig. 4.23 drawn from, hybrid-π model of transistor f_H is given by $\frac{1}{2\pi R_{eq} C_{eq}}$.

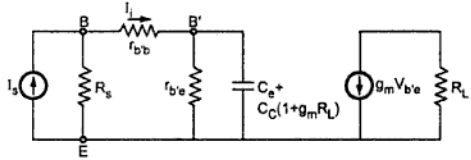


Fig. 4.23

where $R_{eq} = \frac{(R_s + r_{bb'})\, r_{b'e}}{R_s + r_{bb'} + r_{b'e}}$

and $C_{eq} = C_e + C_C\,[1 + g_m\, R_L]$

$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{100}{50\,mA\,/\,V} = 2\ K$

$r_{bb'} + r_{b'e} = 100\ \Omega + 2\ K = 2.1\ K$

$\therefore \quad f_H = \frac{1}{2\pi R_{eq} C_{eq}}$

$C_{eq} = C_e + C_C\,[1 + g_m\, R_L]$

$= C_e + C_C\,[1 + 50 \times 10^{-3} \times 600]$

$= C_e + 62\ pF$

$C_e = \frac{g_m}{2\pi f_T} = \frac{50\times10^{-3}}{2\pi(300\ MHz)}$

$= 26.5\ pF$

$\therefore \quad C_{eq} = 26.5\ pF + 62\ pF = 88.5\ pF$

$\therefore \quad R_{eq} = \frac{1}{2\pi f_H C_{eq}} = \frac{1}{(6.28)\times 4\ MHz \times 88.5\,pF}$

$= 449.59\ \Omega$

$\therefore \quad 449.59 = \frac{(R_s + 0.1\,K)\,(2\,K)}{R_s + 2.1\,K}$

$449.59\ R_s + 944139 = 2000\ R_s + 200000$

$$f_H = \frac{1}{2\pi R_{eq} C_{eq}} = 4 \text{ MHz}$$

$$R_{eq} = \frac{1}{2\pi f_H C_{eq}} = \frac{1}{2\pi \times 4\times10^6 \times 116.52\times10^{-12}}$$

$$= 341.53\ \Omega$$

$$R_{eq} = (R_s + r_{b'b}) \parallel r_{b'e}$$

$$\therefore \quad \frac{(R_s + r_{bb'})\, r_{b'e}}{R_s + r_{bb'} + r_{b'e}} = 341.5\ \Omega$$

$$\therefore \quad (R_s + 100)\frac{2\times10^3}{R_s + 100 + 2\times10^3} = 341.5$$

$$\therefore \quad 2\times10^3 R_s + 200\times10^3 = 341.5\, R_s + 717.15\times10^3$$

$$\therefore \quad R_s = 311.8\ \Omega$$

ii)
$$A_v = \frac{-h_{fe}\times R_L}{R_s + r_{bb'} + r_{b'e}}$$

$$= \frac{-100\times600}{311.8+100+2000}$$

$$= -24.88$$

Example 4.10 : *The hybrid-π parameters of the transistor used in the circuit of Fig. 4.24 are $g_m = 50$ mA/V, $r_{b'c} = 1$ kΩ, $r_{b'e} = 4$ MΩ, $r_{ce} = 80$ kΩ, $C_C = 3$ pF, $C_e = 100$ pF and $r_{bb'} = 100\ \Omega$. Find*

a) Upper 3 dB frequency of current gain $A_i = \frac{I_L}{I_i}$

b) The magnitude of voltage gain at $A_{vs} = \frac{V_o}{V_s}$ at frequency of part (a).

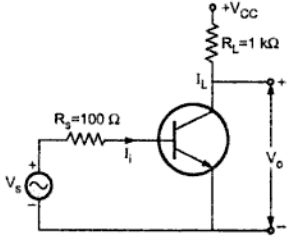


Fig. 4.24

$$R_{eq'} = r_{b'e} \parallel r_{bb'} + R_s = \frac{r_{b'e} \parallel r_{bb'} + R_s}{r_{b'e} + r_{bb'} + R_s}$$

$$\therefore \quad 181.8 = \frac{1000\,(100 + R_s)}{1000 + 100 + R_s}$$

$$= \frac{1 \times 10^5 + 1000\,R_s}{1100 + R_s}$$

$$\therefore \; 199980 + 181.8\,R_s = 1 \times 10^5 + 1000\,R_s$$

$$\therefore \quad R_s = 122.2\ \Omega$$

Example 4.12 : *For a single stage CE amplifier whose hybrid-π parameters are given below. What value of R_s will give 3 dB frequency $f_{H'}$ which is twice the value obtained with $R_s = \infty$ (ideal current source). Hybrid-π parameters : $g_m = 50$ mA/V, $r_{bb'} = 100\ \Omega$, $r_{b'e} = 1$ K, $C_C = 3$ pF, $C_e = 100$ pF.*

Solution :

$$f_H = \frac{1}{2\pi R_{eq}\, C_{eq}}$$

and $$f_{H'} = 2\, f_H$$

$$\therefore \quad \frac{1}{2\pi R_{eq'}\, C_{eq}} = \frac{2}{2\pi R_{eq}\, C_{eq}}$$

$$\therefore \quad R_{eq'} = \frac{R_{eq}}{2}$$

$$R_{eq} = r_{b'e} \parallel (r_{bb'} + R_s)$$

$$= r_{b'e} \parallel r_{bb'}$$

$$= r_{b'e} = 1000\ \Omega$$

$$\therefore \quad R_{eq'} = 500\ \Omega$$

$$\therefore \quad 500 = \frac{r_{b'e}\,(r_{bb'} + R_s)}{r_{b'e} + r_{bb'} + R_s}$$

$$= \frac{1000\,(100 + R_s)}{1000 + 100 + R_s}$$

$$\therefore \; 5.5 \times 10^5 + 500\,R_s = 1 \times 10^5 + 1000\,R_s$$

$$\therefore \quad R_s = 900\ \Omega$$

$$= \frac{g_m}{2\pi\,[C_e + C_C\, g_m\, R_L]} \times \frac{R_L}{R_s + r_{bb'}} \qquad \because g_m R_L >> 1$$

$$= \frac{R_L}{R_s + r_{bb'}} \times \frac{2\pi f_T\, C_e}{2\pi\,[C_e + C_C\,(2\pi f_T\, C_e)\, R_L]}$$

$\because \quad g_m = 2\pi f_T\, C_e,$

$$= \frac{R_L}{R_s + r_{bb'}} \times \frac{2\pi C_e\, f_T}{2\pi C_e\,[1 + 2\pi f_T\, C_C\, R_L]}$$

$$= \frac{R_L}{R_s + r_{bb'}} \times \frac{f_T}{1 + 2\pi f_T\, C_C\, R_L} \qquad \text{... proved}$$

Example 4.15 : *Using hybrid-π equivalent circuit show that short circuit current gain as a function of frequency for a common collector transistor is given by*

$$A_i = \frac{\left[\frac{1}{1-\alpha}\right]}{1 + j\left(\frac{f}{f_\beta}\right)}$$

Neglect r_{ce}, $r_{b'c}$, C_C

Solution : Hybrid-π model of CE configuration

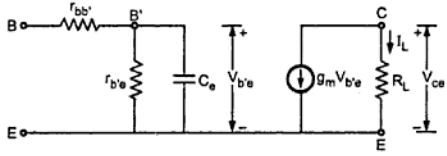


Fig. 4.25

Making collector common and $R_L = 0$ we get,

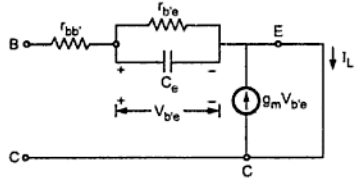


Fig. 4.26

Parallel combination of $r_{b'e}$ and C_e can be given as

$$Z = \frac{r_{b'e} \times \frac{1}{j\omega C_e}}{r_{b'e} + \frac{1}{j\omega C_e}} = \frac{r_{b'e}}{1 + j\omega r_{b'e} C_e}$$

Simplified equivalent circuit can be given as shown in the Fig. 4.27.

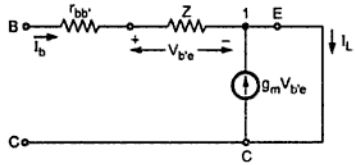


Fig. 4.27

Looking at Fig. 4.27 we have,

$$V_{b'e} = I_b Z = \frac{r_{b'e} I_b}{1 + j\omega r_{b'e} C_e}$$

Applying KCL at node 1 we get,

$$I_L = I_b + g_m V_{b'e}$$

Substituting value of $V_{b'e}$ we get,

$$I_L = I_b + \frac{g_m r_{b'e} I_b}{1 + j\omega r_{b'e} C_e} = I_b \left[1 + \frac{g_m r_{b'e}}{1 + j\omega r_{b'e} C_e}\right]$$

$$A_i = \frac{I_L}{I_b} = 1 + \frac{g_m r_{b'e}}{1 + j\omega r_{b'e} C_e} = 1 + \frac{h_{fe}}{1 + j\omega r_{b'e} C_e} = 1 + \frac{h_{fe}}{1 + j2\pi f r_{b'e} C_e}$$

We know that $\approx \frac{h_{fe}}{1 + j2\pi f r_{b'e} C_e}$

$$f_\beta = \frac{1}{2\pi r_{b'e}(C_e + C_C)}$$

Neglecting C_C we get,

$$f_\beta = \frac{1}{2\pi r_{b'e} C_e}$$

$$\therefore \quad \frac{1}{f_\beta} = 2\pi r_{b'e} C_e$$

$$\therefore \quad A_i = \frac{h_{fe}}{1+j\left(\frac{f}{f_\beta}\right)}$$

α_o is the current gain of CB at low frequency

$$\alpha_o = \frac{h_{fe}}{1+h_{fe}}$$

$$\therefore \quad 1-\alpha_o = 1-\frac{h_{fe}}{1+h_{fe}}$$

$$1-\alpha_o = \frac{1}{1+h_{fe}} \approx \frac{1}{h_{fe}}$$

$$\therefore \quad \frac{1}{1-\alpha_o} = h_{fe}$$

$$\therefore \quad A_i = \frac{\left[\frac{1}{1-\alpha_o}\right]}{1+j\left(\frac{f}{f_\beta}\right)}$$

Example 4.16 : *The amplifier shown in Fig. 4.28 uses a transistor with the following parameters.*

$g_m = 0.2\ A/V$, $r_{bb'} = 100$ ohm, $r_{b'e} = 1\ K$

$C_e = 200\ pF$, $C_C = 4\ pF$, $r_{ce} = 80\ K$

Assume coupling and bypass capacitors to be perfect short at mid and high frequencies. Draw hybrid-π equivalent circuit of the amplifier and calculate :

i) Mid frequency voltage gain V_o / V_s

ii) f_β iii) f_T

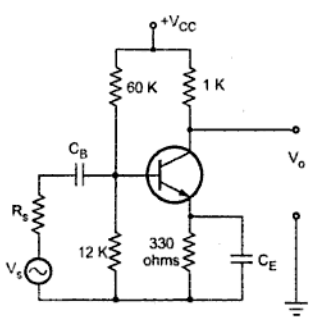


Fig. 4.28

Solution : Hybrid-π Equivalent

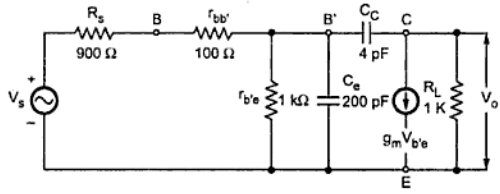


Fig. 4.29

i) Mid frequency voltage gain :

$$\frac{V_o}{V_s} = \frac{-h_{fe} R_L}{R_s + h_{ie}}$$

$$h_{ie} = r_{bb'} + r_{b'e}$$

$$= 100 + 1000 = 1100\ \Omega = 1.1\ K$$

$$h_{fe} = g_m \times r_{b'e}$$

$$= 0.2\ A/V \times 1\ K = 200$$

$$\therefore \quad \frac{V_o}{V_s} = \frac{-200 \times 1}{0.9 + 1.1} = \frac{-200}{2.0}$$

$$= -100$$

ii) f_β

$$f_\beta = \frac{1}{2\pi r_{b'e}(C_e + C_C)}$$

$$= \frac{1}{2\pi \times 1\ K \times (200\ pF + 4\ pF)}$$

$$= 780.17\ kHz$$

$$f_\beta \simeq 780\ kHz$$

iii)

$$f_T = h_{fe} \cdot f_\beta$$

$$= 200 \times 780$$

$$= 156\ MHz$$

Example 4.17 : *A single stage CE amplifier is measured to have a voltage gain bandwidth f_H of 5 MHz with R_L = 500 Ω. Assume h_{fe} = 100, g_m = 100 mA/V, $r_{bb'}$ = 100 Ω, C_C = 1 pF, and f_T = 400 MHz.*

i) Find the value of source resistance that will give the required bandwidth.

ii) With the value of R_s found in (i), find the midband voltage gain V_o/V_s.

Solution : i) We know that,

$$f_H = \frac{1}{2\pi R_{eq} C_{eq}}$$

where $$R_{eq} = \frac{(R_s + r_{bb'})\, r_{b'e}}{R_s + r_{bb'} + r_{b'e}}$$

and $$C_{eq} = C_e + C_C\,[1 + g_m R_L]$$

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{100}{100 \text{ mA / V}}$$

$$= 1 \text{ K}$$

$$C_{eq} = C_e + C_C\,[1 + g_m R_L] = C_e + C_C\,[1 + 100 \times 10^{-3} \times 500]$$

$$= C_e + 51 \text{ pF}$$

$$C_e = \frac{g_m}{2\pi f_T} = \frac{100 \times 10^{-3}}{2\pi(400 \times 10^6)}$$

$$= 39.79 \text{ pF}$$

$\therefore$ $$C_{eq} = 39.79 + 51 = 90.79 \text{ pF}$$

$$R_{eq} = \frac{1}{2\pi f_{11} C_{eq}} = \frac{1}{2\pi \times 5 \times 10^6 \times 90.79 \times 10^{-12}}$$

$$= 350.6\ \Omega$$

$\therefore$ $$350.6 = \frac{(R_s + 100)(1000)}{R_s + 1100}$$

$\therefore$ $$350.6\, R_s + 385.66 \times 10^3 = 1000\, R_s + 100000$$

$\therefore$ $$649.4\, R_s = 285.66 \times 10^3$$

$\therefore$ $$R_s = 439.88\ \Omega$$

ii) The mid band voltage gain V_o/V_s is given as

$$\frac{V_o}{V_s} = \frac{-h_{fe} R_L}{R_s + h_{ie}}$$

where $h_{ie} = r_{bb'} + r_{bb'} = 100 + 1000$

$= 1.1 \text{ K}$

$\therefore \quad \frac{V_o}{V_s} = \frac{-100 \times 500}{439.88 + 1100} = -32.47$

Example 4.18 : *For the circuit shown in Fig. 4.30, determine* $A_{vs} = \frac{V_o}{V_s}$ *as a function of frequency. The transistor Q has the following parameters :*

$r_{bb'} = 50\ \Omega$, $r_{ce} = \infty$, $g_m = 1\ mA/V$

$r_{b'e} = 2600\ \Omega$, $C_e = 200\ pF$

$r_{b'c} = \infty$, $C_C = 3\ pF$

Assume that the output time-constant is negligible as compared to the input time constant.

All coupling and bypass capacitors may be treated as short for frequencies of operation of the circuit.

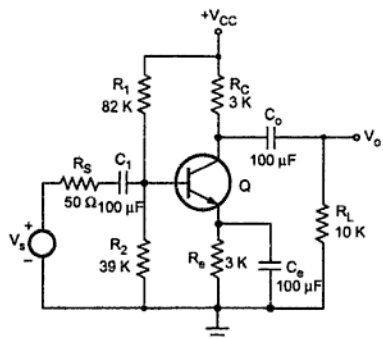


Fig. 4.30

Solution : When the output time constant is negligible as compared to the input time constant

$$A_{vs} = \frac{V_o}{V_s} = \frac{-g_m R'_L G'_s}{G'_s + g_{b'e} + sC}$$

where $G'_s = \frac{1}{(R_s \parallel R_b) + r_{bb'}} = \frac{1}{50 \| (82\text{ K} \| 59\text{ K}) + 50}$

$= \frac{1}{99.9} = 10.01 \times 10^{-3}$

$$h_{oe} = g_{ce} + (1 + h_{fe})\, g_{b'e} = \frac{1}{r_{ce}} + \frac{(1+h_{fe})}{r_{b'c}}$$

$$= \frac{1}{80\ K} + \frac{(1+77.238)}{2M\Omega}$$

$$= 51.619 \times 10^{-6}$$

Example 4.20 : *Calculate the voltage gain* $\frac{V_o}{V_s}$ *for the circuit shown in Fig. 4.31.*

Transistor parameters are given as under :

$I_c = 1\ mA$, $r_{bb'} = 100\ \Omega$, $r_{ce} = 80\ k\Omega$

$g_m = 50\ mA/V$, $r_{b'e} = 1\ k\Omega$, $C_C = 3\ pF$

$r_{b'c} = 4\ M\Omega$, $C_e = 100\ pF$

You may use the following conversion formulae :

$$h_{ie} = r_{bb'} + r_{b'e}, \quad h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}}$$

$$h_{fe} = g_m \cdot r_{b'e}, \quad h_{oe} = \frac{1}{r_{ce}} + \frac{1}{r_{b'c}} + g_m\, h_{re}$$

Make suitable approximations to simplify your circuit.

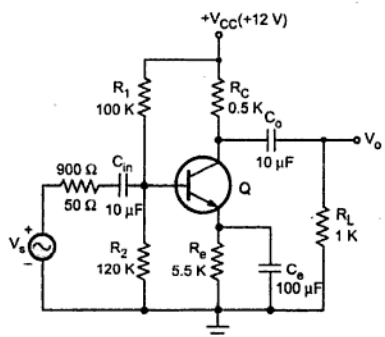


Fig. 4.31

Solution : Assume that the output time-constant is negligible as compared to the input time consedtant. When this is the case

$$A_{vs} = \frac{V_o}{V_s} = \frac{-g_m R'_L G'_s}{G'_s + g_{b'e} + sC}$$

where $$G_s' = \frac{1}{(R_s \parallel R_b) + r_{bb'}} = \frac{1}{50 \parallel (100\,K \parallel 120\,K) + 100}$$

$$= 6.66 \times 10^{-3}$$

$$g_{b'e} = \frac{1}{r_{b'e}} = \frac{1}{1\,K} = 1 \times 10^{-3}$$

$$R_L' = R_L \parallel R_C = 1\,K \parallel 0.5\,K$$

$$= 333.33\,\Omega$$

$$sC = \text{admittance of C}$$

where $$C = C_e + C_C\,(1 + g_m R_L')$$

$$= 100\,pF + 3\,pF\,(1 + 50 \times 10^{-3} \times 333.33)$$

$$= 153\,pF$$

At 10 kHz,

$$sC = 2\pi fC = 2\pi \times 10 \times 10^3 \times 153\,pF$$

$$= 9.613 \times 10^{-6}$$

$\therefore$ At 10 kHz signal frequency

$$A_{vs} = \frac{V_o}{V_s}$$

$$= \frac{-50 \times 10^{-3} \times 333.33 \times 6.66 \times 10^{-3}}{6.66 \times 10^{-3} + 1 \times 10^{-3} + 9.613 \times 10^{-6}}$$

$$= -14.47$$

Example 4.21 : *Given the following transistor measurements made at I_c = 5 mA, V_{CE} = 10 V and at room temperature h_{fe} = 100, h_{ie} = 600 Ω, A_{ie} = 10 at 10 MHz, C_e = 3 pF.*

Find f_β, f_T, $C_{e'}$, $r_{b'e}$ and $r_{bb'}$. **(R.U. : 1995, 2005)**

Solution : From equation (5) of section 4.7.1 we have,

$$|A_i| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{f_\beta}\right)^2}}$$

5 Tuned Amplifier

5.1 Band Pass Amplifiers

To amplify the selective range of frequencies, the resistive load, R_C is replaced by a tuned circuit. The tuned circuit is capable of amplifying a signal over a narrow band of frequencies centered at f_r. The amplifiers with such a tuned circuit as a load are known as **tuned amplifier**. Since tuned amplifiers amplify narrow band of frequencies they are also known as **narrow band amplifiers**. In the tuned RF amplifiers the center frequency may range from 1 to many megahertz and side frequencies extend to 5 or 10 kHz for amplitude modulated voice or music and to several hundred kilohertz for other amplifications.

The tuned circuits resonate at a particular frequency. The response of tuned amplifiers is maximum at resonant frequency and it falls sharply for frequencies below and above the resonant frequency, as shown in the Fig. 5.1.

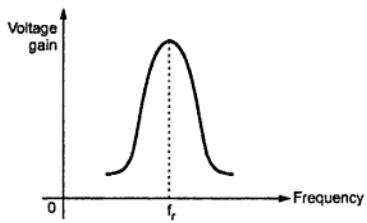


Fig. 5.1

At resonance, inductive and capacitive effects of tuned circuit cancel each other. As a result, circuit is like resistive and cos $\phi = 1$ i.e. voltage and current are in phase. For frequencies above resonance circuit is like capacitive and for frequencies below resonance it is like inductive. Since tuned circuit is purely resistive at resonance it can be used as a load for amplifier.

We need tuned amplifiers to select or to amplify particular band of frequencies in a radio receiver or TV receiver. All frequencies in the desired band would be amplified

equally, and all frequencies outside the desired band would produce zero response. A measure of relative selectivity is sometimes defined as the ratio of the frequency width of the response curve at 60 dB down from the center frequency response to the bandwidth at which a signal only 6 dB down.

5.2 Parallel Resonant Circuit

The Fig. 5.2 shows the tuned parallel LC circuit which resonates at a particular frequency.

The total admittance of the parallel tuned circuit is given by

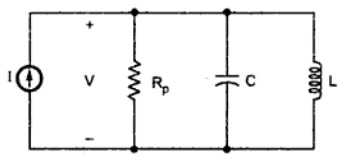


Fig. 5.2 Parallel resonant LC circuit

$$Y_T = \frac{1}{R_p} + \frac{1}{1/j\omega C} + \frac{1}{j\omega L}$$

$$= \frac{1}{R_p} + j\left(\omega C - \frac{1}{\omega L}\right) \quad \ldots (1)$$

At resonance imaginary part is zero, thus equating it to zero we get,

$$\omega_0 C = \frac{1}{\omega_0 L} \qquad \therefore \omega_0^2 L C = 1 \quad \ldots (2)$$

$$\therefore \quad \boxed{f_0 = \frac{1}{2\pi\sqrt{LC}}} \quad \ldots (3)$$

Q factor

Quality factor (Q) is important characteristics of an inductor. The Q is the ratio of reactance to resistance and therefore it is unit less. It is the measure of how 'pure' or 'real' an inductor is (i.e. the inductor contains only reactance). The higher the Q of an inductor the fewer losses there are in the inductor. The Q factor also can be defined as the measure of efficiency with which inductor can store the energy.

$$Q = 2\pi \frac{\text{Maximum energy stored per cycle}}{\text{Energy dissipated per cycle}} \quad \ldots (4)$$

The voltage V is common to the three circuit elements, and we can write the maximum energy of the circuit in terms of the capacitance as $CV_m^2/2$. The energy loss per cycle is $(V_m^2/2R_p) / f$. Then Q is

$$Q = \frac{2\pi V_m^2 C/2}{V_m^2/2R_p f} = \omega_0 CR_p = \frac{R_p}{\omega_0 L} = R_p\sqrt{\frac{C}{L}} \quad \ldots (5)$$

Once the resonant condition is determined by $\omega_0^2 L C = 1$, the value of Q of a resonant circuit is determined by R_p, or by the ratio of C to L.

At resonance, reactive term is equal to zero, therefore,

$$Y_T = \frac{1}{R_p}$$

$\therefore$ Impedance at resonance, $Z_0 = R_p$ ... (6)

Using equation (6) and (5) we can write

$$Z_0 = Q\omega_0 L = \frac{Q}{\omega_0 C} \quad \ldots (7)$$

The impedance of the resonant circuit is required in determining circuit gain. The gain of the circuit shown in Fig. 5.3 is

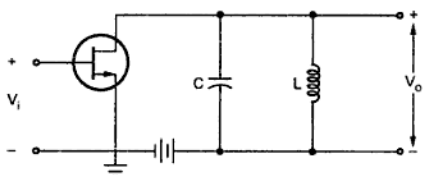


Fig. 5.3 LC resonant circuit

$$A_v = -g_m R_L = -g_m Q\omega_0 L \quad \ldots (8)$$

5.3 Series Resonant Circuit

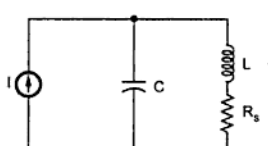


Fig. 5.4 (a) R in series

The Fig. 5.4 (a) shows the series resonant circuit. Here, the loss element R_s is in series with L. The admittance of the R_s L series branch is

$$Y = \frac{1}{R_s + j\omega L} = \frac{R_s - j\omega L}{R_s^2 + \omega^2 L^2} \quad \ldots (1)$$

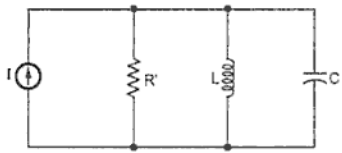


Fig. 5.4 (b) R in parallel

Usually at high Q conditions, $\omega^2 L^2 >> R_s^2$. Therefore, we can drop term R_s^2 in the denominator to get

$$Y = \frac{R_s}{\omega^2 L^2} + \frac{1}{j\omega L} = \frac{1}{R'} + \frac{1}{j\omega L} \quad \ldots (2)$$

This equation gives us the parallel arrangement as shown in Fig. 5.4 (b). Where R' is given by

$$R' = \frac{\omega^2 L^2}{R_s} \quad \ldots (3)$$

$$\therefore \quad R_s = \frac{\omega^2 L^2}{R'} \quad \ldots (4)$$

The equations (3) and (4) represent transformations for passing from the series form of circuit to the parallel form, or vice versa. The inductance L does not change in the transformations but a small series R_s transforms to a large R' in parallel with L.

In the previous section we have seen that for parallel circuit Q is

$$Q = \omega_0 C R_p$$

Here, R_p is represented by R'

$$\therefore \quad Q = \omega_0 C R' = \omega_0 C \frac{\omega_0^2 L^2}{R_s} \quad \ldots (5)$$

Since $\omega_0^2 LC = 1$ We have

$$Q = \frac{\omega_0 L}{R_s} \quad \ldots (6)$$

Example 5.1 : *An inductor of 250 μH has Q = 300 at 1 MHz. Determine R_s and R_p of inductor.*

Solution :

$$R_p = \omega_0 L Q = 2\pi \times 1\,\text{MHz} \times 250 \times 10^{-6} \times 300$$

$$= \mathbf{471.24\ k\Omega}$$

$$R_s = \frac{\omega_0 L}{Q} = \frac{2\times\pi\times 10^6 \times 250 \times 10^{-6}}{300} = \mathbf{5.235\ \Omega}$$

5.4 Bandwidth of Parallel Resonant Circuit

Let us define a frequency variation parameter as δ. It indicates the frequency deviation from resonance frequency and it defined as.

$$\delta = \frac{\omega - \omega_0}{\omega_0} = \frac{f - f_0}{f_0} \quad \ldots (1)$$

At resonance $\delta = 0$ and the voltage of parallel resonant circuit is

$$\boxed{V_0 = IZ_0 = IR_p} \quad \ldots (2)$$

The impedance expression for parallel resonant circuit is given by,

$$\boxed{Z = \frac{R_p}{1 + j\,2Q\,\delta}} \quad \ldots (3)$$

At a half-power bandwidth limit the real and reactive terms of the circuit impedance are equal and we get,

$$\boxed{1 = 2\,Q\,\delta} \quad \ldots (4)$$

At a half power we also have,

$$V_0 = \frac{V_0}{\sqrt{2}} = \frac{IR_p}{\sqrt{1+1}}$$

At the below resonance band limit we have $f_1 < f_0$ and equation (1) gives,

$$\delta_1 = \frac{f_0 - f_1}{f_0} = 1 - f_1/f_0 \quad \ldots(5)$$

Substituting value of δ_1 from equation (5) in equation (4) we get,

$$1 = 2Q\left(1 - \frac{f_1}{f_0}\right) \quad \ldots(6)$$

At above resonance band limit we have,

$f_2 > f_0$ and equation (1) gives,

$$\delta_2 = \frac{f_2 - f_0}{f_0} = f_2/f_0 - 1 \quad \ldots(7)$$

Substituting value of δ_2 from equation (6) in equation (4) we get,

$$1 = 2Q\left(\frac{f_2}{f_0} - 1\right) \quad \ldots(8)$$

Adding the relations we get from equations (6) and (8), we have,

$$2 = 2\,Q\,\frac{f_2 - f_1}{f_0}$$

$$\therefore \qquad f_2 - f_1 = \frac{f_0}{Q}$$

The bandwidth for the resonant circuit is $f_2 - f_1$ and hence it is given by

$$BW = f_2 - f_1 = \frac{f_0}{Q} \qquad ...(9)$$

The equation (9) shows that the bandwidth of the parallel resonant circuit is inversely proportional to the circuit Q.

The Fig. 5.5 shows the impedance and phase angle for parallel resonant circuit. It shows that the phase angle of the circuit impedance changes in an almost linear manner from + 45 ° to – 45 °. The average rate of change of phase angle is,

$$\frac{d\theta}{d\omega} = -\frac{90°}{BW} = -90° \frac{Q}{\omega_0} \qquad ...(10)$$

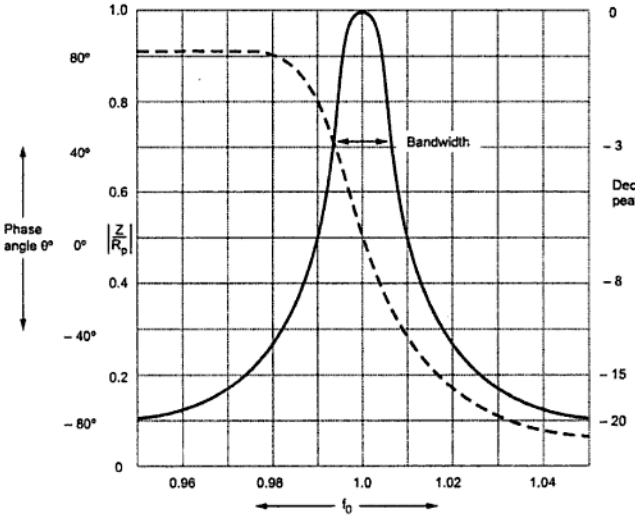


Fig. 5.5 Impedance and phase angle for parallel resonant circuit for Q = 100

The equation (10) shows that the higher the value of Q greater is the rate of phase angle change. This is the important advantage of a high Q circuit in constant frequency oscillator circuits.

The impedance of a parallel-resonant circuit shown in Fig. 5.2 is given by

$$Z = \frac{1}{Y} = \frac{1}{\frac{1}{R_p} + j\,[\omega C - (1/\omega L)]}$$

$$= \frac{R_p}{1 + j\omega C R_p [1 - (1/\omega^2 LC)]}$$

$$= \frac{R_p}{1 + jQ\,[1 - (\omega_0/\omega)^2]} \qquad \because \ \omega_0^2 = \frac{1}{LC} \text{ and } \omega C R_p = Q \qquad ...(11)$$

Substituting the value of Q from equation (5) of section 5.2 in equation (11) we can write the equality of real and reactive terms at f_2 as

$$1 = R_p \sqrt{\frac{C}{L}} \left(\omega_2 \sqrt{LC} - \frac{1}{\omega_2 \sqrt{LC}} \right)$$

$$= Q \left(\frac{f_2}{f_0} - \frac{f_0}{f_2} \right) \qquad ...(12)$$

Similarly, at f_1 with $f_0 | f_1 > 1$ we have,

$$1 = Q \left(\frac{f_0}{f_1} - \frac{f_1}{f_0} \right) \qquad ...(13)$$

Equating equations (12) and eliminating Q we have

$$\left(\frac{f_2}{f_0} - \frac{f_0}{f_2} \right) = \left(\frac{f_0}{f_1} - \frac{f_1}{f_0} \right)$$

$$\therefore \quad \frac{f_2^2 - f_0^2}{f_0 f_2} = \frac{f_0^2 - f_1^2}{f_1 f_0}$$

$$\therefore \quad \frac{f_2^2 - f_0^2}{f_2} = \frac{f_0^2 - f_1^2}{f_1}$$

$$\therefore \quad f_1 f_2^2 - f_0^2 f_1 = f_0^2 f_2 - f_1^2 f_2$$

$$\therefore \quad f_0^2 (f_1 - f_2) = f_1 f_2 (f_1 - f_2)$$

$$\therefore \quad f_0 = \sqrt{f_1 f_2} \qquad ...(14)$$

The equation (14) gives the exact result. However, we can calculate f_0 approximately by expression :

$$f_0 = \frac{f_1 + f_2}{2} \qquad ...(15)$$

5.5 Analysis of Single Tuned Amplifier

A common emitter amplifier can be converted into a single tuned amplifier by including a parallel tuned circuit as shown in Fig. 5.6. The biasing components are not shown for simplicity.

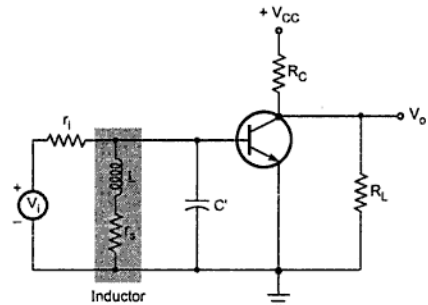


Fig. 5.6 Single tuned amplifier

Before going to study the analysis of this amplifier we see the several practical assumptions to simplify the analysis.

Assumptions :

1. $R_L << R_C$
2. $r_{bb'} = 0$

With these assumptions, the simplified equivalent circuit for a single tuned amplifier is as shown in Fig. 5.7.

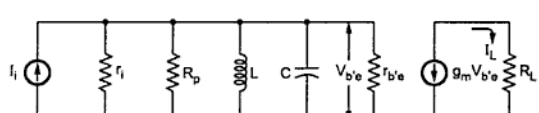


Fig. 5.7 Equivalent circuit of single tuned amplifier

where $C_{eq} = C' + C_{b'e} + (1 + g_m R_L) C_{b'c}$

C' : External capacitance used to tune the circuit

$(1 + g_m R_L) C_{b'c}$: The Miller capacitance

r_s : Represents the losses in coil

where $\omega_0^2 = \frac{1}{LC}$

We define the Q of the tuned circuit at the resonant frequency ω_0 to be

$$Q_i = \frac{R}{\omega_0 L} = \omega_0 RC \quad ...(5)$$

$$\therefore \quad \boxed{A_v = \frac{-g_m R}{1 + jQ_i(\omega/\omega_0 - \omega_0/\omega)}}$$

At $\omega = \omega_0$, gain is maximum and it is given as

$$\therefore \quad \boxed{A_{v\,(max)} = -g_m R} \quad ...(6)$$

The Fig. 5.9 shows the gain versus frequency plot for single tuned amplifier. It shows the variation of the magnitude of the gain as a function of frequency.

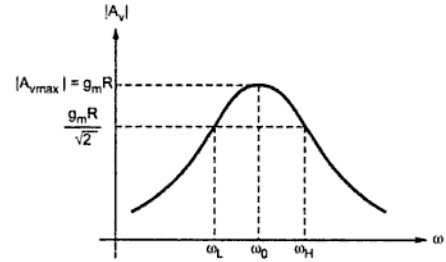


Fig. 5.9 Gain versus frequency for single-tuned amplifier

At 3 dB frequency,

$$|A_v| = \frac{g_m R}{\sqrt{2}} \quad ...(7)$$

∴ At 3 dB frequency

$$1 + jQ(\omega/\omega_0 - \omega_0/\omega) = \sqrt{2}$$

$$\therefore \quad 1 + Q^2\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)^2 = 2 \quad ...(8)$$

This equation is quadratic in ω^2 and has two positive solutions, ω_H and ω_L. After solving equation (8) we get 3 dB bandwidth as given below.

$$BW = f_H - f_L = \frac{\omega_0}{2\pi Q} = \frac{f_0}{Q} \quad \frac{1}{2\pi RC} \qquad \ldots(9)$$

$$\therefore \quad \boxed{BW = \frac{1}{2\pi RC}}$$

Example 5.2 : *Design a single tuned amplifier for following specifications :*

1. *Center frequency = 500 kHz*
2. *Bandwidth = 10 kHz*

Assume transistor parameters : $g_m = 0.04$ *S,* $h_{fe} = 100$, $C_{b'e} = 1000$ *pF and* $C_{b'c} = 100$ *pF. The bias network and the input resistance are adjusted so that* $r_i = 4$ kΩ *and* $R_L = 510\ \Omega$.

Solution : From equation (9) we have

$$BW = \frac{1}{2\pi RC}$$

$$\therefore \quad RC = \frac{1}{2\pi BW} = \frac{1}{2\pi \times 10 \times 10^3}$$

$$= 15.912 \times 10^{-6}$$

From equation (3) we have

$$R = r_i \parallel R_p \parallel r_{b'e}$$

where $r_i = 4\ k\Omega$

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{100}{0.04} = 2500\ \Omega$$

$$R_p = Q_c\, \omega_0 L = \frac{Q_c}{\omega_0 C}$$

$$\therefore \quad R = 4 \times 10^3 \parallel 2500 \parallel \frac{Q_c}{\omega_0 C}$$

$$C = \frac{1}{2\pi \times 10 \times 10^3 \times R}$$

$$\therefore \quad C = \frac{1}{2\pi \times 10 \times 10^3 \times \left[4 \times 10^3 \parallel 2500 \parallel \frac{Q_c}{2\pi \times 500 \times 10^3 \times C}\right]}$$

The typical range for Q_c is 10 to 150. However, we have to assume Q such that value of C_P should be positive. Let us assume Q = 100.

$$\therefore \quad C = \frac{1}{2\pi\times10\times10^{3}\left[1538.5 \,||\, \frac{1}{2\pi\times5000\times C}\right]}$$

$$= \frac{1}{2\pi\times10\times10^{3}\left[\frac{1}{\frac{1}{1538.5}+2\pi\times5000\times C}\right]}$$

Solving for C we get

$$C = 0.02\ \mu F$$

We have

$$C = C' + C_{b'e} + (1 + g_m R_L)\, C_{b'c}$$

$$\therefore \quad C' = C - [C_{b'e} + (1 + g_m R_L)\, C_{b'c}]$$

$$= 0.02 \times 10^{-6} - [1000 \times 10^{-12} + (1 + 0.04 \times 510) \times 100 \times 10^{-12}]$$

$$\therefore \quad C' = \mathbf{0.01686\ \mu F}$$

We have,

$$\omega_0^2 = \frac{1}{LC}$$

$$\therefore \quad L = \frac{1}{\omega_0^2 C} = \frac{1}{(2\pi\times500\times10^{3})^2\times0.02\times10^{-6}}$$

$$= \mathbf{5\ \mu H}$$

From equation (2) we have,

$$R_p = \omega L\, Q_c = 2\pi \times 500 \times 10^3 \times 5 \times 10^{-6} \times 100$$

$$= \mathbf{1570\ \Omega}$$

$$\therefore \quad R = r_i \,||\, R_p \,||\, r_{b'e} = 4 \times 10^3 \,||\, 1570 \,||\, 2500$$

$$= \mathbf{777\ \Omega}$$

We have mid frequency gain as

$$A_{v\,max} = -\, g_m R = (-\,0.04)\,(777) = \mathbf{-\,31}$$

5.6 Primary Tuned Amplifier with BJT

An inductively coupled circuit as shown in the Fig. 5.10 is frequently employed as a coupling element between successive amplifier stages at the higher frequencies. Such circuits are mainly used to obtain impedance matching for maximum power transfer between successive amplifier stages.

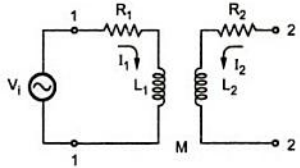


Fig. 5.10 Inductive coupled circuit

Here, M is the mutual inductance and it determines a coefficient of coupling K. It is given by,

$$K = \frac{M}{\sqrt{L_1 L_2}}$$

The Fig. 5.10 shows the inductive coupled parallel resonant circuit with BJT used as an amplifier. The component R_{11}, C_1 and L_1 in collector circuit of first stage forms the resonant circuit. At $\omega_0^2 L_1 C_1 = 0$, the circuit impedance is resistive at 1, 1 and by selection of an optimum value of mutual reactance, ωM, we can then match the load R_{22} to the first-stage.

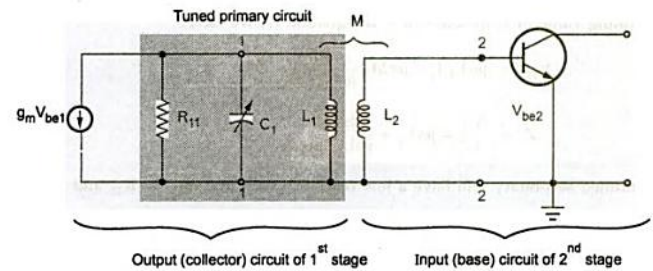


Fig. 5.10 (a) Inductive coupled parallel resonant circuit

The Fig. 5.10(b) shows the equivalent circuit of the inductive coupled parallel resonant circuit shown in the Fig. 5.10(a). Here, the inductive coupled circuit is replaced by its equivalent T network and the current source is replaced by voltage source.

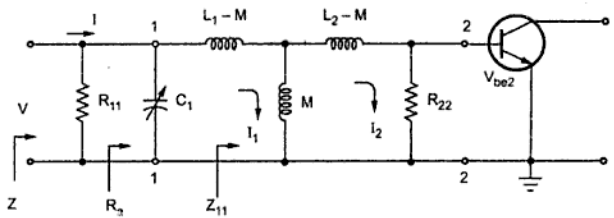


Fig. 5.10(b) Equivalent circuit

Looking at Fig. 5.10(b), we have

$$V_{11} = j\omega L_1 I_1 - j\omega M I_1 + j\omega M (I_1 - I_2)$$

$$= j\omega L_1 I_1 - j\omega M I_2 \quad \ldots(1)$$

$$0 = j\omega M (I_1 - I_2) - j\omega L_2 I_2 + j\omega M I_2 - R_{22} I_2$$

$$= j\omega M I_1 - (j\omega L_2 + R_{22}) I_2 \quad \ldots(2)$$

$$\therefore \quad I_2 = \left(\frac{j\omega M}{j\omega L_2 + R_{22}}\right) I_1 \quad \ldots(3)$$

we have,

$$Z_{11} = \frac{V_{11}}{I_1}$$

Substituting value of I_2 in terms of I_1 in equation (1) we have,

$$V_{11} = j\omega L_1 I_1 - j\omega M \left(\frac{j\omega M}{j\omega L_2 + R_{22}}\right) I_1$$

$$\therefore \quad Z = \frac{V_{11}}{I_1} = j\omega L_1 + \frac{\omega^2 M^2}{j\omega L_2 + R_{22}} \quad \ldots(4)$$

The untuned secondary will have a low reactance such that $\omega L_2 << R_{22}$ and therefore we have,

$$Z_{11} = j\omega L_1 + \frac{\omega^2 M^2}{R_{22}} \quad \ldots(5)$$

The equation (5) represents series circuit of L_1 and R_s where $R_s = \frac{\omega^2 M^2}{R_{22}}$. This is illustrated in Fig. 5.10(c).

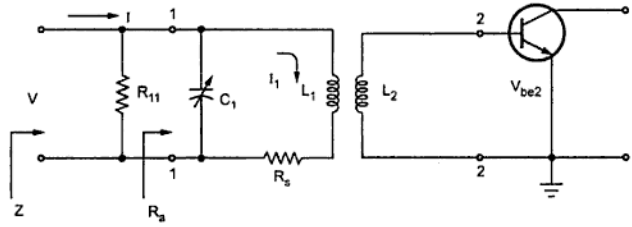


Fig. 5.10(c)

From equation (3) of section 5.3, we can find the equivalent parallel resistance at 1, 1 as

$$R_a = \frac{\omega^2 L_1^2}{R_s} = \frac{\omega^2 L_1^2}{\omega^2 M^2 / R_{22}} = \frac{L_1^2}{M^2 / R_{22}} = \frac{R_{22} L_1^2}{M^2} \qquad ...(6)$$

We have,

$$Z = R_a \parallel R_{11}$$

$$= \frac{R_a R_{11}}{R_a + R_{11}} = \frac{\frac{R_{22} L_1^2}{M^2} R_{11}}{\frac{R_{22} L_1^2}{M^2} + R_{11}}$$

$\therefore$ $$Z = R_p = \frac{R_{11}}{\left(1 + \frac{R_{11} M^2}{R_{22} L_1^2}\right)}$$

Looking at Fig. 5.10(c) the voltage V is

$$V = IZ = (j\omega L_1 + R_s) I_1$$

$$= j\omega L_1 I_1 \qquad \because \omega L_1 >> R_s$$

$$V_{be2} = R_{22} I_2$$

of the coupled circuit is tuned to resonance, as shown in the Fig. 5.11(a). The Fig. 5.11(b) shows the equivalent circuit for Fig. 5.11(a).

Let us derive the optimum value for M. Looking at Fig. 5.11 (b) we have,

$$V_{11} = j\omega L_1 I_1 - j\omega M I_1 + j\omega M (I_1 - I_2)$$

$$= j\omega L_1 I_1 - j\omega M I_2 \quad \ldots(1)$$

$$0 = j\omega M (I_2 - I_1) + j\omega L_2 I_2 - j\omega M I_2 + R_2 I_2 - \frac{j}{\omega C_2}$$

$$= -j\omega M I_1 + j\omega L_2 I_2 + R_2 I_2 - \frac{j}{\omega C_2}$$

$$= -j\omega M I_1 + \left[j\left(\omega L_2 - \frac{1}{\omega C_2}\right) + R_2 \right] I_2$$

$$\therefore \quad I_2 = \frac{j\omega M I_1}{j\left(\omega L_2 - \frac{1}{\omega C_2}\right) + R_2}$$

At resonance in the secondary, $\omega_0 L_2 = \frac{1}{\omega_0 C_2}$ and we have,

$$I_2 = \frac{j\omega_0 M I_1}{R_2}$$

We have,

$$Z_{11} = \frac{V_{11}}{I_1}$$

Substituting value of I_2 in terms of I_1 in equation (1) we have,

$$V_{11} = j\omega L_1 I_1 - j\omega M \left(\frac{j\omega M I_1}{R_2} \right)$$

$$\therefore \quad Z_{11} = \frac{V_{11}}{I_1} = j\omega L_1 + \frac{\omega_0^2 M^2}{R_2}$$

Looking at Fig. 5.11(b) we have,

$$I_1 = \frac{I \cdot r_d}{r_d + Z_{11}}$$

$$= \frac{I \ r_d}{r_d + j\omega L_1 + \frac{\omega_0^2 M^2}{R_2}}$$

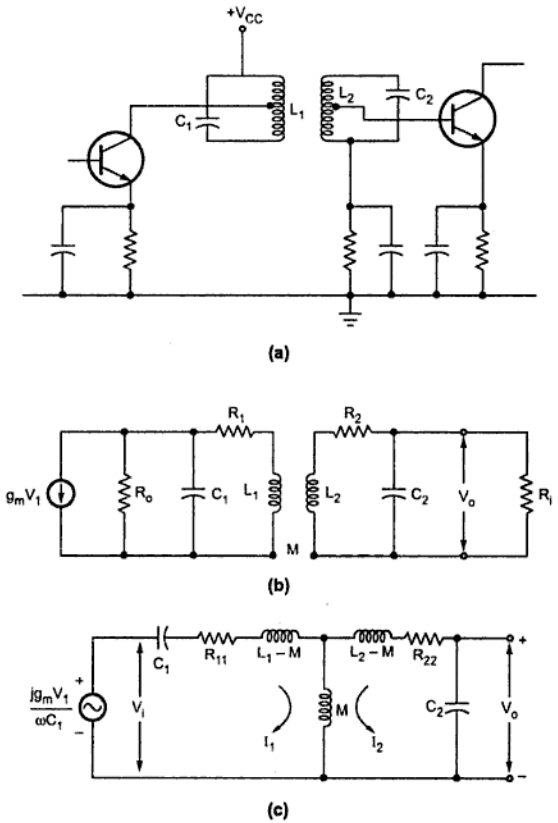


Fig. 5.13 Equivalent circuits for double tuned amplifier

The Fig. 5.13 (c) shows the simplified equivalent circuit for the Fig. 5.13 (b). In simplified equivalent circuit the series and parallel resistances are combined into series elements. Referring equation (9) we have

$$R_p = \frac{\omega^2 L^2}{R} \text{ i.e. } R = \frac{\omega^2 L^2}{R_p}$$

where R represents series resistance and R_p represents parallel resistance.

Therefore we can write,

$$R_{11} = \frac{\omega_0^2 L_1^2}{R_0} + R_1$$

$$R_{12} = \frac{\omega_0^2 L_2^2}{R_i} + R_2$$

In the simplified circuit the current source is replaced by voltage source, which is now in series with C_1. It also shows the effect of mutual inductance on primary and secondary sides.

We know that, $Q = \frac{\omega_r L}{R}$

Therefore, the Q factors of the individual tank circuits are

$$Q_1 = \frac{\omega_r L_1}{R_{11}} \text{ and } Q_2 = \frac{\omega_r L_2}{R_{22}} \quad \ldots(1)$$

Usually, the Q factors for both circuits are kept same. Therefore, $Q_1 = Q_2 = Q$ and the resonant frequency $\omega_r^2 = 1/L_1 C_1 = 1/L_2 C_2$.

Looking at Fig. 5.13 (c), the output voltage can be given as

$$V_o = -\frac{j}{\omega_r C_2} I_2 \quad \ldots (2)$$

To calculate V_o/V_1 it is necessary to represent I_2 in terms of V_1. For this we have to find the transfer admittance Y_T. Let us consider the circuit shown in Fig. 5.14. For this circuit, the transfer admittance can be given as

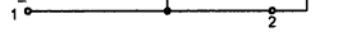


Fig. 5.14

$$Y_T = \frac{I_2}{V_1} = \frac{I_2}{I_1 Z_{11}} = \frac{A_i}{Z_{11}}$$

By doing similar analysis as for Z_i we can write

$$Z_o + Z_L = \frac{\omega_r L_2}{Q} + (1 + j2Q\delta)$$

Then

$$Y_T = \frac{Z_f}{Z_f^2 - Z_i (Z_o + Z_L)} = \frac{1}{Z_f - Z_i (Z_o + Z_L) / Z_f}$$

$$Y_T = \frac{1}{j\omega_r k\sqrt{L_1 L_2} - \dfrac{\left[\dfrac{\omega_r L_1}{Q}(1 + j2Q\delta)\left\{\dfrac{\omega_r L_2}{Q}(1 + j2Q\delta)\right\}\right]}{j\omega_r k\sqrt{L_1 L_2}}}$$

$$Y_T = \frac{kQ^2}{\omega_r \sqrt{L_1 L_2}\left[4Q\delta - j(1 + k^2Q^2 - 4Q^2\delta^2)\right]} \quad \ldots (3)$$

Substituting value of I_2, i.e. $V_i \times Y_T$ we get

$$V_o = \frac{-j}{\omega_r C_2} \frac{j g_m V_i}{\omega_r C_1}\left[\frac{kQ^2}{\omega_r \sqrt{L_1 L_2}\left[4Q\delta - j(1 + k^2Q^2 - 4Q^2\delta^2)\right]}\right]$$

$$\because V_i = \frac{j g_m V_1}{\omega C_1}$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = g_m \omega_r^2 L_1 L_2\left[\frac{kQ^2}{\omega_r \sqrt{L_1 L_2}\left[4Q\delta - j(1 + k^2Q^2 - 4Q^2\delta^2)\right]}\right]$$

$$\because \frac{1}{\omega_r C} = \omega_r L$$

$$= \left[\frac{g_m \omega_r \sqrt{L_1 L_2}\, kQ^2}{4Q\delta - j(1 + k^2Q^2 - 4Q^2\delta^2)}\right] \quad \ldots (4)$$

Taking the magnitude of equation (4) we have

$$|A_v| = g_m \omega_r \sqrt{L_1 L_2}\, Q \frac{kQ}{\sqrt{1 + k^2Q^2 - 4Q^2\delta^2 + 16Q^2\delta^2}} \quad \ldots (5)$$

The Fig. 5.15 shows the universal response curve for double tuned amplifier plotted with kQ as a parameter.

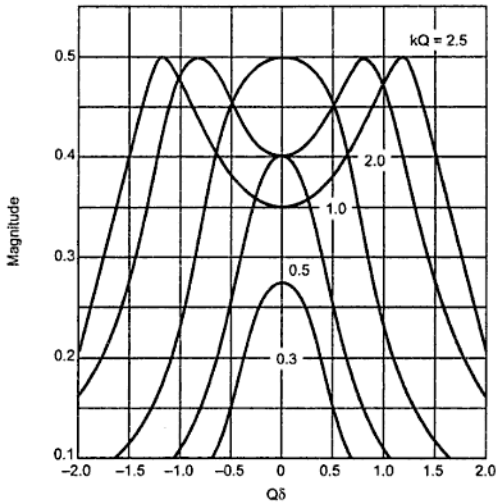


Fig. 5.15

The frequency deviation δ at which the gain peaks occur can be found by maximising equation (4), i.e.

$$4Q\delta - j(1 + k^2Q^2 - 4Q^2\delta^2) = 0 \quad \ldots (6)$$

As shown in the Fig. 5.16, two gain peaks in the frequency response of the double tuned amplifier can be given at frequencies :

$$f_1 = f_r\left(1 - \frac{1}{2Q}\sqrt{k^2Q^2 - 1}\right) \text{ and}$$

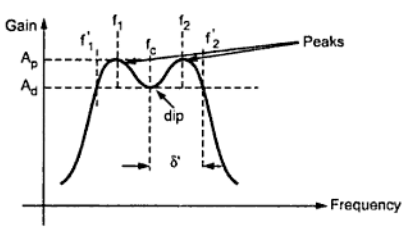


Fig. 5.16

$$f_2 = f_r\left(1+\frac{1}{2Q}\sqrt{k^2Q^2-1}\right) \quad \ldots (7)$$

At $k^2Q^2 = 1$, i.e. $k = \frac{1}{Q}$, $f_1 = f_2 = f_r$. This condition is known as **critical coupling**. For values of $k < 1/Q$, the peak gain is less than maximum gain and the coupling is poor.

At $k > 1/Q$, the circuit is overcoupled and the response shows the double peak. Such double peak response is useful when more bandwidth is required.

The gain magnitude at peak is given as

$$|A_p| = \frac{g_m \omega_0 \sqrt{L_1 L_2}\, kQ}{2} \quad \ldots (8)$$

and gain at the dip at $\delta = 0$ is given as

$$|A_d| = |A_p| \frac{2kQ}{1+k^2Q^2} \quad \ldots (9)$$

The ratio of peak gain and dip gain is denoted as γ and it represents the magnitude of the ripple in the gain curve.

$$\gamma = \left|\frac{A_p}{A_d}\right| = \frac{1+k^2Q^2}{2kQ} \quad \ldots (10)$$

Using quadratic simplification and choosing positive sign we get

$$kQ = \gamma+\sqrt{\gamma^2-1} \quad \ldots (11)$$

The bandwidth between the frequencies at which the gain is $|A_d|$ is the useful bandwidth of the double tuned amplifier. It is given as

$$BW = 2\delta' = \sqrt{2}\,(f_2 - f_1) \quad \ldots (12)$$

At 3 dB bandwidth,

$$\gamma = \sqrt{2}$$

$$\therefore \quad kQ = \gamma+\sqrt{\gamma^2+1} = \sqrt{2}+\sqrt{\sqrt{2}^2+1} = 2.414$$

$$\therefore \quad 3 \text{ dB BW} = 2\delta' = \sqrt{2}\,(f_2 - f_1)$$

$$= \sqrt{2}\left[f_r\left(1+\frac{1}{2Q}\sqrt{k^2Q^2-1}\right) - f_r\left(1-\frac{1}{2Q}\sqrt{k^2Q^2-1}\right)\right]$$

$$= \sqrt{2}\left[\left(\frac{f_r}{Q}\sqrt{k^2Q^2-1}\right)\right]$$

$$= \sqrt{2}\left[\frac{f_r}{Q}\sqrt{(2.414)^2-1}\right] = \frac{3.1\, f_r}{Q}$$

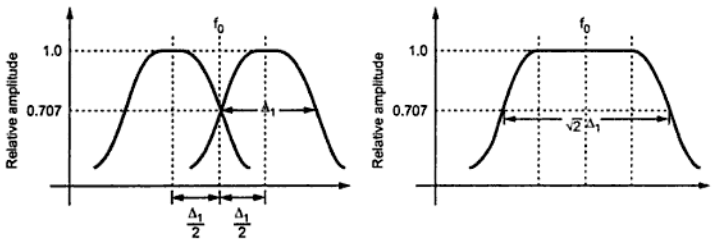
We know that, the 3 dB bandwidth for single tuned amplifier is 2 f_r/Q. Therefore, the 3 dB bandwidth provided by double tuned amplifier ($3.1f_r/Q$) is substantially greater than the 3 dB bandwidth of single tuned amplifier.

Compared with a single tuned amplifier, the double tuned amplifier

1. Possesses a flatter response having steeper sides.
2. Provides larger 3 dB bandwidth.
3. Provides large gain-bandwidth product.

5.9 Stagger Tuned Amplifier

We have seen that double tuned amplifier gives greater 3 dB bandwidth having steeper sides and flat top. But alignment of double tuned amplifier is difficult. To overcome this problem two single tuned cascaded amplifiers having certain bandwidth are taken and their resonant frequencies are so adjusted that they are separated by an amount equal to the bandwidth of each stage. Since the resonant frequencies are displaced or staggered, they are known as stagger tuned amplifiers. The advantage of staggered tuned amplifier is to have a better flat, wideband characteristics in contrast with a very sharp, rejective, narrow band characteristic of synchronously tuned circuits (tuned to same resonant frequencies). Fig. 5.17 shows the relation of amplification characteristics of individual stages in a staggered pair to the overall amplification of the two stages.



(a) Response of individual stages (b) Overall response of staggered pair

Fig. 5.17

The overall response of the two stage stagger-tuned pair is compared in Fig. 5.18 with the corresponding individual single tuned stages having same resonant circuits. Looking at Fig. 5.18, it can be seen that staggering reduces the total amplification of the center frequency to 0.5 of the peak amplification of the individual stage, and at the centre frequency each stage has an amplification that is 0.707 of the peak amplification of the individual stage. Thus the equivalent voltage amplification per stage of the staggered pair is 0.707 times as great as when the same two stages are used without staggering. However, the half power (3 dB) bandwidth of the staggered pair is $\sqrt{2}$ times as great as the half

The bandwidth of n stage identical amplifier is given as

$$BW_n = f_2 - f_1 = (f_2 - f_r) + (f_r - f_1)$$

$$= \frac{f_r}{2Q_{eff}}\sqrt{2^{\frac{1}{n}} - 1} + \frac{f_r}{2Q_{eff}}\sqrt{2^{\frac{1}{n}} - 1}$$

$$= \frac{f_r}{Q_{eff}}\sqrt{2^{\frac{1}{n}} - 1}$$

$$= BW_1\sqrt{2^{\frac{1}{n}} - 1} \quad \ldots (13)$$

where BW_1 is the bandwidth of single stage and BW_n is the bandwidth of n stages.

Example 5.3 : *The bandwidth for single tuned amplifier is 20 kHz. Calculate the bandwidth if such three stages are cascaded. Also calculate the bandwidth for four stages.*

Solution : i) We know that,

$$BW_n = BW_1\sqrt{2^{\frac{1}{n}} - 1} = 20\times10^3\times\sqrt{2^{\frac{1}{3}} - 1}$$

$$= \mathbf{10.196\ kHz}$$

ii) $$BW_n = 20\times10^3\times\sqrt{2^{\frac{1}{4}} - 1} = \mathbf{8.7\ kHz}$$

The above example shows that bandwidth decreases as number of stages increase.

5.11 Effect of Cascading Double Tuned Amplifiers on Bandwidth

When a number of identical double tuned amplifier stages are connected in cascade, the overall bandwidth of the system is thereby narrowed, and the steepness of the sides of the response is increased, just as when single tuned stages are cascaded. The quantitative relation between the 3 dB bandwidth of n identical double tuned critically coupled stages compared with the bandwidth Δ_2 of such a system can be shown to be 3 dB bandwidth for

$$\text{n identical stages double tuned amplifiers} = \Delta_2 \times \left(\sqrt{2^{\frac{1}{n}} - 1}\right)^{\frac{1}{4}} \quad \ldots (1)$$

where Δ_2 = 3 dB bandwidth of signal stage double tuned amplifier

Key Point : *The equation (1) assumes that the bandwidth Δ_2 is small compared with the resonant frequency.*

Disadvantages :

1) Since they use inductors and capacitors as tuning elements, the circuit is bulky and costly.

2) If the band of frequency is increased, design becomes complex.

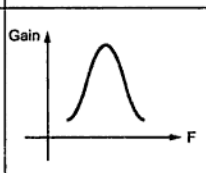
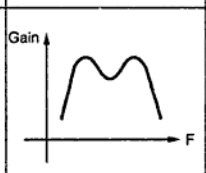
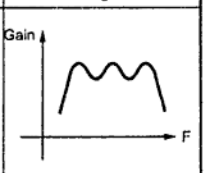
3) They are not suitable to amplify audio frequencies.

5.13 Applications of Tuned Amplifiers

The important applications of Tuned Amplifiers are as follows :

1. Tuned amplifiers are used in radio receivers to amplify a particular band of frequencies for which the radio receiver is tuned.
2. Tuned class B and class C amplifiers are used as an output RF amplifiers in radio transmitters to increase the output efficiency and to reduce the harmonics.
3. Tuned amplifiers are used in active filters such as low pass, high pass and band pass to allow amplification of signal only in the desired narrow-band.

5.14 Comparison between Tuned Circuits

Sr. No.	Parameter	Single Tuned Circuit	Double Tuned Circuit	Stragger Tuned Circuit
1.	Number of tuned circuits	One	Two	More than two
2.	Q factor	High	High	Moderate low
3.	Selectivity	Very High	Moderate	Low
4.	Bandwidth	Small	Moderate	High
5.	Frequency response Vs gain			
6.	Application	RF amplifier stage in radio receivers	If amplifier stage in radio receiver	Band-pass filter

5.15 Pulse Response of Tuned Amplifiers

The rectangular pulse is the basic waveform of radar and of digital systems. The Fig. 5.19 shows the ideal form of rectangular pulse. It consists of a positive step function at t = 0 and a negative step function to end the pulse.

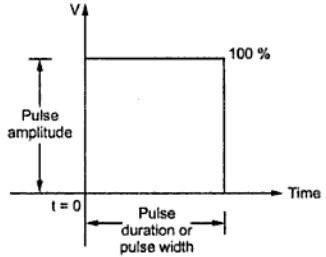


Fig. 5.19 Ideal rectangular pulse

Eventhough, if we apply ideal rectangular pulse at the input of an amplifier we will not get the ideal pulse at the output of amplifier. However, we get the distorted pulse at the output as shown in the Fig. 5.20.

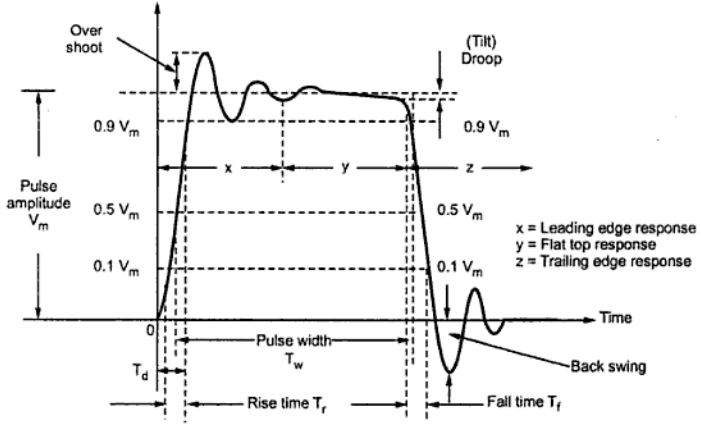


Fig. 5.20 Distorted pulse shape of pulse transformer output

As shown in the Fig. 5.20, there are various parameters which define the limits of permissible pulse distortion. Let us define these parameters.

a) Pulse amplitude (V_m) : It is the maximum absolute peak value of the pulse excluding the unwanted spikes.

b) Rise time (T_r) : It is time taken by the output pulse to rise from 10 % of peak pulse amplitude to 90 % of peak pulse amplitude, during its first attempt. Sometimes it may be defined as the time taken by the output pulse response to rise from 0 to pulse amplitude, for the first time.

c) Delay time (T_d) : The delay time is arbitrarily defined as the time for the pulse to reach 50 % of its final value, starting from t = 0.

d) Overshoot : The amount by which the output pulse exceeds its peak amplitude is called overshoot. Overshoot is caused by inclusion of inductive circuit elements, producing a second-order response with conjugate poles.

e) Pulse width (T_w) : The time interval between the first and last instants at which the instantaneous amplitude reaches 50 % of the peak amplitude. This is also called **pulse duration.**

f) Droop : It is the displacement of the pulse amplitude during its flat response. It is also called **tilt.**

g) Fall Time (T_f) : It is the time taken by the output pulse to decrease from 90% of its peak amplitude to 10% of its peak amplitude, during trailing edge response. It is also called **decay time.**

h) Backswing : The portion of the trailing edge which extends below the zero amplitude level, is called backswing.

5.16 Bandwidth Requirements for Pulse Amplification

In general, amplification of pulse signal requires wide bandwidth. Such a wide band response is observed in the video **amplifier.** Such amplifiers are designed to provide a continuous frequency response starting from a frequency very close to zero to the upper limit of frequency closer to 10 MHz to 20 MHz. When such a video amplifier is used for pulse amplification, the lowest frequency is the frequency of repetition of the signal. For different applications, the lowest frequency is also different. For example the lowest frequency encountered for television signal communication is 30 Hz which is the picture rate. While for some other type of pulse communication is 6 to 8 kHz. Obviously the pass band should enclose all the important signals in the frequency band.

When the input applied to circuit is non-sinusoidal i.e. a pulse, then the response of the circuit to such input is transient response. Consider a pulse train as shown in the Fig. 5.21.

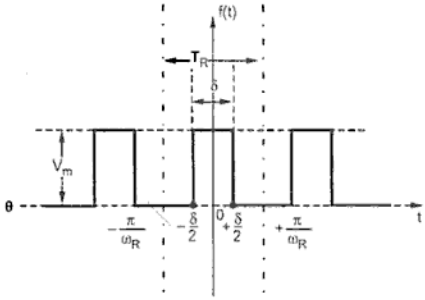


Fig. 5.21 Pulse train

Let ω_R be the **angular repetition frequency**. Hence the repetition frequency f_R is given by

$$f_R = \frac{2\pi}{\omega_R} \quad \ldots(1)$$

Hence the time required for repeating cycles is given by,

$$T_R = \frac{1}{f_R} = \frac{2\pi}{\omega_R} \quad \ldots(2)$$

The pulse train can be mathematically analyzed using **Fourier series**. Given pulse train can be represented using Fourier series as follows,

$$f(t) = a_0 + \sum_{n=1}^{\infty} (a_n \cos n\omega_R t + b_n \sin n\omega_R t)$$

i.e.
$$f(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos n\omega_R t + \sum_{n=1}^{\infty} b_n \sin n\omega_R t \quad \ldots(3)$$

By definition, **a constant** term or d.c. component or average term is given by,

$$a_0 = \frac{1}{T_R} \int_{-\frac{\pi}{\omega_R}}^{+\frac{\pi}{\omega_R}} f(t)\, dt$$

Similarly by definition, the Fourier coefficients are given by,

$$a_n = \frac{2}{T_R} \int_{-\frac{\pi}{\omega_R}}^{+\frac{\pi}{\omega_R}} f(t) \cdot \cos n\omega_R t\, dt, \text{ and}$$

$$b_n = \frac{2}{T_R} \int_{-\frac{\pi}{\omega_R}}^{+\frac{\pi}{\omega_R}} f(t) \cdot \sin n\omega_R t \, dt$$

Now from Fig. 5.21 we can define a pulse mathematically as,

$$\left.\begin{aligned} f(t) &= V_m, \; -\delta/2 < t < \delta/2 \\ &= 0, \; -\frac{\pi}{\omega_R} < t < -\frac{\delta}{2}, \; \frac{\delta}{2} < t < \frac{\pi}{\omega_R} \end{aligned}\right\} \quad \ldots(4)$$

From the pulse waveform, it is clear that it is having even symmetry. So by the concepts of waveform symmetry, the Fourier coefficient $b_n = 0$. And the series will consists only cosine terms. Let us calculate remaining constants.

The d.c. component is given by,

$$a_0 = \frac{1}{T} \int_{-\pi/\omega_R}^{\pi/\omega_R} f(t) \, dt = \frac{\omega_R}{2\pi} \int_{-\delta/2}^{\delta/2} V_m dt$$

$$\therefore \quad a_0 = \frac{\omega_R V_m}{2\pi} [t]_{-\delta/2}^{\delta/2}$$

$$\therefore \quad a_0 = \left(\frac{\omega_R}{2\pi}\right) V_m \cdot \delta$$

$$\therefore \quad \boxed{a_0 = f_R \, \delta \, V_m} \quad \ldots(5)$$

The Fourier coefficient a_n is given by,

$$a_n = \frac{2}{T} \int_{-\pi/\omega_R}^{+\pi/\omega_R} f(t) \cdot \cos n\omega_R t \, dt = 2\left(\frac{\omega_R}{2\pi}\right) \int_{-\delta/2}^{+\delta/2} V_m \cos n \, \omega_R t \, dt$$

$$\therefore \quad a_n = 2 f_R V_m \int_{-\delta/2}^{+\delta/2} \cos 2\pi f_R n t \, dt$$

$$\therefore \quad a_n = 2 V_m f_R \left[\frac{\sin 2\pi f_R n t}{2\pi f_R n}\right]_{-\delta/2}^{+\delta/2}$$

$$\therefore \quad a_n = V_m f_R \left[\frac{\sin 2\pi f_R n\left(\frac{\delta}{2}\right) - \sin 2\pi f_R n(-\delta/2)}{\pi f_R n}\right]$$

$$\therefore \quad a_n = V_m f_R \left\{\frac{\sin \pi f_R n\delta - [-\sin \pi f_R n \, \delta]}{\pi f_R n}\right\}$$

$\ldots[\because \sin(-\theta) = -\sin\theta]$

$$\therefore \quad a_n = \frac{V_m f_R [2 \sin \pi f_R n\delta]}{\pi f_R n}$$

$$\therefore \quad \boxed{a_n = 2 V_m f_R \delta \cdot \frac{\sin (n\pi f_R \delta)}{n\pi f_R \delta}} \qquad \ldots(6)$$

Above equation (6) is in the form $\frac{(\sin x)}{x}$ where $x = n\pi f_R \delta$ and is as shown in the Fig. 5.22.

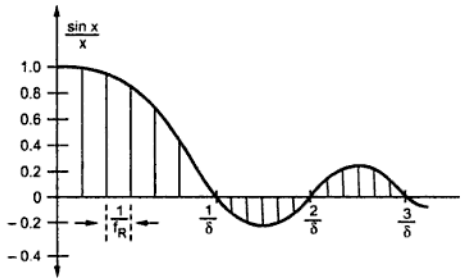


Fig. 5.22 Plot of harmonic amplitudes of pulse train

Thus from equation(6) we can find amplitudes of each harmonic for a pulse train with duration δ and frequency of repetition with peak value V_m.

The frequency at which function crosses zero is called **crossover frequency**. The crossover frequencies can be obtained by making value of function $\frac{(\sin x)}{x}$ as zero. Hence we get, the condition for crossover frequencies as,

$$\frac{\sin(n\pi f_R \delta)}{n \pi f_R \delta} = 0$$

i.e. $\quad n\pi f_R \delta = \sin^{-1}(0) = m\pi$

$$\therefore \quad \boxed{n f_R = \frac{m}{\delta}} \qquad \ldots(7)$$

where m is an integer with values 1, 2, 3, ...

Thus the crossover of the functions takes at frequencies $\frac{1}{\delta}, \frac{2}{\delta}, \frac{3}{\delta}, \frac{4}{\delta}, \ldots$ (where m = 1, 2, 3, 4, ...). So it can be noticed that width of frequencies between two crossovers forming loops becomes narrower for larger pulse width. On the other hand **for narrower pulses, the width of loops between any two crossover frequencies increases.** For example, if the pulse width is of 10 μs, then first crossover frequency occurs at 0.1 MHz while second

crossover frequency occurs at 0.2 MHz. But now if the pulse width is reduced to 1 μs, then first crossover frequency occurs at 1 MHz while second crossover frequency occurs at 2 MHz. From the equations obtained we can also calculate the number of harmonics present in each loop. It is given by,

$$\therefore \quad \boxed{n = \frac{1}{f_R \, \delta}} \qquad \ldots(8)$$

As the number of harmonics is inversly proportional to the repetition frequency f_R, more number of harmonics appear in each loop with repetition frequency goes on reducing. Thus within a limit only a single pulse is transmitted, we get continuous spectrum of frequencies as shown in the Fig. 5.22.

By using concept of Fourier integral, the envelope of continuous spectrum of frequencies can be obtained as

$$F(j\omega) = \int_{-\infty}^{\infty} f(t)\, e^{-j\omega t}\, dt$$

Hence for a single pulse considered in the begining, we can write,

$$F(j\omega) = \int_{-\delta/2}^{\delta/2} V_m e^{-j\omega t}\, dt = \frac{V_m}{-j\omega}\left[e^{-j\omega t}\right]_{-\delta/2}^{\delta/2}$$

$$\therefore \quad F(j\omega) = \frac{V_m}{-j\omega}\left[e^{-\frac{j\omega\delta}{2}} - e^{+\frac{j\omega\delta}{2}}\right]$$

$$\therefore \quad F(j\omega) = \frac{V_m}{\omega}\left[\frac{e^{j\frac{\omega\delta}{2}} - e^{-j\frac{\omega\delta}{2}}}{j}\right]$$

$$F(j\omega) = \frac{2V_m}{\omega}\left[\frac{e^{j\frac{\omega\delta}{2}} - e^{-j\frac{\omega\delta}{2}}}{j2}\right]$$

$$\therefore \quad F(j\omega) = \frac{2V_m}{\omega}\left[\sin\frac{\omega\delta}{2}\right]$$

$$\therefore \quad \boxed{F(j\omega) = \delta V_m\left[\frac{\sin\left(\frac{\omega\delta}{2}\right)}{\frac{\omega\delta}{2}}\right]} \qquad \ldots(9)$$

As above function is also of the form $\frac{(\sin x)}{x}$, the amplitudes of the harmonics for a single pulse lie with the envelope only shown in the Fig. 5.22.

The **pulse amplification fidelity** mainly depends on the number of harmonic frequencies included in the passband of amplifier. It is observed that when only first zero is included in the envelope, then the pulse reproduction is resonably accurate. But when

the envelope includes fourth zero, then the pulse reproduction is excellent. Thus for better pulse reproduction, the bandwidth requirement of the amplifier is considered to be $\frac{1}{\delta}$ Hz.

5.17 Shunt Peaking Circuits for Increased Bandwidth

The video amplifier, for pulse amplification requires very large bandwidth in the range of few Megahertz. In such amplifiers, at frequencies above certain range, the gain will fall due to the Miller effect capacitance of the transistor, reducing the bandwidth. One way to increase bandwidth is to decrease the load resistance, thus trading gain for bandwidth. We can solve this problem and extend f_2 values with higher loads by using an inductance in the load. The inductance in the load results a resonance with the input capacitance and raises the load impedance at those frequencies where the reactance of the shunting capacitance falls with frequency.

The Fig. 5.23 (a) shows the circuit with inductance in the load. Such circuit is called a shuntpeaked circuit, since L is in shunt with C_d.

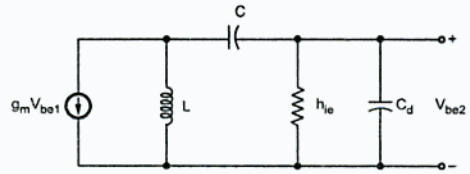
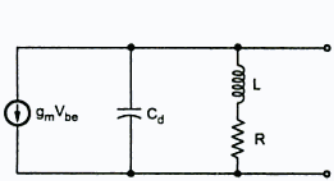
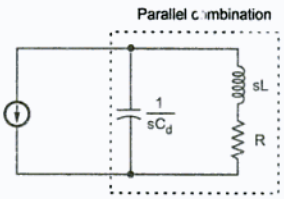


Fig. 5.23(a) Shunt peaked circuit

The Fig. 5.23 (b) shows the equivalent circuit of shunt peaked circuit. Here, h_{ie} is reflected as a series resistance with L. The total resistance in series with L is the equivalent input resistance plus the other resistance required to produce a given midfrequency gain. At high frequencies capacitor C is shorted and can be neglected.



(b) Equivalent circuit of shunt peaking circuit



(c) Laplace domain network

Fig. 5.23

Substituting value of ω_2 from equation (1) we have

$$q = \frac{1}{RC_d}\frac{L}{R} = \frac{L}{R^2C_d}$$

$$= \frac{L}{4\,L_{crit}} \qquad \because L_{crit} = \frac{R^2C_d}{4}$$

Using q and S = jω for the steady state, the gain magnitude is

$$|A_{VH}| = A_{im}\left[\frac{1 + q^2(\omega/\omega_2)^2}{1 + (1-2q)(\omega/\omega_2)^2 + q^2(\omega/\omega_2)^4}\right]^{1/2} \qquad ...(3)$$

The above equation has the form

$$H(\omega) = \frac{1 + a_1\omega^2 + a_2\omega^4 + ...}{1 + b_1\omega^2 + b_2\omega^4 + ...}$$

and we can get the flattest monotonic response by equating coefficients of equivalent powers of the variable such that $a_1 = b_1$, $a_2 = b_2$ and so on.

Thus, equating coefficients of $(\omega/\omega_2)^2$ we have,

$$q^2 = 1 - 2q$$

$$\therefore \quad q^2 + 2q - 1 = 0$$

Using $$q = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} = \frac{-2 \pm \sqrt{2^2 - 4\times1\times-1}}{2\times1}$$

$$= -1 \pm \sqrt{2}$$

$$\therefore \quad q = 0.414 \text{ or } -2.414$$

Since negative value of q has no physical meaning we have,

$$q = 0.414 \qquad ...(4)$$

We have,

$$q = \frac{L}{4\,L_{crit}}$$

$$L = 4\,L_{crit}\,q$$

$$= 4\,L_{crit} \times 0.414 \qquad \because q = 0.414$$

$$\therefore \quad L = 1.656\,L_{crit}$$

$$= 1.656\,\frac{R^2C_d}{4} \qquad \because L_{crit} = \frac{R^2C_d}{4}$$

$$\therefore \quad L = 0.414\,R^2C_d \qquad ...(5)$$

The equation (5) gives the condition for maximally flat gain. The Fig. 5.24 shows response of the shunt-peaked amplifier for different values of q. The curve with q = 0 is the curve for the uncompensated amplifier. With q = 0.414, the bandwidth of the compensated amplifier is given by $f_2' = 1.72\,f_2$.

The phase angle of the shunt-peaked circuit is given by

$$\theta = -\tan^{-1}\frac{\omega}{\omega_2}\left[1-q+q^2\left(\frac{\omega}{\omega_2}\right)^2\right]$$

Taking the derivative $d\theta/d\omega$, it is found that for constant time delay q = 0.32. We obtain flat gain with q = 0.414 and constant time delay with q = 0.32. Thus, it is necessary to compromise the value of q. The q = 0.35 is the best compromise.

Example 5.6 : *For a shunt peaked FET amplifier with g_m = 5 mA/V, A_{vmid} = – 15, C_{gs} = 1 pF and C_{gd} = 3 pF, find :*

a. The value of R

b. Miller effect capacitance

c. The limit frequency of the uncompensated amplifier

d. The value of L

e. The possible extension of frequency range.

Solution : a) We have,

$$A_{vmid} = -g_m R = -15$$

$$\therefore \quad R = \frac{-15}{-5\times10^{-3}} = \mathbf{3\ K}$$

b) The Miller effect capacitance is given by

$$C_d = C_{gs} + (1 + g_m R)\, C_{gd}$$

$$= 1 \times 10^{-12} + (1 + 15) \times 3 \times 10^{-12}$$

$$= \mathbf{49\ pF}$$

c) The limit frequency of the uncompensated amplifier is

$$f_2 = \frac{1}{2\pi C_d R} = \frac{1}{2\pi\times 49\times10^{-12}\times 3\times10^{3}}$$

$$= \mathbf{1.08\ MHz}$$

d) $$L = q R^2 C_d = 0.414 \times (3 \times 10^3)^2 \times 49 \times 10^{-12}$$

$$= \mathbf{182.574\ \mu H}$$

c) The bandwidth is given as

$$BW = \frac{f_r}{Q_{eff}} = \frac{225\times10^3}{14.147}$$

$$= \textbf{15.904 kHz}$$

Example 5.8 : *The transistor shown in Fig. 5.25 has* $h_{fe} = 50$ *and input resistance of* $200\ \Omega$.

The coil used has Q factor = 30

Calculate : i) Resonant frequency of the tuned circuit

ii) Impedance of the tuned circuit.

iii) Voltage gain of the stage.

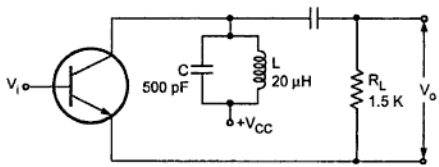


Fig. 5.25

Solution : i) Resonant frequency :

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{20\times10^{-6}\times500\times10^{-12}}}$$

$$= \frac{1}{2\pi\times10^{-7}} = 0.159\times10^7\ \text{Hz}$$

$$= \textbf{1.59 MHz.}$$

ii) We know that

$$Q_r = \frac{R_p}{\omega_r L}$$

$\therefore$ Impedance of tuned circuit R_p

$$= Q_r\ \omega_r\ L = 30\times2\pi\times1.59\times10^6\times20\times10^{-6}$$

$$= 5994\ \Omega$$

iii) Voltage gain of stage A_v

$$A_v = \frac{A_1 R'_L}{R'_i}$$

$$= \frac{-h_{fe}(R_p \parallel R_L)}{R_i} = \frac{-50(5994 \parallel 1.5\,K)}{200}$$

$$= -300$$

Example 5.9 : *A tuned amplifier should have a gain of 50 for a centre frequency of 10.7 MHz and bandwidth of 200 kHz. A FET with g_m = 5 mA/V and r_d = 100 K is to be used. Calculate the tank circuit parameters.*

Solution :

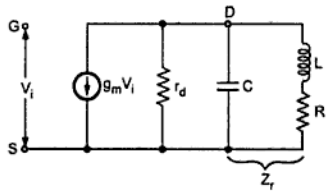


Fig. 5.26

$$f_r = \frac{1}{2\pi\sqrt{LC}} = 10.7\ \text{MHz} \quad \ldots (1)$$

$$\therefore \quad Q = \frac{f_r}{3\,\text{dB (BW)}} = \frac{10.7\ \text{MHz}}{200\ \text{kHz}} = 53.5$$

$$\therefore \quad 53.5 = \frac{\omega_r L}{R} \quad \ldots (2)$$

$$A_v = -50 = -g_m R_L$$

$$\therefore \quad R_L = \frac{50}{5\times10^{-3}}$$

$$= 10\ \text{k}\Omega$$

where $R_L = r_d \parallel R_p$

$$\therefore \quad \frac{1}{R_L} = \frac{1}{r_d} + \frac{1}{R_p}$$

Solution : i) f_r = Resonant frequency

$$= \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{400\,\mu H \times 2500\,pF}}$$

$$= \mathbf{0.159\ MHz}$$

ii) Tuned circuit dynamic resistance = $R_p = \frac{L}{CR}$

$$= \frac{400\,\mu H}{2500\,pF \times 5\,\Omega} = \frac{10^6 \times 80}{2500}$$

$$= 0.032 \times 10^6 = \mathbf{32\ k\Omega}$$

iii) Gain at resonance $= A_v = -g_m R_L = -g_m R_p$

$$= 6\ mA/V \times 32\ k\Omega = -192$$

iv) The signal bandwidth = BW = $\frac{f_r}{Q}$

$$Q = \frac{\omega_r L}{R} = \frac{2\pi \times 0.159 \times 10^6 \times 400 \times 10^{-6}}{5\,\Omega}$$

$$= 79.92$$

$$BW = \frac{f_r}{Q} = \frac{0.159\ MHz}{79.92}$$

$$= \mathbf{1.98\ kHz.}$$

Example 5.11 : *An RF amplifier of Fig. 5.27 uses FET having r_d = 500 kΩ and g_m = 5 mA/V. The drain tuned circuit consists of a coil of 200 μH and Q = 50 and parallel capacitance tuned to f_r = 1.59 MHz, find gain at,*

i) The resonant frequency ω_r ii) A frequency 10 kHz higher than ω_r.

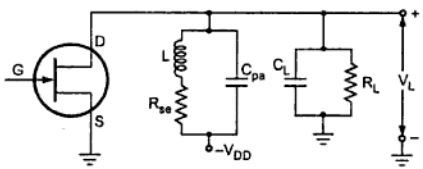


Fig. 5.27

Solution : i) $R_L = r_d \parallel R_p$

R_p = Tank circuit impedance at resonance = $\frac{L}{CR}$

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

$$\therefore \quad f_r^2 = \frac{1}{4\pi^2 LC}$$

$$\therefore \quad C = \frac{1}{4\pi^2 f_r^2 LC}$$

$$= \frac{1}{2\pi^2 (1.59\times10^6)^2 \times 200\times10^{-6}}$$

$$= 50\times10^{-12}\text{F} = 50\text{ pF}$$

$$Q = \frac{\omega_r L}{R} = \frac{2\pi f_r L}{R}$$

$$R = \frac{2\pi f_r L}{R}$$

$$= \frac{2\pi\times(1.59\times10^6)\times200\times10^6}{50} = 40\ \Omega$$

$$R_p = \frac{L}{CR} = \frac{200\times10^{-6}}{50\times10^{-12}\times40} = 100\text{ K}$$

$$R_L = \frac{r_d R_p}{r_d + R_p}$$

$$= \frac{500\times10^3\times100\times10^3}{(500+100)\times10^3} = 83.33\times10^3$$

$$A_v = -g_m R_L = 5\times10^{-3}\times83.33\times10^3$$

$$A_v = \textbf{416.67 at resonance frequency } \omega_r$$

ii) At $f = f_r + 10\text{ kHz} = 1.6\text{ MHz}$

$$\left|\frac{A_v}{A_{v(\text{at resonance})}}\right| = \frac{1}{\sqrt{1+\left(\frac{f}{f_r}\right)^2}}$$

$$\therefore \quad |A_v| = \frac{|A_{v\,(\text{at resonance})}|}{\sqrt{1+\left(\frac{f}{f_r}\right)^2}} = \frac{416.67}{\sqrt{1+\left(\frac{1.6}{1.59}\right)^2}}$$

$$= 293.7$$

Example 5.12 : *A single tuned amplifier using FET has tank circuit components $L = 100\ \mu H$, $R = 5\ \Omega$ and $C = 1000\ pF$. The FET used has $r_d = 500\ k\Omega$ and $g_m = 5\ mA/V$ find i) Resonant frequency ii) Tank circuit impedance at resonance*

iii) Voltage gain at resonance and iv) Bandwidth

Solution : i) Resonant frequency $f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{100\,\mu H \times 1000\,pF}}$

$$= \mathbf{503.29\ kHz}$$

ii) Tank circuit impedance at resonance can be given as

$$R_p = \frac{L}{CR} = \frac{100\ \mu H}{1000\,pF \times 5}$$

$$= \mathbf{20\ K}$$

iii) $$A_v = -g_m R_L = -g_m (r_d \parallel R_p) = -5\ mA/V\ (500\ K \parallel 20\ K)$$

$$= \mathbf{-96.15}$$

iv) $$BW = \frac{f_r}{Q}$$

$$= \frac{f_r R}{\omega_r L} \quad \therefore Q = \frac{\omega_r L}{R}$$

$$= \frac{R}{2\pi L} = \frac{5}{2\pi \times 100\,\mu H} = \mathbf{7.957\ kHz}$$

Example 5.13 : *A tuned amplifier is required to have a voltage gain of 30 at 10.7 MHz with 200 kHz BW. An FET with $g_m = 5\ mA/V$ and $r_d = 100\ k\Omega$ is available. Calculate values of tank circuit elements.*

Solution : Given : $|A_v| = 30$, $f_r = 10.7$ MHz

BW = 200 kHz, $g_m = 5$ mA/V and $r_d = 100$ kΩ

$$BW = \frac{f_r}{Q}$$

$$\therefore \quad Q = \frac{f_r}{BW} = \frac{10.7\ MHz}{200\ kHz} = 53.5$$

$$Q = \frac{\omega_r L}{R} = \frac{2\pi f_r L}{R}$$

$$\therefore \quad \frac{L}{R} = \frac{Q}{2\pi f_r} = \frac{53.5}{2\pi \times 10.7\ \text{MHz}}$$

$$= 795 \times 10^{-9}$$

$$|A_v| = g_m R_L = 30$$

$$\therefore \quad R_L = (r_d || R_p) = \frac{30}{5\ \text{mA / V}} = 6\ \text{K}$$

$$\therefore \quad 100\ \text{K} || R_p = 6\ \text{K}$$

$$\therefore \quad R_p = 6383\ \Omega$$

We know that,

$$R_p = \frac{L}{CR} = \frac{1}{C} \times 795 \times 10^{-9}$$

$$\therefore \quad C = \frac{795 \times 10^{-9}}{R_p} = \frac{795 \times 10^{-9}}{6383}$$

$$= \mathbf{124.5\ pF}$$

We know that

$$f_r = \frac{1}{2\pi \sqrt{LC}}$$

$$\therefore \quad 10.7 \times 10^6 = \frac{1}{2\pi \sqrt{L \times 124.5\ \text{pF}}}$$

$$\therefore \quad L = \mathbf{1.777\ \mu H}$$

We have

$$R_p = \frac{L}{CR}$$

$$\therefore \quad R = \frac{L}{CR_p} = \frac{1.777\ \mu\text{H}}{124.5\ \text{pF} \times 6383}$$

$$= \mathbf{2.236\ \Omega}$$

Therefore, elements of tank circuits are :

L = 1.777 μH, C = 124.5 pF and R = 2.236 Ω

Review Questions

1. *What do you mean by tuned amplifiers ?*
2. *Define Q.*
3. *What is bandpass amplifier ?*
4. *Write a note on parallel resonant circuit.*
5. *Write a note on resonant circuit with series resistance.*
6. *Derive the expression for bandwidth of parallel resonant circuit.*
7. *Derive an expression for bandwidth of a single stage tuned amplifier.*
8. *Draw the typical graph of gain versus frequency for single tuned amplifier.*
9. *With circuit diagram, a.c. equivalent circuit and frequency response characteristics, explain the operation of a single tuned amplifier.*
10. *Draw the primary tuned amplifier with BJT and derive the expression for bandwidth.*
11. *Draw the secondary tuned amplifier with FET and derive the bandwidth expression for.*
12. *Draw and explain the circuit of double tuned amplifier with the help of frequency response.*
13. *What is stagger tuning ?*
14. *Explain the frequency response of stagger tuned pair.*
15. *Derive the expression for bandwidth of a two stage synchronously tuned amplifier.*
16. *What is the effect of cascading single tuned amplifiers on bandwidth ? Derive the expression for it.*
17. *What is the effect of cascading double tuned amplifiers on bandwidth ?*
18. *Discuss advantages and disadvantages of tuned amplifiers.*
19. *What are the applications of tuned amplifier ?*
20. *Write a note on pulse response of tuned amplifiers.*
21. *What is the necessity of shunt peaking circuit ?*
22. *Derive the expressions for L_{crit} and extended f_2 for amplifier with shunt peaking circuit.*

❑❑❑

6.2 Features of Power Amplifiers

The various features of power amplifiers are,

1. A power amplifier is the last stage of multistage amplifier. The previous stages develop sufficient gain and the **input signal level or** amplitude of a power **amplifier is large** of the order of few volts.
2. The **output of power amplifier has large current and** voltage swings. As it handles large signals called power amplifiers.
3. **The h-parameter analysis** is applicable to the **small signal** amplifiers and hence **cannot be used for the** analysis of power amplifiers. The analysis of power amplifiers is carried out graphically by drawing a load line on the output characteristics of the transistors used in it.
4. The power amplifiers i.e large signal amplifiers are used to feed the loads like loudspeakers having low impedance. So for maximum power transfer the impedance matching is important. Hence **the power amplifiers** must have low **output impedance**. Hence common collecter or emitter follower circuit is very common in power amplifiers. The common emitter circuit with a step down transformer for impedance matching is also commonly used in power amplifiers.
5. The power amplifiers develop an a.c. power of the order of few watts. Similarly large power gets dissipated in the form of heat, at the junctions of the transistors used in the power amplifiers. **Hence the transistors used in the** power amplifiers **are of large size, having large power dissipation rating, called** power transistors. Such transistors have heat sinks. A heat sink is a metal cap having bigger surface area, press fit on the body of a transistor, to get more surface area, in order to dissipate the heat to the surroundings. In general, the power amplifiers have bulky components.
6. A faithful reproduction of the signal, after the conversion, is important. Due to nonlinear nature of the transistor characteristics, there exists a harmonic distortion in the signal. Ideally signal should not be distorted. Hence the analysis of **signal distortion in case of the power amplifiers is important.**
7. Many a times, the power amplifiers are used in public address systems and many audio circuits to supply large power to the loudspeakers. **Hence power amplifiers are also called audio amplifiers or** audio frequency (A.F.) power amplifiers.

6.3 Classification of Large Signal Amplifiers

For an amplifier, a quiescent operating point (Q point) is fixed by selecting the proper d.c. biasing to the transistors used. The quiescent operating point is shown on the load line, which is plotted on the output characteristics of the transistor. The position of the quiescent point on the load line decides the class of operation of the power amplifier. The various classes of the power amplifiers are :

i) Class A ii) Class B iii) Class C and iv) Class AB.

Such a load line is shown in the Fig. 6.3.

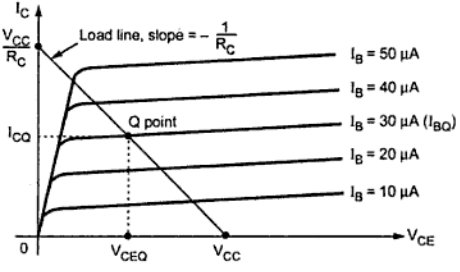


Fig. 6.3 Output characteristics with a load line

The characteristic curves are plotted for various values of I_B. The intersection of the output characteristic curve and a load line is the operating point. This point is fixed for a transistor called **quiescent point** or **Q point** as shown in the Fig. 6.3.

The values of collector current and the collector to emitter voltage, corresponding to the Q point are I_{CQ} and V_{CEQ} respectively. Hence the co-ordinates of the Q point are (V_{CEQ}, I_{CQ}). The corresponding value of the base current is denoted as I_{BQ}.

On this d.c. quiescent operating point, if an a.c. signal is superimposed, by the application of a.c. sinusoidal voltage at the input, the base current varies sinusoidally about its quiescent value I_{BQ} as shown in the Fig. 6.4 (a). Since the transistor is biased to operate in the active region, the output is linearly proportional to the input. The output i.e. the collector current is β times larger than the input base current in the common emitter configuration. Hence the collector current also varies sinusoidally about its quiescent value I_{CQ}. The output voltage also varies sinusoidally about its quiescent value V_{CEQ}. The sinusoidal variations in I_C and V_{CE} are shown in the Fig. 6.4 (b) and (c) respectively.

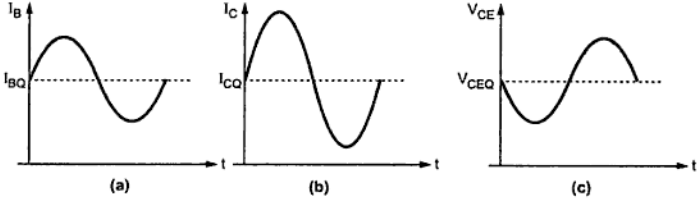


Fig. 6.4 Variations in I_B, I_C and V_{CE} due to the sinusoidal input

These variations in I_C and V_{CE}, due to the change in I_B, can be shown graphically with the help of a load line as shown in the Fig. 6.5.

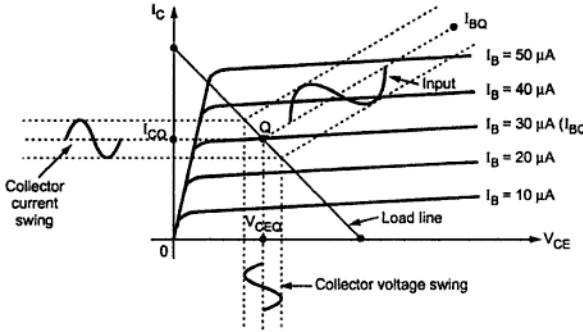


Fig. 6.5 Graphical representation of I_B, I_C and V_{CE} swings

The collector current varies above and below its quiescent value, in phase with the base current. The collector-to-emitter voltage varies above and below its quiescent value, 180° out of phase with the base current, as shown in the Fig. 6.5.

Now let us define the various classes of the power amplifiers, depending on the position of the Q point, on a load line.

6.3.1 Class A Amplifiers

The power amplifier is said to be class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input cycle.

Key Point : *For this class, position of the Q point is approximately at the midpoint of the load line.*

For all values of input signal, the transistor remains in the active region and never enters into cut-off or saturation region. When an a.c. input signal is applied, the collector voltage varies sinusoidally hence the collector current also varies sinusoidally. The collector current flows for 360° (full cycle) of the input signal. In other words, the angle of the collector current flow is 360° i.e. one full cycle.

The current and voltage waveforms for a class A operation are shown with the help of output characteristics and the load line, in the Fig. 6.6.

As shown in the Fig. 6.6, for full input cycle, a full output cycle is obtained. Here signal is faithfully reproduced, at the output, without any distortion. This is an important feature of a class A operation. The efficiency of class A operation is very small.

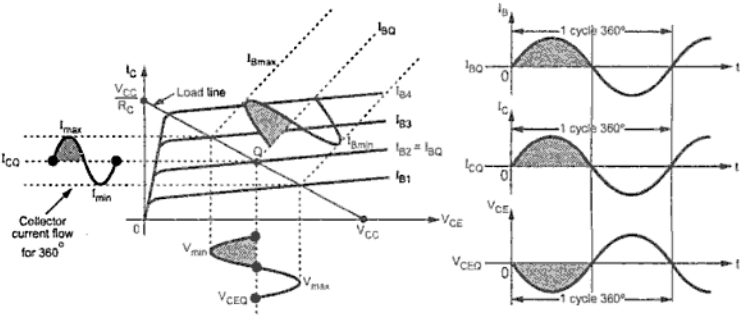


Fig. 6.6 Waveforms representing class A operation

6.3.2 Class B Amplifiers

The power amplifier is said to be class B amplifier if the Q point and the input signal are selected, such that the output signal is obtained only for one half cycle for a full input cycle.

Key Point : *For this operation, the Q point is shifted on X-axis i.e. transistor is biased to cut-off.*

Due to the selection of Q point on the X-axis, the transistor remains, in the active region, only for positive half cycle of the input signal. Hence this half cycle is reproduced at the output. But in a negative half cycle of the input signal, the transistor enters into a cut-off region and no signal is produced at the output. The collector current flows only for 180° (half cycle) of the input signal. In other words, the angle of the collector current flow is 180° i.e. one half cycle.

The current and voltage waveforms for a class B operation are shown in the Fig. 6.7.

As only a half cycle is obtained at the output, for full input cycle, the output signal is distorted in this mode of operation. To eliminate this distortion, practically two transistors are used in the alternate half cycles of the input signal. Thus overall a full cycle of output signal is obtained across the load. Each transistor conducts only for a half cycle of the input signal.

The efficiency of class B operation is much higher than the class A operation.

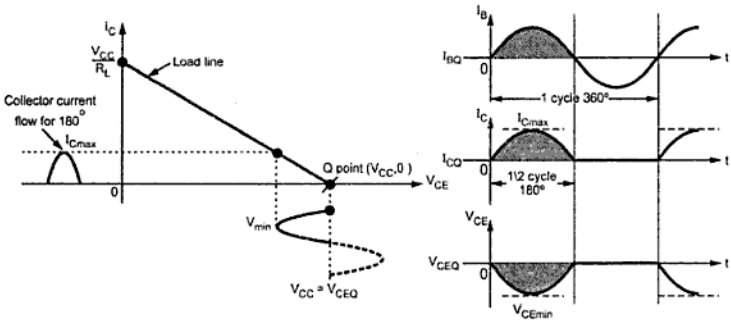


Fig. 6.7 Waveforms representing class B operation

6.3.3 Class C Amplifiers

The power amplifiers is said to be class C amplifier, if the Q point and the input signal are selected such that the output signal is obtained for less than a half cycle, for a full input cycle.

Key Point : *For this operation, the Q point is to be shifted below X-axis.*

Due to such a selection of the Q point, transistor remains active, for less than a half cycle. Hence only that much part is reproduced at the output. For remaining cycle of the input cycle, the transistor remains cut-off and no signal is produced at the output. The angle of the collector current flow is less than 180°.

The current and voltage waveforms for a class C amplifier operation are shown in the Fig. 6.8.

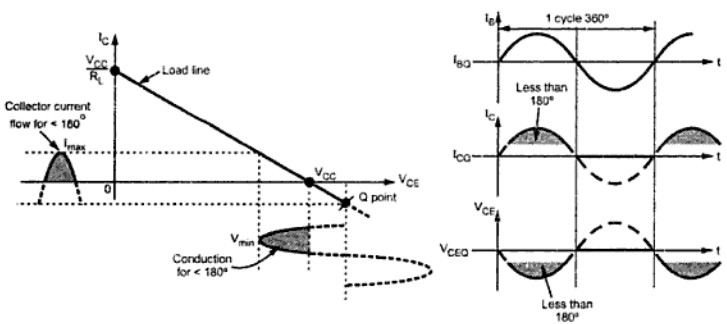


Fig. 6.8 Waveform representing class C operation

Key Point : *In class C operation, the transistor is biased well beyond cut-off. As the collector current flows for less than 180°, the output is much more distorted and hence the class C mode is never used for A.F. power amplifiers.*

But the efficiency of this class of operation is much higher and can reach very close to 100 %.

Applications : The class C operation is not suitable for audio frequency power amplifiers. The class C amplifiers are used in tuned circuits used in communication areas and in radio frequency (RF) circuits with tuned RLC loads. As used in tuned circuits, class C amplifiers are called **tuned amplifiers**. These are also used in mixer or converter circuits used in radio receivers and wireless communication systems.

The Fig. 6.9 shows the calss C tuned amplifier.

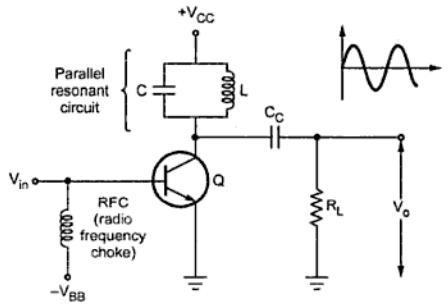


Fig. 6.9 Class C tuned amplifier

The LC parallel circuit is a **parallel** resonant circuit. This circuit acts as a load impedance. Due to class C operation, the collector current consists of a series of pulses containing harmonics i.e. many other frequency components along with the fundamental frequency component of input. The parallel tuned circuit is designed to be tuned to the fundamental input frequency. Hence it eliminates the harmonics and produce a sine wave of fundamental component of input signal. As the transistor and coil losses are small, the most of the d.c. input power is converted to a.c. load power. Hence efficiency of class C is very high.

6.3.4 Class AB Amplifiers

The power amplifier is said to be class AB amplifier, if the Q point and the input signal are selected such that the output signal is obtained for more than 180° but less than 360°, for a full input cycle.

Key Point : *The Q point position is above X-axis but below the midpoint of a load line.*

The current and voltage waveforms for a class AB operation, are shown in the Fig. 6.10.

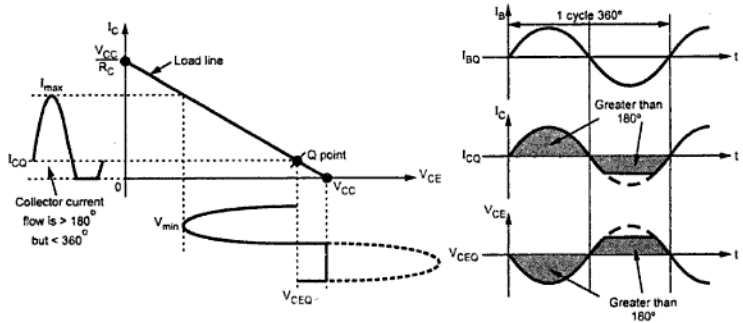


Fig. 6.10 Waveforms representing class AB operation

The output signal is distorted in class AB operation. The efficiency is more than class A but less than class B operation. The class AB operation is important to eliminate cross-over distortion.

In general as the Q point moves away from the centre of the load line below towards the X-axis, the efficiency of class of operation increases.

6.4 Class D Amplifiers

The Fig. 6.11 shows the basic concept of class D amplifier. The amplifier consists of two complementary symmetry transistors driving a load R_L. This means one transistor is p-n-p and other is n-p-n.

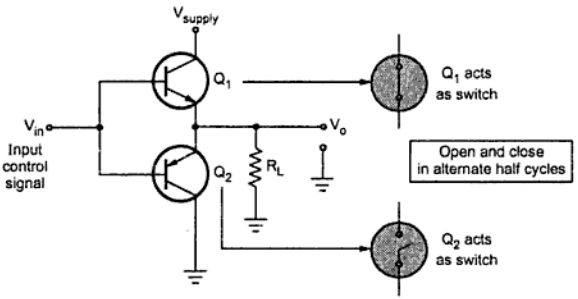


Fig. 6.11 Concept of class D amplifier

The transistors are biased in such a way that they behave as ideal switches. When transistor is ON, it is biased to saturation so that voltage across it is zero while current is high. When transistor is OFF, it is biased to cut-off so that current through it is zero while voltage is high. Thus when input goes positive Q_1 conducts heavily acting as closed switch while Q_2 is OFF. While when input goes negative, Q_2 conducts heavily acting as closed switch while Q_1 is OFF. Thus the load voltage V_o across R_L has one of two possible values which are V_{supply} or 0 V. This is a type of digital output having two levels high and low.

The transistors dissipate almost zero power as in any of the states, either voltage is zero or current is zero for the transistors. Thus entire power input is available to the load. **Hence efficiency of class D amplifiers is almost 100 %.** The figure of merit which is the ratio of the maximum power dissipated in transistor to that delivered to the load, is zero. These facts make the class D amplifier as an ideal amplifier.

Practically class D amplifiers are designed to operate with digital or pulse type of signals. The basic block diagram of unit used along with class D amplifier in the application circuits is shown in the Fig. 6.12.

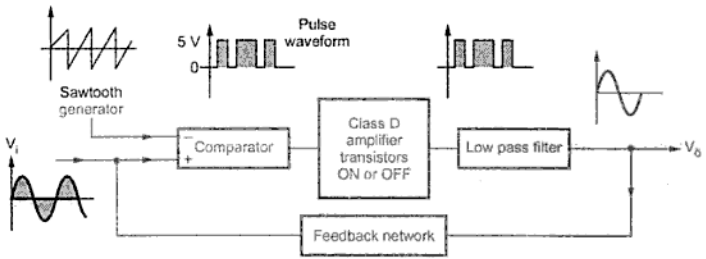


Fig. 6.12 Block diagram of class D amplifier

The op-amp comparator is used for which one input is sawtooth type while other is sinusoidal. The comparator converts sinusoidal signal to digital pulse type signal with the help of sawtooth waveform. This is called chopping of sinusoidal signal to produce digital signal. This signal drives the class D smplifier. When pulse signal is high the transistors are ON and when it is low, the transistors are OFF. Thus most of the power supplied is delivered to the load by producing high power output signal. The digital signal is converted back to the original sinusoidal signal using low pass filter. Using feedback network, it is fed back to the comparator. Practically instead of power BJT, power MOSFET devices are used as driver devices for class D amplifier.

The class D amplifiers are mainly used in the pulse and digital circuits.

6.5 Comparison of Amplifier Classes

The comparison of various amplifier classes is summarized in Table 6.1.

Class	A	B	C	AB
Operating cycle	360°	180°	Less than 180°	180° to 360°
Position of Q point	Centre of load line	On X-axis	Below X-axis	Above X-axis but below the centre of load line
Efficiency	Poor, 25 % to 50 %	Better, 78.5 %	High	Higher than A but less than B 50 % to 78.5 %
Distortion	Absent No distortion	Present More than class A	Highest	Present

Table 6.1

Key Point : *It is important to note that class C operation is never used for audio frequency amplifiers.*

The class C is used in special areas of tuned circuits, such as radio or communications.

6.6 Analysis of Class A Amplifiers

The class A amplifiers are further classified as **directly coupled** and **transformer coupled** amplifiers. In directly coupled type, the load is directly connected in the collector circuit. While in the transformer coupled type, the load is coupled to the collector using a transformer called an output transformer. Let us study in detail the various aspects of the two types of class A amplifiers.

6.7 Series Fed, Directly Coupled Class A Amplifier

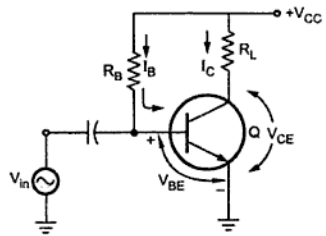


Fig. 6.13 Large signal class A amplifier

A simple fixed-bias circuit can be used as a large signal class A amplifier as shown in the Fig. 6.13.

The difference between small signal version of this circuit is that the signals handled by this large signal circuit are of the order of few volts. Similarly the transistor used, is a power transistor. The value of R_B is selected in such a way that the Q point lies at the centre of the d.c. load line.

The circuit represents the directly coupled class A amplifier as the load resistance is directly connected in the collector

circuit. Most of the times the load is a loudspeaker, the impedance of which varies from 3 to 4 ohms to 16 ohms. The beta of the transistor used is less than 100.

Key Point : *This is called directly coupled, as the load R_L is directly connected in the collector circuit of power transistor.*

The overall circuit handles large power, in the range of a few to tens of watts without providing much voltage gain.

The graphical representation of a class A amplifier is shown in the Fig. 6.14.

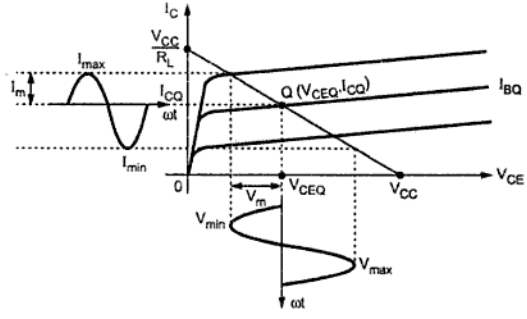


Fig. 6.14 Graphical representation of class A amplifier

Applying Kirchhoff's voltage law to the circuit shown in the Fig. 6.13, we get

$$V_{CC} = I_C R_L + V_{CE}$$

$$\therefore \quad I_C R_L = -V_{CE} + V_{CC}$$

$$\therefore \quad I_C = \left[-\frac{1}{R_L}\right] V_{CE} + \frac{V_{CC}}{R_L} \qquad \ldots (1)$$

The equation is similar to equation (1) of section 6.3 and thus the slope of the load line is $-\frac{1}{R_L}$ while the Y-intercept is $\frac{V_{CC}}{R_L}$.

The change is because the collector resistance R_C is named as load resistance R_L in this circuit. The Q point is adjusted approximately at the centre of the load line.

6.7.1 D.C. Operation

The collector supply voltage V_{CC} and resistance R_B decides the d.c. base-bias current I_{BQ}. The expression is obtained applying KVL to the B-E loop and with $V_{BE} = 0.7$ V.

$$\therefore \quad \boxed{I_{BQ} = \frac{V_{CC} - 0.7}{R_B}} \qquad \ldots (2)$$

The corresponding collector current is then,

$$\boxed{I_{CQ} = \beta I_{BQ}} \qquad \ldots (3)$$

From the equation (1), the corresponding collector to emitter voltage is,

$$\boxed{V_{CEQ} = V_{CC} - I_{CQ} R_L} \qquad \ldots (4)$$

Hence the Q point can be defined as Q (V_{CEQ}, I_{CQ}).

6.7.2 D.C. Power Input

The d.c. power input is provided by the supply. With no a.c input signal, the d.c. current drawn is the collector bias current I_{CQ} . Hence d.c. power input is,

$$\boxed{P_{DC} = V_{CC} \cdot I_{CQ}} \qquad \ldots (5)$$

It is important to note that even if a.c. input signal is applied, the average current drawn from the d.c. supply remains same. Hence equation (5) represents d.c. power input to the class A series fed amplifier.

6.7.3 A.C. Operation

When an input a.c. signal is applied, the base current varies sinusoidally.

Assuming that the nonlinear distortion is absent, the nature of the collector current and collector to emitter voltage also vary sinusoidally as shown graphically in the Fig. 5.14.

The output current i.e. collector current varies around its quiescent value while the output voltage i.e collector to emitter voltage varies around its quiescent value. The varying output voltage and output current deliver an a.c. power to the load. Let us find the expressions for the a.c. power delivered to the load.

6.7.4 A.C. Power Output

For an alternating output voltage and output current swings, shown in the Fig. 6.14, we can write,

V_{min} = Minimum instantaneous value of the collector (output) voltage

V_{max} = Maximum instantaneous value of the collector (output) voltage

and V_{pp} = Peak to peak value of a.c. output voltage across the load.

$$\therefore \quad V_{pp} = V_{max} - V_{min} \qquad \ldots (6)$$

Now V_m = Amplitude (peak) of a.c. output voltage as shown in the Fig. 6.14.

$$\therefore \quad \boxed{V_m = \frac{V_{pp}}{2} = \frac{V_{max} - V_{min}}{2}} \quad \ldots (7)$$

Similarly we can write for the output current as,

I_{min} = Minimum instantaneous value of the collector (output) current

I_{max} = Maximum instantaneous value of the collector (output) current

and I_{pp} = Peak to peak value of a.c. output (load) current.

$$\therefore \quad I_{pp} = I_{max} - I_{min} \quad \ldots (8)$$

Now I_m = Amplitude (peak) of a.c. output (load) current as shown in the Fig. 6.14

$$\therefore \quad \boxed{I_m = \frac{I_{pp}}{2} = \frac{I_{max} - I_{min}}{2}} \quad \ldots (9)$$

Hence the r.m.s. values of alternating output voltage and current can be obtained as,

$$V_{rms} = \frac{V_m}{\sqrt{2}} \quad \ldots (10)$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \ldots (11)$$

Hence we can write,

$$V_{rms} = I_{rms} \; R_L \quad \ldots (12)$$

i.e. $$V_m = I_m R_L \quad \ldots (13)$$

The a.c. power delivered by the amplifier to the load can be expressed by using r.m.s values, maximum i.e. peak values and peak to peak values of output voltage and current.

i) Using r.m.s values

$$\therefore \quad \boxed{P_{ac} = V_{rms} \; I_{rms}} \quad \ldots (14)$$

or $$P_{ac} = I_{rms}^2 \; R_L \quad \ldots (15)$$

or $$\boxed{P_{ac} = \frac{V_{rms}^2}{R_L}} \quad \ldots (16)$$

ii) Using peak values

$$P_{ac} = V_{rms} \; I_{rms} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}$$

$$\therefore \quad \boxed{P_{ac} = \frac{V_m \; I_m}{2}} \quad \ldots (17)$$

or $$\boxed{P_{ac} = \frac{I_m^2 \; R_L}{2}} \quad \ldots (18)$$

or $$\boxed{P_{ac} = \frac{V_m^2}{2 R_L}} \quad \ldots (19)$$

iii) Using peak to peak values

$$P_{ac} = \frac{V_m I_m}{2} = \frac{\left(\frac{V_{PP}}{2}\right)\left(\frac{I_{PP}}{2}\right)}{2}$$

$$\boxed{P_{ac} = \frac{V_{pp} I_{pp}}{8}} \quad \ldots (20)$$

or $$\boxed{P_{ac} = \frac{I_{pp}^2 R_L}{8}} \quad \ldots (21)$$

or $$\boxed{P_{ac} = \frac{V_{PP}^2}{8 R_L}} \quad \ldots (22)$$

But as $V_{pp} = V_{max} - V_{min}$ and $I_{pp} = I_{max} - I_{min}$; from equation (20), the a.c. power can be expressed as below, for graphical calculations.

$$\boxed{P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}} \quad \ldots (23)$$

6.7.5 Efficiency

The efficiency of an amplifier represents the amount of a.c. power delivered or transferred to the load, from the d.c. source i.e. accepting the d.c. power input. The generalised expression for an efficiency of an amplifier is,

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 \quad \ldots (24)$$

Now for class A operation, we have derived the expressions for P_{ac} and P_{dc}, hence using equations (5) and (23), we can write

$$\boxed{\% \eta = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} I_{CQ}} \times 100} \quad \ldots (25)$$

The efficiency is also called **conversion efficiency** of an amplifier.

6.7.6 Maximum Efficiency

For maximum efficiency calculation, assume maximum swings of both the output voltage and the output current. The maximum swings are shown in the Fig. 6.15.

From the Fig. 6.15, we can see that the minimum voltage possible is zero and maximum voltage possible is V_{CC}, for a maximum swing. Similarly the minimum current is zero and the maximum current possible is $2 I_{CQ}$, for a maximum swing.

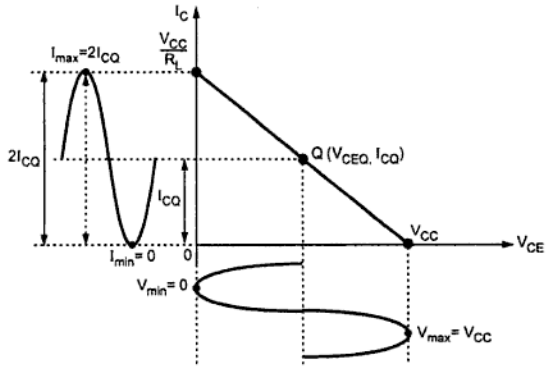


Fig. 6.15 Maximum voltage and current swings

$$\left.\begin{array}{l} V_{max} = V_{CC} \text{ and } V_{min} = 0 \\ I_{max} = 2\,I_{CQ} \text{ and } I_{min} = 0 \end{array}\right\} \text{ for maximum swing}$$

Using equation (25) we can write,

$$\%\,\eta_{max} = \frac{(V_{CC}-0)(2I_{CQ}-0)}{8\,V_{CC}\,I_{CQ}} \times 100 = \frac{2\,V_{CC}\,I_{CQ}}{8\,V_{CC}\,I_{CQ}} \times 100$$

$$= 25\ \%$$

Key Point : ***Thus the maximum efficiency possible in case of directly coupled series fed class A amplifier is just 25 %.***

This maximum efficiency is an ideal value. For a practical circuit, it is much less than 25 %, of the order of 10 to 15 %.

Key Point : ***Very low efficiency is the biggest disadvantage of class A amplifier.***

6.7.7 Power Dissipation

As stated earlier, power dissipation in large signal amplifier is also large. The amount of power that must be dissipated by the transistor is the difference between the d.c. power input P_{dc} and the a.c. power delivered to the load P_{ac}.

P_d = Power dissipation

i.e. $\boxed{P_d = P_{DC} - P_{ac}}$ ... (26)

The maximum power dissipation occurs when there is zero a.c. input signal. When a.c. input is zero, the a.c. power output is also zero. But transistor operates at quiescent condition, drawing d.c. input power from the supply equal to $V_{CC}\ I_{CQ}$. This entire power gets dissipated in the form of heat. Thus d.c. power input without a.c. input signal is the maximum power dissipation.

$$\boxed{(P_d)max = V_{CC}\ I_{CQ}} \quad \text{... (27)}$$

Key Point : *Thus value of maximum power dissipation decides the maximum power dissipation rating of the transistor to be selected for the amplifier.*

6.7.8 Advantages and Disadvantages

The **advantages** of directly coupled class A amplifier can be stated as,

1. The circuit is simple to design and to implement.
2. The load is connected directly in the collector circuit hence the output transformer is not necessary. This makes the circuit cheaper.
3. Less number of components required as load is directly coupled.

The **disadvantages** are,

1. The load resistance is directly connected in collector and carries the quiescent collector current. This causes considerable wastage of power.
2. Power dissipation is more. Hence power dissipation arrangements like heat sink are essential.
3. The output impedance is high hence circuit cannot be used for low impedance loads, such as loudspeakers.
4. The efficiency is very poor, due to large power dissipation.

Example 6.1 : *A series fed class A amplifier shown in Fig. 6.16, operates from d.c. source and applied sinusoidal input signal generates peak base current 9 mA. Calculate :*

i) Quiescent current I_{CQ}

ii) Quiescent voltage V_{CEQ}

iii) D.C. input power P_{DC}

iv) A.C. output power P_{ac}

v) Efficiency.

Assume $\beta = 50$ *and* $V_{BE} = 0.7$ *V.*

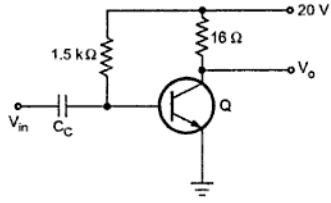


Fig. 6.16

Solution :

i) I_{CQ} $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{20 - 0.7}{1.5 \times 10^3} = 12.87$ mA

$I_{CQ} = \beta \times I_{BQ} = 50 \times 12.87 =$ **643.50 mA**

ii) V_{CEQ} $V_{CC} = I_{CQ} R_L + V_{CEQ}$

$\therefore$ $V_{CEQ} = V_{CC} - I_{CQ} R_L = 20 - 643.50 \times 10^{-3} \times 16 =$ **9.70 volts**

iii) P_{DC} $P_{DC} = V_{CC} \times I_{CQ} = 20 \times 643.5 \times 10^{-3} =$ **12.87 watt**

iv) P_{ac} Peak current $i_b = 9$ mA

$i_c = \beta i_b = 50 \times 9 = 450$ mA (peak)

$\therefore$ $i_{c(rms)} = \frac{i_{c(peak)}}{\sqrt{2}} = \frac{450}{\sqrt{2}} = 318.19$ mA $= I_{rms}$

$\therefore$ $P_{ac} = I_{rms}^2 R_L = (318.19 \times 10^{-3})^2 \times 16 =$ **1.619 watt**

v) Efficiency $\eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{1.619}{12.87} \times 100 =$ **12.58 %**

6.8 Transformer Coupled Class A Amplifier

As stated earlier, for maximum power transfer to the load, the impedance matching is necessary. For loads like loudspeaker, having low impedance values, impedance matching is difficult using directly coupled amplifier circuit. This is because loudspeaker resistance is in the range of 3 to 4 ohms to 16 ohms while the output impedance of series fed directly coupled class A amplifier is very much high. This problem can be eliminated by using a transformer to deliver power to the load.

Key Point : *The transformer is called an **output transformer** and the amplifier is called **transformer coupled class A amplifier.***

Before studying the operation of the amplifier, let us revise few concepts regarding the transformer.

6.8.1 Properties of Transformer

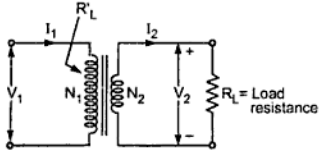


Fig. 6.17 Transformer with load

Consider a transformer as shown in the Fig. 6.17 which is connected to a load of resistance R_L.

While analysing the transformer, it is assumed that the transformer is ideal and there are no losses in the transformer. Similarly the winding resistances are assumed to be zero.

Let
N_1 = Number of turns on primary
N_2 = Number of turns on secondary
V_1 = Voltage applied to primary
V_2 = Voltage on secondary
I_2 = Primary current

i) Turns Ratio : The ratio of number of turns on secondary to the number of turns on primary is called turns ratio of the transformer denoted by n.

$$\therefore \quad \boxed{n = \text{Turns ratio} = \frac{N_2}{N_1}} \qquad \ldots (1)$$

Some times it is specified as $\frac{N_2}{N_1} : 1$ or $\frac{N_1}{N_2} : 1$.

ii) Voltage Transformation : The transformer transforms the voltage applied on one side to other side proportional to the turns ratio. The transformer can be step up or step down transformer.

$$\therefore \quad \frac{V_2}{V_1} = \frac{N_2}{N_1} = n \qquad \ldots (2)$$

In the amplifier analysis, the load impedance is going to be small. And the transformer is to be used for impedance matching. Hence it has to be a step down transformer. Hence

Example 6.2 : *The load of 4 Ω is connected to the secondary of a transformer having primary turns of 200 and the secondary turns of 20. Calculate the reflected load impedance on primary.*

Solution : $R_L = 4\ \Omega$, $N_1 = 200$, $N_2 = 20$

$$\therefore \quad n = \frac{N_2}{N_1} = \frac{20}{200} = 0.1$$

$$\therefore \quad R_L' = \frac{R_L}{n^2} = \frac{4}{(0.1)^2} = 400\ \Omega$$

As $N_2 < N_1$, the transformer is step down and hence $R_L' > R_L$, as the primary winding is high voltage winding.

Example 6.3 : *For a transformer, the load connected to the secondary has an impedance of 8 Ω. Its reflected impedance on primary is observed to be 648 Ω. Calculate the turns ratio.*

Solution : $R_L = 8\ \Omega$, $R_L' = 648\ \Omega$

Now $$R_L' = \frac{R_L}{n^2}$$

$$\therefore \quad n^2 = \frac{R_L}{R_L'} = \frac{8}{648} = 0.01234$$

$$\therefore \quad n = 0.1111 = \text{Turns ratio}$$

But $$n = \frac{N_2}{N_1} = 0.1111$$

$$\therefore \quad \frac{N_1}{N_2} = 9$$

Generally the turns ratio is specified as $\frac{N_1}{N_2}$: 1 i.e. for this transformer it is 9 : 1.

Key Point : *For all the calculations, we will use the turns ratio as $n = N_2/N_1$. Only for specifying the turns ratio, the method of specification is used as (N_1 / N_2) : 1. e.g. if the transformer turns ratio is given as 10 : 1 then for the calculation purpose we will consider the turns ratio as,*

$$n = \frac{N_2}{N_1} = \frac{1}{10} = 0.1.$$

6.8.2 Circuit Diagram of Transformer Coupled Amplifier

The basic circuit of a transformer coupled amplifier is shown in the Fig. 6.18. The loudspeaker connected to the secondary acts as a load having impedance of R_L ohms.

The transformer used is a step down transformer with the turns ratio as

$$\boxed{n = N_2/N_1}$$

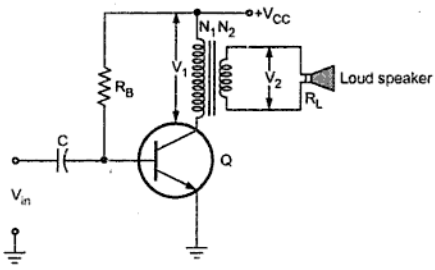


Fig. 6.18 Transformer coupled class A amplifier

6.8.3 D.C. Operation

It is assumed that the winding resistances are zero ohms. Hence for d.c. purposes, the resistance is 0 Ω. There is no d.c. voltage drop across the primary winding of the transformer. The slope of the d.c. load line is reciprocal of the d.c. resistance in the collector circuit, which is zero in this case. Hence slope of the d.c. load line is ideally infinite. This tells that the d.c. load line in the ideal condition is a vertically straight line.

Applying Kirchhoff's voltage law to the collector circuit we get,

$$V_{CC} - V_{CE} = 0$$

i.e. $V_{CC} = V_{CE}$ ... Drop across winding is zero

This is the d.c. bias voltage V_{CEQ} for the transistor.

So $$\boxed{V_{CEQ} = V_{CC}} \quad \text{... (5)}$$

Hence the d.c. load line is a vertical straight line passing through a voltage point on the X-axis which is $V_{CEQ} = V_{CC}$.

The intersection of d.c. load line and the base current set by the circuit is the quiescent operating point of the circuit. The corresponding collector current is I_{CQ}.

The d.c. load line is shown in the Fig. 6.19.

6.8.4 D.C Power Input

The d.c. power input is provided by the supply voltage with no signal input, the d.c. current drawn is the collector bias current I_{CQ}.

Hence the d.c. power input is given by,

So $$\boxed{P_{DC} = V_{CC}\, I_{CQ}} \quad \text{... (6)}$$

The expression is same as derived earlier for series fed directly coupled class A amplifier.

6.8.5 A.C. Operation

For the a.c. analysis, it is necessary to draw an a.c. load line on the output characteristics.

For a.c. purposes, the load on the secondary is the load impedance R_L ohms. And the reflected load on the primary i.e. R'_L can be calculated using the equation (4). The load line drawn with a slope of $\left(\frac{-1}{R'_L}\right)$ and passing through the operating point i.e. quiescent point Q is called **a.c. load line**. The d.c. and a.c. load lines are shown in the Fig. 6.19.

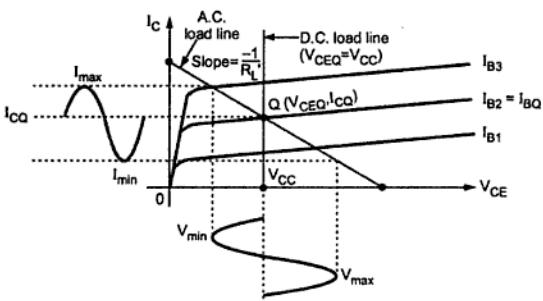


Fig. 6.19 Load lines for transformer coupled class A amplifier

The output current i.e. collector current varies around its quiescent value I_{CQ}, when a.c. input signal is applied to the amplifier. The corresponding output voltage also varies sinusoidally around its quiescent value V_{CEQ} which is V_{CC} in this case.

6.8.6 A.C. Output Power

The a.c. power developed is on the primary side of the transformer. While calculating this power, the primary values of voltage and current and reflected load R'_L must be considered. The a.c. power delivered to the load is on the secondary side of the transformer. While calculating load voltage, load current, load power the secondary voltage, current and the load R_L must be considered.

The slope of the a.c. load line can be expressed interms of the primary current and the primary voltage.

The slope of the a.c. load line is,

$$= \frac{1}{R'_L} = \frac{I_{lm}}{V_{lm}} \quad \ldots (15)$$

The generalised expression for a.c. power output represented by the equation (24) in section (6.7), can be used as it is for transformer coupled amplifier. The expression is mentioned again for the convenience of the reader.

$$\therefore \quad \boxed{P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}} \quad \ldots (16)$$

Key Point : *The a.c. power calculated is the power developed across the primary winding of the output transformer. Assuming ideal transformer, the power delivered to the load on secondary, is same as that developed across the primary. If the transformer efficiency is known, the power delivered to the load must be calculated from the power developed on the primary, considering the efficiency of the transformer.*

6.8.7 Efficiency

The general expression for the efficiency remains same as that given by equations (24) and (25) in section 6.7.

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} I_{CQ}} \times 100$$

6.8.8 Maximum Efficiency

Assume maximum swings of both the output voltage and output current, to calculate maximum efficiency, as shown in the Fig. 6.20.

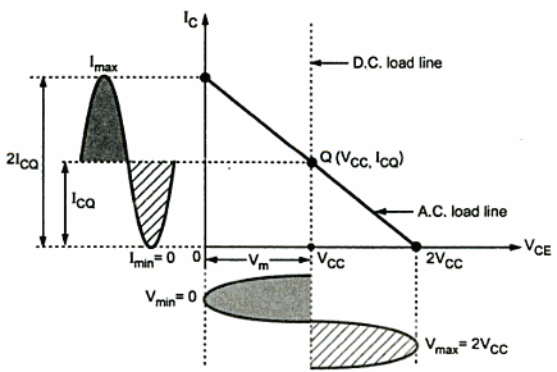


Fig. 6.20 Maximum voltage and current swings

6.8.9 Power Dissipation

The power dissipation by the transistor is the difference between the a.c. power output and the d.c. power input. The power dissipated by the transformer is very small due to negligible (d.c.) winding resistances and can be neglected.

$$\therefore \quad P_d = P_{DC} - P_{ac} \quad \ldots (18)$$

When the input signal is larger, more power is delivered to the load and less is the power dissipation. But when there is no input signal, the entire d.c. input power gets dissipated in the form of heat, which is the maximum power dissipation.

$$\therefore \quad \boxed{(P_d)_{max} = V_{CC} I_{CQ}} \quad \ldots (19)$$

Thus the class A amplifier dissipates less power when delivers maximum power to the load. While it dissipates maximum power while delivering zero power to the load i.e. when load is removed and there is no a.c. input signal. The maximum power dissipation decides the maximum power dissipation rating for the power transistor to be selected for an amplifier.

6.8.10 Advantages and Disadvantages

The **advantages** of transformer coupled class **A amplifier** circuit are,

1. The efficiency of the operation is higher than directly coupled amplifier.
2. The d.c. bias current that flows through the load in case of directly coupled amplifier is stopped in case of transformer coupled.
3. The impedance matching required for maximum power transfer is possible.

The **disadvantages** are,

1. Due to the transformer, the circuit becomes bulkier, heavier and costlier compared to directly coupled circuit.
2. The circuit is complicated to design and implement compared to directly coupled circuit.
3. The frequency response of the circuit is poor.

Example 6.4 : *The loudspeaker of 8 Ω is connected to the secondary of the output transformer of a class A amplifier circuit. The quiescent collector current is 140 mA. The turns ratio of the transformer is 3:1. The collector supply voltage is 10 V. If a.c. power delivered to the loudspeaker is 0.48 W, assuming ideal transformer, calculate :*

1. *A.C. power developed across primary*
2. *R.M.S. value of load voltage*
3. *R.M.S. value of primary voltage*
4. *R.M.S. value of load current*

3. The r.m.s value of the primary voltage is $(V_1)_{rms}$ as calculated above.

$\therefore \quad (V_1)_{rms} = \mathbf{5.8787\ V}$

4. The power delivered to the load $= I_{2rms}^2 \times R_L$ ... Refer equation 13.

$\therefore \quad 0.48 = I_{2rms}^2 \times 8$

$\therefore \quad I_{2rms}^2 = 0.06$

$\therefore \quad I_{2rms} = \mathbf{0.2449\ A}$

This is the r.m.s value of the load current as the resistance value used is R_L and not R_L'.

5. The r.m.s values of primary and secondary are related through the transformation ratio.

$$\therefore \quad \frac{(I_1)_{rms}}{(I_2)_{rms}} = \frac{N_2}{N_1} = n = 0.333$$

$$\therefore \quad (I_1)_{rms} = (I_2)_{rms} \times n = 0.2449 \times 0.333 = 0.0816A = \mathbf{81.64\ mA}.$$

6. The d.c. power input is,

$$P_{DC} = V_{CC}\ I_{CQ} = 10 \times 140 \times 10^{-3} = \mathbf{1.4\ W}$$

7. $$\%\,\eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{0.48}{1.4} \times 100 = \mathbf{34.28\%}$$

8. $$P_d = P_{DC} - P_{ac} = 1.4 - 0.48 = \mathbf{0.92\ W}$$

This is the power dissipation.

6.9 Distortion in Amplifiers

The input signal applied to the amplifiers is alternating in nature. The basic features of any alternating signal are amplitude, frequency and phase. The amplifier output should be reproduced faithfully i.e. there should not be the change or distortion in the amplitude, frequency and phase of the signal. Hence the possible distortions in any amplifier are amplitude distortion, phase distortions and frequency distortion. But the phase distortions are not detectable by human ears as human ears are insensitive to the phase changes. While **the change in gain of the amplifier with respect to the frequency is called frequency distortion.**

Key Point : *The frequency distortion is not significant in A.F. power amplifiers.*

In the earlier discussion, it is assumed that the transistor is perfectly linear device. That is the dynamic characteristics of a transistor is a straight line over the operating range [$i_c = Ki_b$]. But in practical circuits, the dynamic characteristics is not perfectly linear. Due to such non-linearity in the dynamic characteristics, the waveform of the output voltage

differs from that of the input signal. Such a distortion is called nonlinear distortion or **amplitude distortion** or **harmonic distortion.**

Key Point : *The harmonic distortion plays an important role in the analysis of A.F. power amplifiers.*

Let us see, what is the exact meaning of harmonic distortion and how it affects the waveform of the output signal.

6.9.1 Harmonic Distortion

The harmonic distortion means the presence of the frequency components in the output waveform, which are not present in the input signal. The component with frequency same as the input signal is called fundamental frequency component. The additional frequency components present in the output signal are having frequency components which are integer multiples of fundamental frequency component. These components are called harmonic components or harmonics. For example if the **fundamental frequency** is f Hz, then the output signal contains fundamental frequency component at f Hz and additional frequency components at 2f Hz, 3f Hz, 4f Hz and so on. The 2f component is called **second harmonic,** the 3f component is called third harmonic and so on. The fundamental frequency component is not considered as a harmonic. Out of all the harmonic components, the second harmonic has the largest amplitude.

Key Point : *As the order of the harmonic increases, its amplitude decreases.*

As the second harmonic amplitude is largest, the second harmonic distortion is more important in the analysis of A.F. power amplifiers. The Fig. 6.21 shows the various harmonic components.

It can be seen from the Fig. 6.21 that the distorted waveform can be obtained by adding the fundamental and the harmonic components. The percentage harmonic distortion due to each order (2^{nd}, 3^{rd} and so on) can be calculated by comparing the amplitude of each order of harmonic with the amplitude of the fundamental frequency component.

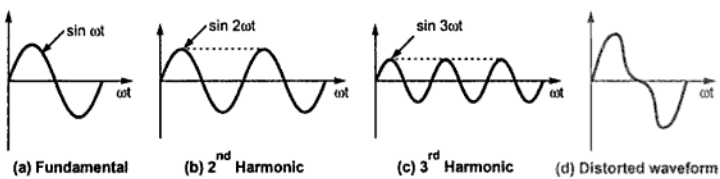


Fig. 6.21 Distortion due to harmonic components

If the fundamental frequency component has an amplitude of B_1 and the n^{th} harmonic component has an amplitude of B_n then the percentage harmonic distortion due to n^{th} harmonic component is expressed as,

$$\% \, n^{th} \text{ harmonic distortion} = \% \, D_n = \frac{|B_n|}{|B_1|} \times 100 \quad \ldots (1)$$

So $$\% \, D_2 = \frac{|B_2|}{|B_1|}, \% \, D_3 = \frac{|B_3|}{|B_1|} \text{ and so on.}$$

6.9.2 Total Harmonic Distortion

When the output signal gets distorted due to various harmonic distortion components, the total harmonic distortion, which is the effective distortion due to all the individual components is given by

$$\% \, D = \sqrt{D_2^2 + D_3^2 + D_4^2 + \ldots} \times 100 \quad \ldots (2)$$

where D = Total harmonic distortion

As stated earlier, the most important component in the distortion is the second harmonic distortion. Let us discuss the graphical method of calculating second harmonic distortion.

6.9.3 Second Harmonic Distortion (Three Point Method)

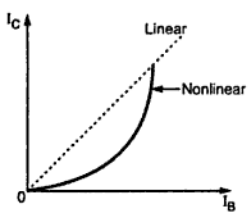


Fig. 6.22 Nonlinear dynamic characteristics

To investigate the second harmonic distortion, assume that the dynamic transfer characteristics of the transistor is parabolic (nonlinear) in nature rather than a straight line (linear) as shown in the Fig. 6.22.

As discussed earlier such type of nonlinearity introduces harmonic distortion, in which second harmonic distortion is the most dominant.

Let an a.c. input signal, causes the base current swing which is cosine in nature

$$\therefore \quad i_b = I_{Bm} \cos \omega t \quad \ldots (3)$$

Due to this, collector current swings around its quiescent value but the relation between i_b and i_c is nonlinear as shown in the Fig. 6.22.

Mathematically this can be expressed as,

$$i_c = G_1 \, i_b + G_2 \, i_b^2$$

$$= G_1 \, I_{Bm} \cos \omega t + G_2 \, I_{Bm}^2 \cos^2 \omega t \quad \ldots (4)$$

But $\cos^2 \omega t = \frac{1 + \cos 2\omega t}{2}$

Substituting in equation (4),

$$i_c = G_1 I_{Bm} \cos \omega t + G_2 I_{Bm}^2 \left(\frac{1 + \cos 2\omega t}{2} \right)$$

$$\therefore \quad i_c = G_1 I_{Bm} \cos \omega t + \frac{1}{2} G_2 I_{Bm}^2 + \frac{G_2}{2} I_{Bm}^2 \cos 2\omega t$$

$$\therefore \quad \boxed{i_c = B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t} \qquad \ldots (5)$$

The last term represents the second harmonic component. Thus the equation shows that, there is second harmonic component present.

Hence the total collector current waveform can be shown as in the Fig. 6.23, which is swinging about its quiescent value I_{CQ}.

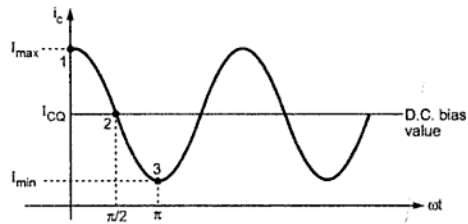


Fig. 6.23 Output current waveform

Hence the total collector current can be expressed in terms of its d.c. bias value, d.c. signal component, fundamental frequency and second harmonic component as,

$$\boxed{i_c = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t} \qquad \ldots (6)$$

where $(I_{CQ} + B_0)$ = The d.c. component, independent of time.

B_1 = Amplitude of the fundamental frequency.

B_2 = Amplitude of the second harmonic component.

It can be seen that due to the presence of harmonics, the d.c. current increases.

Practically the presence of harmonics can be detected by connecting milliammeter in the collector circuit. The readings can be observed without an a.c. input signal and with a.c. input signal. If the two readings are almost same there are no harmonics present. But if milliammeter shows an increase in the current, when an a.c. input is applied, then the harmonics can be concluded to be present in the output signal.

Let us find out the value of the total collector current at the various instants 1, 2 and 3, shown in the Fig. 6.23.

At point 1, $\omega t = 0$, substituting in equation (6) we get,

$$\therefore \quad i_c = I_{CQ} + B_0 + B_1 + B_2 \qquad \ldots (7)$$

At point 2, $\omega t = \frac{\pi}{2}$,

$$\therefore \quad i_c = I_{CQ} + B_0 - B_2 \qquad \ldots (8)$$

At point 3, $\omega t = \pi$,

$$\therefore \quad i_c = I_{CQ} + B_0 - B_1 + B_2 \qquad \ldots (9)$$

But at $\omega t = 0$, $i_c = I_{max}$

At $\omega t = \frac{\pi}{2}$, $i_c = I_{CQ}$

At $\omega t = \pi$, $i_c = I_{min}$

Hence the equations get modified as,

$$I_{max} = I_{CQ} + B_0 + B_1 + B_2 \qquad \ldots (10)$$

$$I_{CQ} = I_{CQ} + B_0 - B_2 \qquad \ldots (11)$$

$$I_{min} = I_{CQ} + B_0 - B_1 + B_2 \qquad \ldots (12)$$

From equation (11),

$$\boxed{B_0 = B_2} \qquad \ldots (13)$$

Now $I_{max} - I_{min} = 2B_1$

$$\therefore \quad \boxed{B_1 = \frac{I_{max} - I_{min}}{2}} \qquad \ldots (14)$$

$$I_{max} + I_{min} = 2I_{CQ} + 2B_0 + 2B_2$$
$$= 2I_{CQ} + 2B_2 + 2B_2 \qquad \ldots \text{As } B_0 = B_2$$
$$= 2I_{CQ} + 4B_2$$

$$\therefore \quad \boxed{B_2 = \frac{I_{max} + I_{min} - 2I_{CQ}}{4}} \qquad \ldots (15)$$

As the amplitudes of the fundamental and second harmonic are known, the second harmonic distortion can be calculated as,

$$\% D_2 = \frac{|B_2|}{|B_1|} \times 100 \qquad \ldots (16)$$

As the method uses three points on the collector current waveform to obtain the amplitudes of the harmonics, the method is called **'Three Point Method'** of determining the second harmonic distortion.

6.9.4 Power Output Due to Distortion

When the distortion is negligible, the power delivered to the load is given by,

$$P_{ac} = \frac{I_m^2 R_L}{2} \quad \text{... Refer equation (18) in section 6.7}$$

But I_m = Peak value of the output current

$$= \frac{I_{pp}}{2} = \frac{I_{max} - I_{min}}{2} \quad \text{... Refer equation (9) in section 6.7}$$

But $$B_1 = \frac{I_{max} - I_{min}}{2}$$

$\therefore$ $I_m = B_1$ = Fundamental frequency component

$\therefore$ $$P_{ac} = \frac{1}{2} B_1^2 R_L \quad \text{... (17)}$$

With distortion, the power delivered to the load increases proportional to the amplitude of the harmonic component.

$\therefore$ $(P_{ac})_D$ = A.C. power output with harmonic distortion

$$= \frac{1}{2} B_1^2 R_L + \frac{1}{2} B_2^2 R_L + \frac{1}{2} B_3^2 R_L + \cdots$$

$\therefore$ $$(P_{ac})_D = \frac{1}{2} B_1^2 R_L \left(1 + \frac{B_2^2}{B_1^2} + \frac{B_3^2}{B_1^2} + \cdots\right)$$

$\therefore$ $$\boxed{(P_{ac})_D = \frac{1}{2} B_1^2 R_L (1 + D_2^2 + D_3^2 + \cdots)}$$

$\therefore$ $$\boxed{(P_{ac})_D = P_{ac}[1 + D^2]} \quad \text{... } D^2 = D_2^2 + D_3^2 + \cdots \quad \text{... (18)}$$

This is the power delivered to the load due to the harmonic distortion.

6.9.5 Higher Order Harmonic Distortion (Five Point Method)

As the nonlinearity present in dynamic characteristics increases, the order of the harmonic distortion also increases.

Let the mathematical expression for the collector current due to higher order harmonics be,

$$i_c = G_1 i_b + G_2 i_b^2 + G_3 i_b^3 + G_4 i_b^4 \quad \text{... (19)}$$

Substituting the input signal $i_b = I_{Bm} \cos \omega t$ we get,

$i_c = G_1 I_{Bm} \cos \omega t + G_2 I_{Bm} \cos^2 \omega t + G_3 I_{Bm} \cos^3 \omega t + G_4 I_{Bm} \cos^4 \omega t$

Substituting $\cos^2 \omega t$, $\cos^3 \omega t$ and $\cos^4 \omega t$ and doing trigonometric operations, we get,

$$i_c = B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + B_4 \cos 4\omega t \quad \ldots (20)$$

The equation shows that there are harmonics upto 4^{th} order. The collector current waveform and the various instants to be considered for higher order harmonic distortion calculation, are shown in the Fig. 6.24.

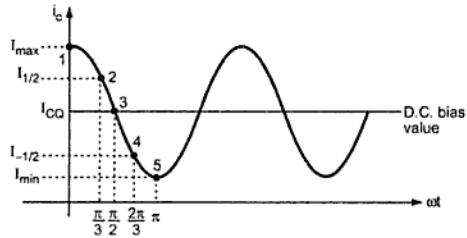


Fig. 6.24 Output current waveform

The total collector current including d.c. bias can be written as,

$$i_c = I_{CQ} + B_0 + B_1 \cos \omega t + B_2 \cos 2\omega t + B_3 \cos 3\omega t + B_4 \cos 4\omega t \quad \ldots (21)$$

where $(I_{CQ} + B_0)$ is the d.c. component.

B_1, B_2 , B_3 and B_4 are the amplitudes of the fundamental component, second, third and fourth harmonic components respectively.

Consider the five instants as shown in the Fig. 6.24 .

At point 1, $\omega t = 0$, $i_c = I_{max}$

$$\therefore \quad I_{max} = I_{CQ} + B_0 + B_1 + B_2 + B_3 + B_4 \quad \ldots (22)$$

At point 2, $\omega t = \pi/3$, $i_c = I_{1/2}$

$$\therefore \quad I_{1/2} = I_{CQ} + B_0 + 0.5B_1 - 0.5B_2 - B_3 - 0.5B_4 \quad \ldots (23)$$

At point 3, $\omega t = \frac{\pi}{2}$, $i_c = I_{CQ}$

$$\therefore \quad I_{CQ} = I_{CQ} + B_0 - B_2 + B_4 \quad \ldots (24)$$

At point 4, $\omega t = \frac{2\pi}{3}$, $i_c = I_{-1/2}$

$$\therefore \quad I_{-1/2} = I_{CQ} + B_0 - 0.5B_1 - 0.5B_2 + B_3 - 0.5B_4 \quad \ldots (25)$$

At point 5, $\omega t = \pi$, $i_c = I_{min}$

$$\therefore \quad I_{min} = I_{CQ} + B_0 - B_1 + B_2 - B_3 + B_4 \quad \ldots (26)$$

Solving the above five equations from (21) to (26) simultaneously, for the values of B_0, B_1, B_2, B_3 and B_4 we get,

$$B_0 = \frac{1}{6}[I_{max} + 2\, I_{\frac{1}{2}} + 2\, I_{-\frac{1}{2}} + I_{min}] \quad \text{... (27)}$$

$$B_1 = \frac{1}{3}[I_{max} + I_{\frac{1}{2}} - I_{-\frac{1}{2}} - I_{min}] \quad \text{... (28)}$$

$$B_2 = \frac{1}{4}[I_{max} - 2\, I_{CQ} + I_{min}] \quad \text{... (29)}$$

$$B_3 = \frac{1}{6}[I_{max} - 2\, I_{\frac{1}{2}} + 2\, I_{-\frac{1}{2}} - I_{min}] \quad \text{... (30)}$$

$$B_4 = \frac{1}{12}[I_{max} - 4\, I_{\frac{1}{2}} + 6\, I_{CQ} - 4\, I_{-\frac{1}{2}} + I_{min}] \quad \text{... (31)}$$

Hence the harmonic distortion coefficients can be obtained as,

$$D_n = \frac{|B_n|}{|B_1|} \quad \text{... Refer equation (1)}$$

As the method uses five points on the output waveform to obtain the amplitudes of the various orders of harmonics, the method is called '**Five Point Method**' of determining the higher order harmonic distortion.

6.9.6 Power Output Due to Distortion

Now $P_{ac} = \frac{1}{2} B_1^2 R_L$ ...Refer equation (17)

Hence the output power with harmonic distortion is,

$$(P_{ac})_D = \frac{1}{2} B_1^2 R_L + \frac{1}{2} B_2^2 R_L + \frac{1}{2} B_3^2 R_L + \ldots + \frac{1}{2} B_n^2 R_L$$

$$= \frac{1}{2} B_1^2 R_L \left[1 + \frac{B_2^2}{B_1^2} + \frac{B_3^2}{B_1^2} + \ldots + \frac{B_n^2}{B_1^2}\right]$$

$$\therefore (P_{ac})_D = P_{ac}[1 + D_2^2 + D_3^2 + \cdots + D_n^2] \quad \text{... (32)}$$

But $D^2 = D_2^2 + D_3^2 + \ldots + D_n^2$ ... Refer equation (2)

where D = Total harmonic distortion

$$\therefore \boxed{(P_{ac})_D = P_{ac}(1 + D^2)} \quad \text{...(33)}$$

If the total harmonic distortion is 15 % i.e. D = 0.15

Then $(P_{ac})_D = P_{ac}\,[1 + (0.15)^2\,] = 1.0225\,P_{ac}$

So there is 2.25 % increase in the power given to the load.

Example 6.5 : *Prove that in class A amplifier if distortion is 10 percent power given to the load is increased by 1 percent.*

Solution : The power given to the load without distortion is ,

$$P_{ac} = \frac{1}{2}B_1^2R_L$$

While power given to the load with distortion is

$$(P_{ac})_D \therefore \frac{1}{2}B_1^2R_L + \frac{1}{2}B_2^2R_L + \frac{1}{2}B_3^2R_L + ... + \frac{1}{2}B_n^2R_L$$

Where B_n = Amplitude of n^{th} harmonic component

$$\therefore \quad (P_{ac})_D = \frac{1}{2}B_1^2R_L\left[1 + \frac{B_2^2}{B_1^2} + \frac{B_3^2}{B_1^2} + ... + \frac{B_n^2}{B_1^2}\right] = P_{ac}\left[1 + D_2^2 + D_3^2 + ... + D_n^2\right]$$

Where D_n = n^{th} order harmonic distortion

But $D^2 = D_2^2 + D_3^2 + ... + D_n^2$ = Total Harmonic Distortion

$$\therefore \quad (P_{ac})_D = P_{ac}\,[1 + D^2]$$

Now D = 10 % i.e 0.1 as given

$$\therefore \quad (P_{ac})_D = P_{ac}\,[1 + (0.1)^2] = 1.01\,P_{ac}$$

This shows that power given to the load is increased from 1 to 1.01 i.e increased by 1 %.

Example 6.6 : *A transistor supplies 0.85 W to a 4 kΩ load. The zero signal D.C. collector current is 31 mA and the D.C. collector current with signal is 34 mA. Determine the second harmonic distortion.*

Solution : $R_L = 4\ k\Omega$, $(P_{ac})_D = 0.85$ W

The current without signal is $I_{CQ} = 31$ mA

The current with signal is $I_{CQ} + B_0 = 34$ mA

The increase is due to **harmonic content** in the signal.

$$\therefore \quad B_0 = 34 - 31 = 3\ mA$$

But $B_2 = B_0 = 3$ mA

Now $(P_{ac})_D = P_{ac}\left[1 + D_2^2\right]$ ... Assuming only second harmonic

$$\therefore \quad (P_{ac})_D = \frac{1}{2} B_1^2 R_L \left[1 + \frac{B_2^2}{B_1^2}\right]$$

$$\therefore \quad (P_{ac})_D = \frac{1}{2} B_1^2 R_L + \frac{1}{2} B_2^2 R_L$$

$$\therefore \quad 0.85 = \frac{1}{2} B_1^2 \times 4 \times 10^3 + \frac{1}{2} \times \left(3 \times 10^{-3}\right)^2 \times 4 \times 10^3$$

$$\therefore \quad B_1 = 20.396 \text{ mA}$$

$$\therefore \quad D_2 = \frac{|B_2|}{|B_1|} \times 100 = \frac{3 \times 10^{-3}}{20.396 \times 10^{-3}} \times 100 = 14.708 \%$$

Ans. : second harmonic distortion = **14.708 %.**

6.10 Analysis of Class B Amplifiers

As stated earlier, for class B operation, the quiescent operating point is located on the X-axis itself. Due to this collector current flows only for a half cycle for a full cycle of the input signal. Hence the output signal is distorted. To get a full cycle across the load, a pair of transistors is used in class B operation. The two transistors conduct in alternate half cycles of the input signal and a full cycle across the load is obtained. The two transistors are identical in characteristics and called matched transistors.

Depending upon the types of the two transistors whether p-n-p or n-p-n, the two circuit configurations of class B amplifier are possible. These are,

1. When both the transistors are of same type i.e. either n-p-n or p-n-p then the circuit is called **push pull class B** A.F. power amplifier circuit.
2. When the two transistors form a complementary pair i.e. one n-p-n and other p-n-p then the circuit is called **complementary symmetry class B** A.F. power amplifier circuit. Let us analyse these two circuits of class B amplifiers in detail.

6.11 Push Pull Class B Amplifier

The push pull circuit requires two transformers, one as input transformer called **driver transformer** and the other to connect the load called **output transformer**. The input signal is applied to the primary of the driver transformer. Both the transformers are centre tapped transformers. The push pull class B amplifier circuit is shown in the Fig. 6.25.

In the circuit, both Q_1 and Q_2 transistors are of n-p-n type. The circuit can use both Q_1 and Q_2 of p-n-p type. In such a case, the only change is that the supply voltage must be $-V_{CC}$, the basic circuit remains the same. Generally the circuit using n-p-n transistors is used. Both the transistors are in common emitter configuration.

The driver transformer drives the circuit. The input signal is applied to the primary of the driver transformer. The centre tap on the secondary of the driver transformer is grounded. The centre tap on the primary of the output transformer is connected to the supply voltage + V_{CC}.

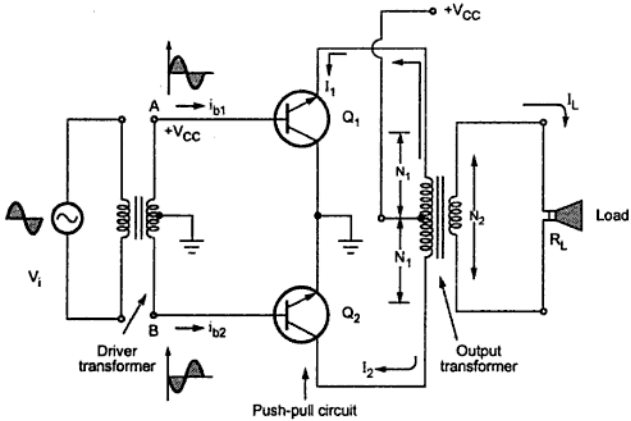


Fig. 6.25 Push pull class B amplifier

With respect to the centre tap, for a positive half cycle of input signal, the point A shown on the secondary of the driver transformer will be positive. While the point B will be negative. Thus the voltages in the two halves of the secondary of the driver transformer will be equal but with opposite polarity. Hence the input signals applied to the base of the transistors Q_1 and Q_2 will be 180° out of phase.

The transistor Q_1 conducts for the positive half cycle of the input producing positive half cycle across the load. While the transistor Q_2 conducts for the negative half cycle of the input producing negative half cycle across the load. Thus across the load, we get a full cycle for a full input cycle. The basic push pull operation is shown in the Fig. 6.26.

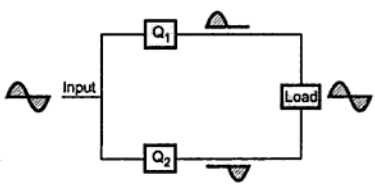


Fig. 6.26 Basic push pull operation

When point A is positive, the transistor Q_1 gets driven into an active region while the transistor Q_2 is in cut-off region. While when point A is negative, the point B is positive, hence the transistor Q_2 gets driven into an active region while the transistor Q_1 is in cut-off region.

The waveforms of the input current, base currents, collector currents and the load current are shown in the Fig. 6.27.

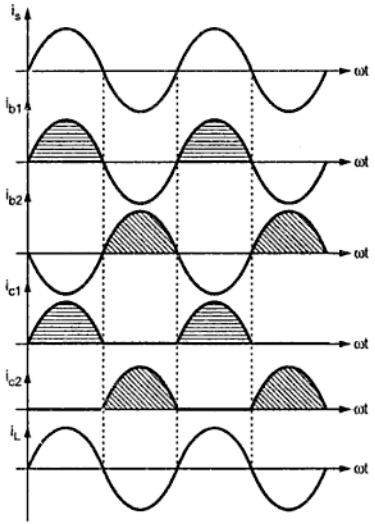


Fig. 6.27 Waveforms for push pull class B amplifier

Key Point : *For the output transformer, the number of the turns of each half of the primary is* N_1 *while the number of the turns on the secondary is* N_2. *Hence the total number of primary turns is* $2N_1$. *So turns ratio of the output transformer is specified as* $2N_1$. *So turns ratio of the output transformer is specified as* $2N_1 : N_2$.

6.11.1 D.C. Operation

The d.c. biasing point i.e. Q point is adjusted on the X-axis such that $V_{CEQ} = V_{CC}$ and I_{CEQ} is zero. Hence the co-ordinates of the Q point are (V_{CC}, 0). There is no d.c. base bias voltage.

6.11.2 D.C. Power Input

Each transistor output is in the form of half rectified waveform. Hence if I_m is the peak value of the output current of each transistor, the d.c. or average value is $\frac{I_m}{\pi}$, due to half rectified waveform. **The two currents, drawn by the two transistors, form the d.c. supply are in the same direction. Hence the total d.c.** or average current drawn from the **supply is the algebraic sum of the individual average** current drawn by each transistor.

$$\therefore \quad \boxed{I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi}} \qquad \ldots (1)$$

The total d.c. power input is given by,

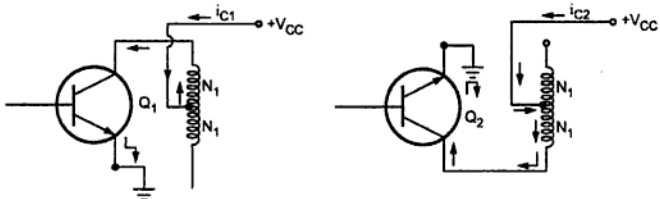
$$P_{DC} = V_{CC} \times I_{dc}$$

$$\therefore \quad \boxed{P_{DC} = \left(\frac{2I_m}{\pi}\right) V_{CC}} \qquad \ldots (2)$$

6.11.3 A.C. Operation

When the a.c. signal is applied to the driver transformer, for positive half cycle Q_1 conducts. The path of the current drawn by the Q_1 is shown in the Fig. 6.28.

For the negative half cycle Q_2 conducts. The path of the current drawn by the Q_2 is shown in the Fig. 6.28 (b).



(a) Q_1 conduction (b) Q_2 conduction

Fig. 6.28

It can be seen that when Q_1 conducts, lower half of the primary of the output transformer does not carry any current. Hence only N_1 number of turns carry the current. While when Q_2 conducts, upper half of the primary does not carry any current. Hence again only N_1 number of turns carry the current. Hence the reflected load on the primary can be written as,

$$\therefore \quad \boxed{R'_L = \frac{R_L}{n^2}} \qquad \ldots (3)$$

where $$n = \frac{N_2}{N_1}$$

It is important to note that the step down turns ratio is $2N_1 : N_2$ but while calculating the reflected load, the ratio n becomes N_2/N_1. So each transistor shares equal load which is the reflected load R'_L given by the equation (3).

The slope of the a.c. load line is $-1/R'_L$ while the d.c. load line is the vertical line passing through the operating point Q on the X-axis. The load lines are shown in the Fig. 6.29.

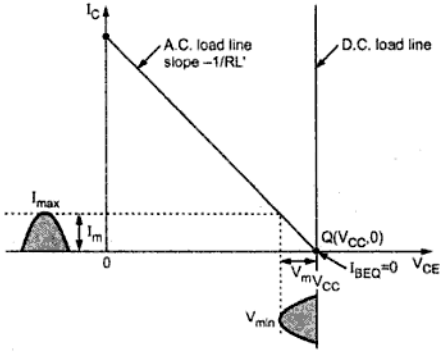


Fig. 6.29 Load lines for push pull class B amplifier

The slope of the a.c. load line (magnitude of slope) can be represented interms of V_m and I_m as,

$$\frac{1}{R'_L} = \frac{I_m}{V_m}$$

$$\therefore \quad \boxed{R'_L = \frac{V_m}{I_m}} \qquad \ldots (4)$$

where I_m = Peak value of the collector current

6.11.4 A.C. Power Output

As I_m and V_m are the peak values of the output current and the output voltage respectively, then

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

and $$I_{rms} = \frac{I_m}{\sqrt{2}}$$

Hence the a.c. power output is expressed as,

$$P_{ac} = V_{rms}\ I_{rms} = I^2_{rms}\ R'_L = \frac{V^2_{rms}}{R'_L} \qquad \ldots (5)$$

$$\therefore \quad P_d = \frac{2}{\pi} V_{CC} \frac{V_m}{R_L'} - \frac{V_m^2}{2R_L'} \quad \ldots (8)$$

Let us find out the condition for maximum power dissipation. In case of class A amplifier, it is maximum when no input signal is there. But in class B operation, when the input signal is zero, $V_m = 0$ hence the power dissipation is zero and not the maximum.

Maximum power dissipation : The condition for maximum power dissipation can be obtained by differentiating the equation (8) with respect to V_m and equating it to zero.

$$\therefore \quad \frac{dP_d}{dV_m} = \frac{2}{\pi} \frac{V_{CC}}{R_L'} - \frac{2V_m}{2R_L'} = 0$$

$$\therefore \quad \frac{2}{\pi} \frac{V_{CC}}{R_L'} = \frac{V_m}{R_L'}$$

$$\boxed{V_m = \frac{2}{\pi} V_{CC}} \quad \ldots \text{ For maximum power dissipation} \quad \ldots (9)$$

This is the **condition for maximum power** dissipation. Hence the maximum power dissipation is,

$$(P_d)_{max} = \frac{2}{\pi} V_{CC} \times \frac{2}{\pi} \frac{V_{CC}}{R_L'} - \frac{4}{\pi^2} \frac{V_{CC}^2}{2R_L'}$$

$$= \frac{4}{\pi^2} \frac{V_{CC}^2}{R_L'} - \frac{2}{\pi^2} \frac{V_{CC}^2}{R_L'}$$

$$\therefore \quad \boxed{(P_d)_{max} = \frac{2}{\pi^2} \frac{V_{CC}^2}{R_L'}} \quad \ldots (10)$$

Key Point : *For maximum efficiency,* $V_m = V_{CC}$ *hence the power dissipation is not maximum when the efficiency is maximum. And when power dissipation is maximum, efficiency is not maximum.* ***So maximum efficiency and maximum power dissipation do not occur simultaneously,*** *in case of class B amplifiers.*

Now $P_{ac} = \frac{V_m^2}{2R_L'}$

and $V_m = V_{CC}$ is the maximum condition.

Hence $(P_{ac})_{max} = \frac{V_{CC}^2}{2R_L'}$ ... (11)

Now $(P_d)_{max} = \frac{2V_{CC}^2}{\pi^2 R_L'} = \frac{4}{\pi^2}\left(\frac{V_{CC}^2}{2R_L'}\right)$

$\therefore \quad (P_d)_{max} = \frac{4}{\pi^2} (P_{ac})_{max}$ ... (12)

This much power is dissipated by both the transistors hence the maximum power dissipation per transistor is $(P_d)_{max} / 2$.

$$\therefore \quad (P_d)_{max} \text{ per transistor} = \frac{\frac{4}{\pi^2}(P_{ac})_{max}}{2}$$

$$\therefore \quad \boxed{(P_d)_{max} \text{ per transistor} = \frac{2}{\pi^2}(P_{ac})_{max}} \qquad \ldots (13)$$

This is the **maximum power dissipation rating** of each transistor. For example, if 10 W maximum power is to be supplied to the load, then power dissipation rating of each transistor should be $\frac{2}{\pi^2} \times 10$ i.e. 2.02 W.

Example 6.7 : *Prove that in case of push pull class B amplifier, the efficiency at the time of maximum power dissipation is just 50 %.*

Solution : The maximum power dissipation occurs when the value of V_m is

$$V_m = \frac{2}{\pi} V_{CC} \qquad \ldots \text{ Refer equation (9)}$$

Now $$P_{ac} = \frac{V_m I_m}{2}$$

So at the time of maximum power dissipation, it is

$$P_{ac} = \frac{2}{\pi} \frac{V_{CC} I_m}{2} = \frac{V_{CC} I_m}{\pi}$$

Now $$P_{DC} = \frac{2}{\pi} V_{CC} I_m$$

Hence $$\% \eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{\left(\frac{V_{CC} I_m}{\pi}\right)}{\left(\frac{2}{\pi} V_{CC} I_m\right)} \times 100$$

$$= 50 \ \%$$

Thus efficiency is just 50 % when the power dissipation is maximum. While the maximum efficiency of the class B operation is 78.5 %.

6.11.8 Harmonic Distortion

Let the base input currents are sinusoidal in nature and given by,

$$i_{b1} = I_{Bm} \cos \omega t \text{ and } i_{b2} = - I_{Bm} \cos \omega t$$

The negative sign indicates that both are 180° out of phase.

5. Ripples present in supply voltage also get eliminated.
6. Due to the transformer, impedance matching is possible.

The disadvantages of the circuit are :

1. Two center tap transformers are necessary.
2. The transformers, make the circuit bulky and hence costlier.
3. Frequency response is poor.

Example 6.8 : *A class B push pull amplifier supplies power to a resistive load of* 12 Ω. *The output transformer has a turns ratio of 3 : 1 and efficiency of 78.5 %.*

Obtain :

i) Maximum power output

ii) Maximum power dissipation in each transistor

iii) Maximum base and collector current for each transistor.

Assume $h_{fe} = 25$ *and* $V_{CC} = 20$ *V.*

Solution : $R_L = 12\ \Omega,\ n = \frac{N_2}{N_1} = \frac{1}{3} = 0.333,\ \eta_{trans} = 78.5\ \%$

$$\therefore \quad R'_L = \frac{R_L}{(n)^2} = 108\ \Omega$$

i) For P_{max}, $V_m = V_{CC}$

$$\therefore \quad (P_{ac})_{max} = \frac{1}{2}\frac{(V_{CC})^2}{R'_L} = \frac{1}{2}\frac{(20)^2}{108} = \mathbf{1.8518\ W}$$

But $\eta_{trans} = 78.5\ \%$

$$\therefore \quad P_L = \eta_{trans} \times (P_{ac})_{max}$$

$$= 0.785 \times 1.8518 = 1.4537\ W$$

ii) Condition for $(P_d)_{max}$ is $V_m = \frac{2}{\pi} V_{CC} = 12.7323\ V$

$$\therefore \quad (P_d)_{max} = \frac{2}{\pi^2}\frac{V_{CC}^2}{R'_L} = \frac{2}{\pi^2}\frac{(20)^2}{108} = 0.7505\ W$$

$$\therefore \quad (P_d)_{max} \text{ per transistor} = \frac{0.7505}{2} = \mathbf{0.3752\ W}$$

iii) $(P_{ac})_{max} = V_{rms}\, I_{rms} = \frac{V_m}{\sqrt{2}}\frac{I_m}{\sqrt{2}} = \frac{V_m I_m}{2}$ and $V_m = V_{CC}$

$$\therefore \quad 1.8518 = \frac{20\, I_m}{2}$$

$\therefore \quad I_m = 0.1851 \text{ A} = (i_c)_{max}$

and $(i_b)_{max} = \frac{(i_c)_{max}}{h_{fe}} = \frac{0.1851}{25} = 7.407 \text{ mA}$

Example 6.9 : *A class B, push pull amplifier drives a load of 16 Ω , connected to the secondary of the ideal transformer. The supply voltage is 25 V. If the number of turns on the primary is 200 and the number of turns on the secondary is 50, calculate maximum power output, d.c. power input, efficiency and maximum power dissipation per transistor.*

Solution : $R_L = 16 \Omega, \ V_{CC} = 25 \text{ V}$

Now $2N_1 = 200, \ N_2 = 50$

$\therefore \quad N_1 = 100$

$\therefore \quad n = \frac{N_2}{N_1} = \frac{50}{100} = 0.5$

$\therefore \quad R'_L = \frac{R_L}{n^2} = \frac{16}{(0.5)^2}$

$= 64 \Omega$

For maximum power output, $V_m = V_{CC}$

i) $(P_{ac})_{max} = \frac{1}{2} \frac{V_{CC}^2}{R_L} = \frac{1}{2} \times \frac{(25)^2}{64}$

$= 4.8828 \text{ W}$

ii) $P_{dc} = \frac{2}{\pi} V_{CC} I_m$

Now $\frac{V_m}{I_m} = R'_L$

and $V_m = V_{CC}$ ... Refer equation (4)

$\therefore \quad I_m = \frac{V_{CC}}{R'_L} = \frac{25}{64} = 0.3906 \text{ A}$

$\therefore \quad P_{DC} = \frac{2}{\pi} \times 25 \times 0.3906$

$= 6.2169 \text{ W}$

iii) $\% \eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{4.8828}{6.2169} \times 100$

$= 78.5 \%$

In addition, voltage feedback can be used to reduce the output impedance for matching.

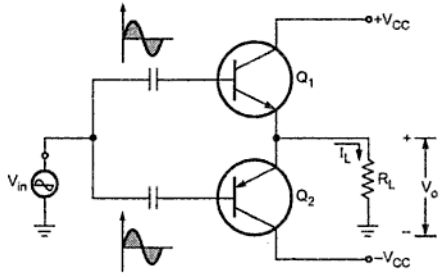


Fig. 6.32 Complementary symmetry class B amplifier

The basic circuit of complementary symmetry class B amplifier is shown in the Fig. 6.32.

The circuit is driven from a dual supply of $\pm V_{CC}$. The transistor Q_1 is n-p-n while Q_2 is of p-n-p type.

In the positive half cycle of the input signal, the transistor Q_1 gets driven into active region and starts conducting. The same signal gets applied to the base of the Q_2 but as it is of complementary type, remains in off condition, during positive half cycle. This results into positive half cycle across the load R_L. This is shown in the Fig. 6.33.

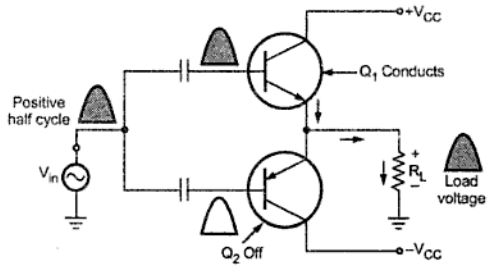


Fig. 6.33 Positive half cycle operation

During the negative half cycle of the signal, the transistor Q_2 being p-n-p gets biased into conduction. While the transistor Q_1 gets driven into cut-off region. Hence only Q_2 conducts during negative half cycle of the input, producing negative half cycle across the load R_L, as shown in the Fig. 6.34 (a).

Thus for a complete cycle of input, a complete cycle of output signal is developed across the load as shown in the Fig. 6.34 (b).

This is the total collector dissipation under maximum power condition.

iii) $$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100$$

$$= \frac{28.125}{35.809} \times 100 = \mathbf{78.5\ \%}$$

The efficiency is maximum possible for class B, due to the fact that the power developed is at its maximum.

iv) For maximum power dissipation,

$$V_m = \frac{2}{\pi} V_{CC}$$

$$= \frac{2}{\pi} \times 15 = 9.5492 \text{ V}$$

$$\therefore \quad I_m = \frac{V_m}{R_L} = \frac{9.5492}{4} = 2.3873 \text{ A}$$

$$\therefore \quad P_{dc} = \frac{2}{\pi} V_{CC}\, I_m$$

$$= \frac{2}{\pi} \times 15 \times 2.3873 = 22.797 \text{ W}$$

While $$P_{ac} = \frac{1}{2} \frac{V_m^2}{R_L} = \frac{1}{2} \frac{(9.5492)^2}{4} = 11.398 \text{ W}$$

$$\therefore \quad (P_d)_{max} = P_{dc} - P_{ac}$$

$$= 22.797 - 11.398 = 11.39 \text{ W}$$

$$\therefore \quad (P_d)_{max} = \frac{11.39}{2} = 5.699 \text{ W per transistor}$$

Alternatively we can directly use the result,

$$(P_d)_{max} = \frac{2}{\pi^2} (P_{ac})_{max} \text{ per transistor}$$

$$= \frac{2}{\pi^2} \times 28.125 = \mathbf{5.699\ W} \text{ per transistor}$$

v) Efficiency under $(P_d)_{max}$ condition,

$$\% \eta = \frac{P_{ac} \text{ under } (P_d)_{max}}{P_{dc} \text{ under } (P_d)_{max}} \times 100 = \frac{11.398}{22.797} \times 100 = \mathbf{50\ \%}$$

This shows that when efficiency is maximum, power dissipation is not maximum. And when power dissipation is maximum, efficiency is not maximum.

Example 6.12 : *A complementary push pull amplifier has capacitive coupled load $R_L = 8\ \Omega$, supply voltage ± 12 V, calculate :*

1) P_{ac} max

2) P_D of each transistor and

3) Efficiency.

Solution : $R_L = 8\ \Omega$, $V_{CC} = \pm 12$ V hence dual supply version

1) $$(P_{ac})_{max} = \frac{1}{2}\frac{V_{CC}^2}{R_L} = \frac{1}{2} \times \frac{(12)^2}{8} = \mathbf{9\ W}$$

2) $$P_{DC} = V_{CC}\, I_{DC} \text{ but } I_{DC} = 2\frac{I_m}{\pi}$$

$$= V_{CC}\left(2\frac{I_m}{\pi}\right)$$

Now $$R_L = \frac{V_m}{I_m} \text{ i.e } I_m = \frac{V_m}{R_L} \text{ and } V_m = V_{CC}$$

$\therefore$ $$P_{DC} = V_{CC} \times 2 \times \frac{V_{CC}}{R_L} \times \frac{1}{\pi} = \frac{(12)^2 \times 2}{8 \times \pi}$$

$$= 11.4591\ \text{W}$$

$\therefore$ $$\text{Total } P_D = P_{DC} - P_{ac} = 11.4591 - 9 = 2.4591\ \text{W}$$

$\therefore$ $$P_D \text{ per transistor} = \frac{2.4591}{2} = \mathbf{1.2295\ W}$$

3) $$\%\ \eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{9}{11.4591} \times 100 = \mathbf{78.5\ \%}$$

Example 6.13 : *A complementary symmetry push pull amplifier is operated using $V_{CC} = \pm 10$ V and delivers power to a load $R_L = 5\ \Omega$.*

Calculate :

(i) Maximum output power

(ii) Power rating of transistors

(iii) D.C. input power.

Solution : $V_{CC} = \pm 10$ V, $R_L = 5\ \Omega$

i) $$(P_{ac})_{max} = \frac{1}{2}\frac{V_{CC}^2}{R_L} = \frac{(10)^2}{2 \times 5} = \mathbf{10\ W}$$

ii) To decide **Power rating of transistors** means to find $(P_D)_{max}$

For $(P_D)_{max}$, $V_m = \frac{2}{\pi} V_{CC} = 6.3662$ V

And $R_L = \frac{V_m}{I_m}$, $\therefore I_m = \frac{V_m}{R_L} = \frac{6.3662}{5} = 1.2732$ A

$\therefore P_{DC} = V_{CC} I_{DC} = V_{CC} \times \frac{2I_m}{\pi}$ ... $I_{DC} = \frac{2I_m}{\pi}$

$= \frac{10 \times 2 \times 1.2732}{\pi} = 8.1056$ W

and $P_{ac} = \frac{V_m I_m}{2} = \frac{6.3662 \times 1.2732}{2} = 4.0527$ W

$\therefore (P_D)_{max} = P_{DC} - P_{ac} = 4.0528$ W

$\therefore P_D$ rating for each transistor $= \frac{(P_D)_{max}}{2} =$ **2.026 W**

iii) For $(P_{ac})_{max}$, $V_m = V_{CC} = 10$ V

$\therefore I_m = \frac{V_m}{R_L} = \frac{10}{5} =$ **2 A**

$\therefore P_{DC} = V_{CC} \times \frac{2I_m}{\pi} = \frac{10 \times 2 \times 2}{\pi} =$ **12.7323 W**

This is P_{DC}, when output power is maximum.

6.13 Comparison of Push Pull and Complementary Symmetry Circuits

Sr. No.	Push Pull Class B	Complementary Symmetry Class B
1.	Both the transistors are similar either p-n-p or n-p-n.	Transistors are complementary type i.e. one n-p-n other p-n-p.
2.	The transformer is used to connect the load as well as input.	The circuit is transformerless.
3.	The impedance matching is possible due to the output transformer.	The impedance matching is possible due to common collector circuit.
4.	Frequency response is poor.	Frequency response is improved.
5.	Due to transformers, the circuit is bulky, costly and heavier.	As transformerless, the circuit is not bulky and costly.
6.	Dual power supply is not required.	Dual power supply is required.
7.	Efficiency is higher than class A.	The efficiency is higher than the push pull.

Table 6.2

than the cut-in voltage of the base emitter junction, the collector current remain zero and transistor remains in cut-off region.

Hence there is a period between the crossing of the half cycles of the input signal, for which none of the transistors is active and the output is zero. Hence the nature of the output signal gets distorted and no longer remains same as that of input. Such a distorted output wave form due to cut-in voltage is shown in the Fig. 6.37.

Such a distortion in the output signal is called a **cross-over distortion**. Due to cross-over distortion each transistor conducts for less than a half cycle rather than the complete half cycle. The part of the input cycles for which the two transistors conduct alternately is shown shaded in the Fig. 6.37. The cross-over distortion is common in both the types of class B amplifiers.

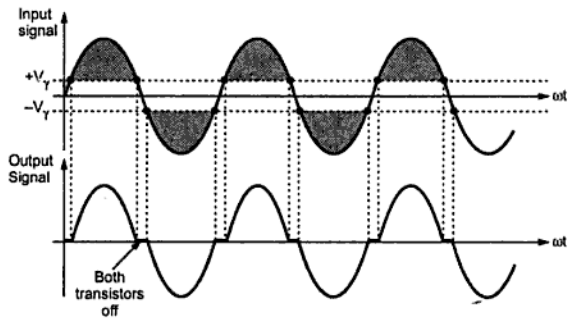


Fig. 6.37 Cross-over distortion

6.16 Elimination of Cross-Over Distortion

To eliminate the cross-over distortion some modifications are necessary, in the basic circuits of the class B amplifiers. The basic reason for the cross over distortion is the cut-in voltage of the transistor junction. To overcome this cut-in voltage, a small forward biased is applied to the transistors. Let us see the practical circuits used to apply such forward biased, in the two types of class B amplifiers.

6.16.1 Push Pull Class B Amplifier

The forward biased across the base-emitter junction of each transistor is provided by using a diode as shown in the Fig. 6.38.

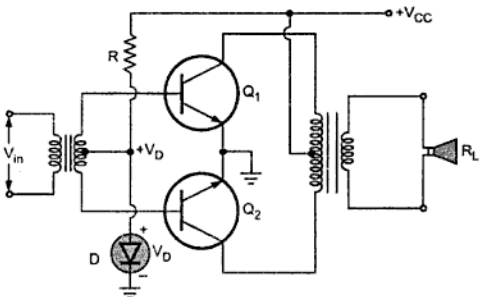


Fig. 6.38 Use of Diode

The drop across the diode D is equal to the cut-in voltage of the base-emitter junction of the transistor. Hence both the transistors conduct for full half cycle, eliminating the cross-over distortion.

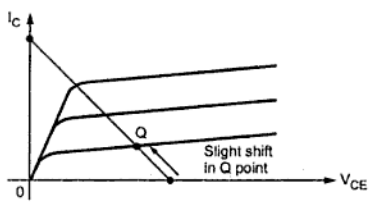


Fig. 6.39

Due to the forward biased provided to eliminate the cross-over distortion, the Q point shifts upwards on the load line as shown in the Fig. 6.39. Hence the operation of the amplifier no longer remains class B but becomes class AB operation.

But as the amplifier handles the large signals in the range of volts, compared to these signals the shift in Q point is negligibly small.

Key Point : *For all the practical purposes, the operation is treated as class B operation and all the expression derived are applicable to these modified circuits.*

6.16.2 Complementary Symmetry Class B Amplifier

In push pull, transformer coupled type, the drop across forward biased one diode is sufficient, to provide necessary cut-in voltage. But in case of complementary symmetry circuit, base emitter junctions of both Q_1 and Q_2, are required to provide a fixed bias. Hence for silicon transistors a fixed bias of 0.7 + 0.7 = 1.4 V is required. This can be achieved by using a potential divider arrangement as shown in the Fig. 6.40.

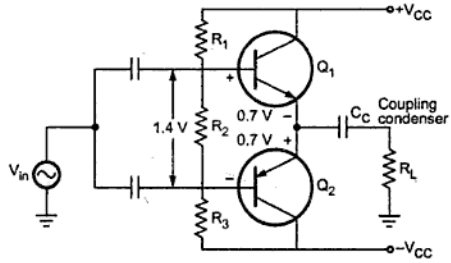


Fig. 6.40 Use of potential divider

But in this circuit, the fixed bias provided is fixed equal to say 1.4 V. While the junction cut-in voltage changes with respect to the temperature. Hence there is still possibility of a distortion when there is temperature change. Hence instead of R_2, the two diodes can be used to provide the required fixed bias. As the temperature changes, along with the junction characteristics, the diode characteristics get changed and maintain the necessary biasing required to overcome the cross-over distortion when there is temperature change. The arrangement of the circuit with the two diodes is shown in the Fig. 6.41.

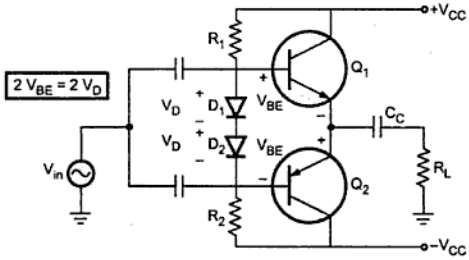


Fig. 6.41 Use of pair of diodes

6.17 Complementary Symmetry Single Supply Version

The main disadvantage as seen earlier of complementary amplifier is the use of dual supply. But in practice the circuit can be modified by grounding – V_{CC} terminal. The resulting circuit is called single supply version of complementary symmetry class B amplifier as shown in the Fig. 6.42.

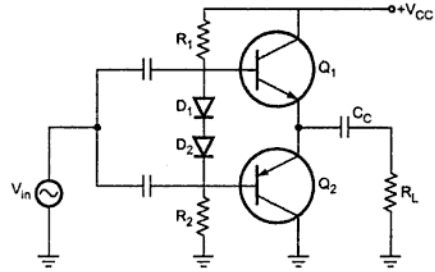


Fig. 6.42 Single supply version of complementary symmetry class B amplifier

Key Point : *All the expression derived for dual supply version are still applicable to single supply version. Only change required is that the value of V_{CC} must be taken as $V_{CC}/2$, while calculating the various parameters of the circuit.*

Example 6.14 : *The circuit shown in Fig. 6.43 operates with sinusoidal input. Calculate :*

i) Maximum A.C. power output

ii) Power dissipation in each transistor

iii) Conversion efficiency at maximum power output.

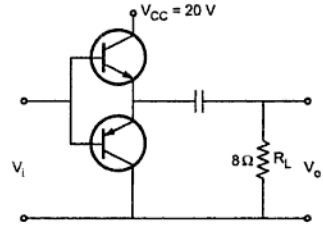


Fig. 6.43

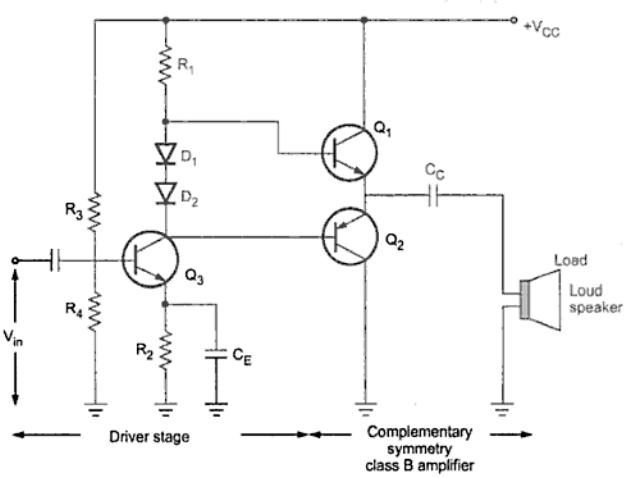


Fig. 6.44

6.19 Quasi - Complementary Push Pull Amplifier

Practically in the power amplifier circuits it is preferred to have both n-p-n transistors to supply to load. But complementary symmetry circuit requires one n-p-n and other p-n-p transistor for its operation.

In practice, the complementary symmetry circuit is modified in such a way that matched n-p-n transistors can supply the load though the operation is complementary. Such a modified circuit is called quasi-complementary push pull amplifier. This is shown in the Fig. 6.45.

The Q_1 and Q_2 are complementary transistors as Q_1 is n-p-n and Q_2 is p-n-p. The complementary operation is possible because of Q_1 and Q_2. The Q_1 and Q_3 form a **Darlington pair** while Q_2 and Q_4 form a Feedback pair. The collector of Q_2 is connected to the base of Q_4. The diodes Q_1 and Q_2 are used to overcome cross-over distortion.

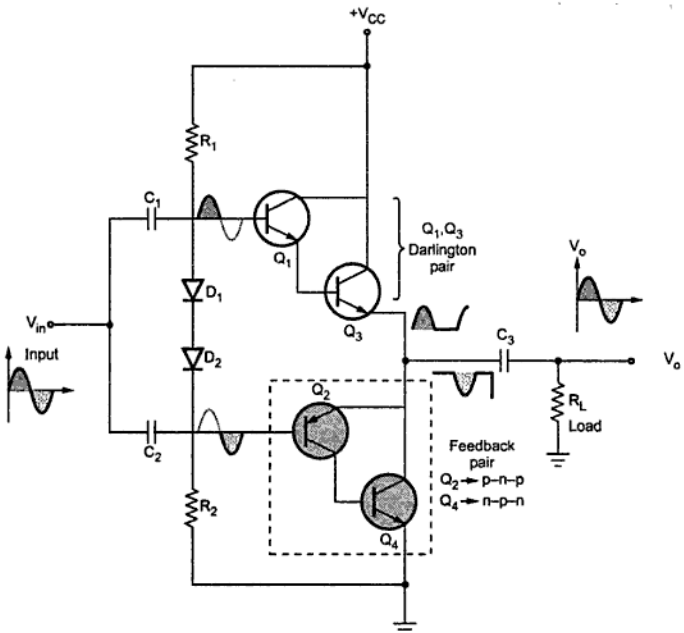


Fig. 6.45 Quasi-complementary power amplifier

6.19.1 Operation

For **positive half cycle** of input, the base of n-p-n Q_1 goes positive and Q_1 conducts, due to which Q_3 conducts. While at the same time base of p-n-p Q_2 goes positive hence Q_2 remains cut-off. Thus the Q_1, Q_3 Darlington pair drives the load providing positive half cycle to the load with a low impedance. For **negative half cycle** of input, the base of n-p-n Q_1 goes negative and hence it remains cut-off. While at the same time base of p-n-p Q_2 goes negative hence Q_2 conducts. This drives Q_4 to conduct providing negative half cycle to the load with a low impedance. Thus for common input signal applied to the circuit, a full cycle is available across the load.

Key Point : *Practically the quasi-complementary push pull power amplifier circuit is most widely used power amplifier circuit.*

Examples with Solutions

Example 6.15 : *How much power is dissipated in the individual transistors of a class B push pull power amplifier ? If V_{CC} = 20 V and R_L = 4 Ω.*

Solution : V_{CC} = 20 V, R_L = 4 Ω

For $(P_d)_{max}$, $V_m = \frac{2}{\pi} V_{CC} = 12.7324$ V

$$R_L = \frac{V_m}{I_m}$$

$$\therefore \quad I_m = \frac{V_m}{R_L} = 3.183 \text{ A}$$

$$\therefore \quad I_{DC} = \frac{2}{\pi} I_m = 2.0254 \text{ A}$$

$$\therefore \quad P_{ac} = \frac{1}{2} \frac{V_m^2}{R_L} = \frac{1}{2} \frac{(12.7324)^2}{4} = 20.2542 \text{ W}$$

and $P_{dc} = V_{CC} I_{DC} = 20 \times 2.0254 = 40.508$ W

$$\therefore \quad \text{Total } (P_d)\,\text{max} = P_{dc} - P_{ac} = 40.508 - 20.2542 = 20.2538 \text{ W}$$

$$\therefore (P_d)\,\text{max per transistor} = \frac{20.2538}{2} = \mathbf{10.1269\ W}$$

Example 6.16 : *A single ended class A transformer coupled amplifier employs a transistor with I_{cm} = 1 A, P_d = 10 W and V_{CEO} = 40 V, feeds a 2.5 Ω load. Calculate the maximum power output that can be delivered to the load. Determine the turns ratio of the output transformer.*

Solution : For a given transistor,

Maximum collector current = I_{cm} = 1 A

Maximum power dissipation = P_d = 10 W

Maximum V_{CEO} = 40 V

For maximum output power,

$$I_{cm} = 2I_{CQ}$$

$$\therefore \quad I_{CQ} = \frac{I_{cm}}{2} = \frac{1}{2} = 0.5 \text{ A}$$

and $V_{CEO} = 2V_{CC}$

$$\therefore \quad V_{CC} = \frac{V_{CEO}}{2} = \frac{40}{2} = 20 \text{ V}$$

For the full wave rectified waveform,

$$I_{DC} = \frac{2I_m}{\pi} = \frac{2\times 0.6333}{\pi} = 0.4031 \text{ A}$$

$$\therefore \quad P_{DC} = V_{CC} \times I_{DC} = 24 \times 0.4031$$

$$= 9.6765 \text{ W}$$

$$\therefore \quad \% \eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{7.1428}{9.6765} \times 100 = \mathbf{73.81\ \%}$$

This is the conversion efficiency of the amplifier.

Example 6.19 : *Calculate the input power, output power and the efficiency of class A amplifier shown in the Fig. 6.47. The input voltage causes a base current 5 mA rms.*

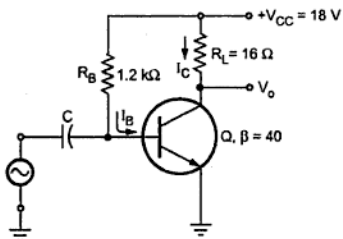


Fig. 6.47

Solution : Using equation (2) from section 6.7, we can determine I_{BQ}.

$$I_{BQ} = \frac{V_{CC} - 0.7}{R_B} = \frac{18 - 0.7}{1.2\times 10^3}$$

$$= 14.4167 \text{ mA}$$

Now $I_{CQ} = \beta I_{BQ} = 40 \times 14.4167 = 576.67 \text{ mA}$

And $V_{CEQ} = V_{CC} - I_{CQ} R_L = 18 - 576.67\times 10^{-7} \times 16 = 8.7733 \text{ V}$

So $P_{dc} = V_{CC} I_{CQ} = 18 \times 576.67 = \mathbf{10.38\ W}$

This is the input power.

Now input a.c. voltage causes a base current of 5 mA r.m.s.

$$\therefore \quad (I_b)rms = 5 \text{ mA}$$

$$\therefore \quad (i_c)rms = \beta\,(i_b)rms = 40 \times 5 = 200 \text{ mA}$$

This is nothing but the output collector current, r.m.s. value I_{rms}.

$$\therefore \quad I_{rms} = 200 \text{ mA}$$

Using equation (13) from section 6.8, we can write,

$$P_{ac} = I_{rms}^2 R_L = (200 \times 10^{-3}) \times 16$$

$$= \mathbf{640 \text{ mW}}$$

This is the power delivered to the load.

Hence the efficiency of the amplifier is,

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{640 \times 10^{-3}}{10.38} \times 100$$

$$= \mathbf{6.165 \%}$$

Example 6.20 : *A transistor connected in class A power amplifier circuit has* $\beta = 40$.

i) Calculate the base current required to set the operating point that will permit maximum possible peak to peak output voltage.

ii) What is the power delivered to the load ?

iii) Verify that the efficiency of the operation is 50 %.

Assume supply voltage of 20 V, the load resistance of 20 Ω and the stepdown turns ratio of 1.58 : 1.

Solution : $V_{CC} = 20$ V, $R_L = 20\ \Omega$, turns ratio 1.58 :1

$$n = \frac{1}{1.58} = 0.6329$$

$$\therefore \quad R'_L = \frac{R_L}{n^2} = \frac{20}{(0.6329)^2} = 49.928\ \Omega$$

i) For maximum possible peak to peak output voltage, the power output is also maximum possible. For this condition the slope of the a.c. load line can be expresed as

$$R'_L = \frac{V_m}{I_m} = \frac{V_{CC}}{I_{CQ}}$$

$$49.928 = \frac{20}{I_{CQ}}$$

$$\therefore \quad I_{CQ} = 0.4 \text{ A}$$

$$\therefore \quad I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{0.4}{40} = \mathbf{0.01}$$

This is the required value of the base current.

ii) $P_{ac} = I_{1rms}^2 R_L'$

But for maximum power output condition,

$$I_{1rms} = \frac{I_{1m}}{\sqrt{2}} = \frac{I_{CQ}}{\sqrt{2}} = \frac{0.4}{\sqrt{2}} = 0.28285 \text{ A}$$

$\therefore$ $P_{ac} = (0.2828)^2 \times 49.928 = \mathbf{3.9942\ W \approx 4\ W}$

iii) $\% \eta = \frac{P_{ac}}{P_{DC}} \times 100$

Now $P_{DC} = V_{CC} I_{CQ} = 20 \times 0.4 = 8$ W

$\% \eta = \frac{4}{8} \times 100 = \mathbf{50\ \%}$

Example 6.21 : *A push pull class B A.F. power amplifier uses the ideal transformer having a total of 160 turns on the primary and 40 turns on the secondary. It must be capable of delivering 40 W power to the 8 Ω speaker, under maximum condition. How much should be the value of V_{CC} ?*

Solution : $R_L = 8\ \Omega$, $P_{ac(max)} = 40$ W

$2N_1 = 160$, $N_2 = 40$

$N_1 = 80$

$n = \frac{N_2}{N_1} = \frac{40}{80} = 0.5$

$\therefore$ $R_L' = \frac{R_L}{n^2} = \frac{8}{(0.5)^2} = 32\ \Omega$

Under maximum condition, $V_{CC} = V_m$

$\therefore$ $P_{ac(max)} = \frac{1}{2} \frac{V_{CC}^2}{R_L'}$

$\therefore$ $40 = \frac{1}{2} \times \frac{V_{CC}^2}{32}$

$\therefore$ $V_{CC}^2 = 40 \times 2 \times 32 = 2560$

$\therefore$ $V_{CC} = \mathbf{50.60\ V}$

This is the required value of V_{CC}.

Example 6.22 : *For a class B amplifier using common collector configuration, the supply voltage is 25 V while the load resistance is 16 Ω. If the input a.c. signal of 20 V peak is supplied, determine the input power, output power and the efficiency.*

Solution : For a common collector configuration the voltage gain is 1.

$$\therefore \quad V_{in(peak)} = V_{out(peak)} = 20 \text{ V}$$

$$\text{i.e.} \quad V_m = 20 \text{ V}$$

$$\text{Now} \quad \frac{V_m}{I_m} = R_L$$

$$\therefore \quad I_m = \frac{V_m}{R_L} = \frac{20}{16} = 1.25 \text{ A}$$

$$\text{while} \quad V_{CC} = 25 \text{ V}$$

$$\text{Now} \quad P_{DC} = \frac{2}{\pi} V_{CC} I_m = \frac{2}{\pi} \times 25 \times 1.25 = 19.8943 \text{ W}$$

$$P_{ac} = \frac{V_m I_m}{2} = \frac{20 \times 1.25}{2} = 12.5 \text{ W}$$

$$\therefore \quad \%\eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{12.5}{19.8943} \times 100 = \mathbf{62.832\ \%}$$

Example 6.23 : *The collector characteristics of a certain transistor is given as,*

V_{CE}	I_C A For		
	I_B = 5 mA	I_B = 15 mA	I_B = 25 mA
1	0.32	0.98	1.55
5	0.38	1.04	1.65
10	0.40	1.12	1.8
15	0.42	1.20	-
20	0.48	-	-

The above transistor is to be used as a single ended transformer coupled class A amplifier with the operating point as V_{CEQ} = 7.5 V and I_{CQ} = 1.1 A. The reflected load across the primary of the transformer is 10 Ω and the input sinusoidal current is 10 mA. Plot the characteristics, draw the loadline and hence calculate the second harmonic distortion.

Solution : For a given power amplifier, V_{CEQ} = 7.5 V and I_{CQ} = 1.1 A. The reflected load R'_L = 10 Ω.

From given data, draw the characteristics to the scale on the graph paper.

Now slope of the load line is $-1/R'_L = -1/10 = -0.1$

$$\text{Slope of load line} = \frac{dI}{dV} = -0.1$$

Solution : The given circuit is the single supply version of class B, complementary symmetry amplifier.

For this case, all the expressions derived for double supply version are applicable but the value of V_{CC} must be used as V_{CC} / 2.. Hence for this circuit,

$$V_{CC} = \frac{12}{2} = 6 \text{ V}$$

$$\therefore \quad (P_{ac})_{max} = \frac{1}{2}\frac{V_{CC}^2}{R_L}$$

Note that, in the circuit given there is additional resistance R_E inserted in the emitter of each transistor. Hence the effective resistance to be considered while calculating the current is $R_L + R_E$.

Now $$I_m = \frac{V_m}{(R_L + R_E)}$$

$$\therefore \quad (P_{ac}) = \frac{V_m I_m}{2}$$

and $$V_m = I_m R_L$$

$$\therefore \quad (P_{ac}) = \frac{I_m^2 R_L}{2} = \frac{V_m^2}{(R_L + R_E)^2} \cdot \frac{R_L}{2}$$

For $(P_{ac})_{max}$, $V_m = V_{CC}$

$$\therefore \quad (P_{ac})_{max} = \frac{V_{CC}^2}{(R_L + R_E)^2} \cdot \frac{R_L}{2} = \frac{(6)^2}{(8+1)^2} \times \frac{8}{2} = 1.77 \text{ W}$$

ii) The maximum power dissipation of each transistor is,

$$(P_d)_{max} = \frac{2}{\pi^2} \times (P_{ac})_{max} \text{ for each transistor}$$

$$= \frac{2}{\pi^2} \times 1.77 = 0.36 \text{ W}$$

or $$(P_d)_{max} = \frac{V_m^2}{(R_L + R_E)^2} \times \frac{R_L}{2} \text{ where } V_m = \frac{2}{\pi} V_{CC}$$

$$\therefore \quad (P_d)_{max} = \left(\frac{2}{\pi}\right)^2 \times \frac{V_{CC}^2}{(R_L + R_E)^2} \times \frac{R_L}{2} = 0.72 \text{ W}$$

Hence per transistor $$(P_d)_{max} = \frac{0.72}{2} = 0.36 \text{ W}.$$

While the voltage rating per transistor is $2V_{CC}$ i.e. $2 \times 6 = 12$ V

Example 6.26 : *A single transistor amplifier with transformer coupled load produces harmonic amplitudes in the output as*

$B_0 = 1.5\ mA \quad B_3 = 4\ mA$

$B_1 = 120\ mA \quad B_4 = 2\ mA$

$B_2 = 10\ mA \quad B_5 = 1\ mA$

i) Determine the percentage total harmonic distortion.

ii) Assume a second identical transistor is used along with a suitable transformer to provide push pull operation. Use the above harmonic amplitudes to determine the new total harmonic distortion.

Solution : i) As single transistor is used, even harmonic components will not get eliminated.

$$D_2 = \frac{|B_2|}{|B_1|} = \frac{10}{120} = 0.0833 \text{ i.e. } 8.33\ \%$$

$$D_3 = \frac{|B_3|}{|B_1|} = \frac{4}{120} = 0.0333 \text{ i.e. } 3.33\ \%$$

$$D_4 = \frac{|B_4|}{|B_1|} = \frac{2}{120} = 0.01667 \text{ i.e. } 1.667\ \%$$

$$D_5 = \frac{|B_5|}{|B_1|} = \frac{1}{120} = 0.00833 \text{ i.e. } 0.833\ \%$$

The total harmonic distortion is,

$$\% D = \sqrt{D_2^2 + D_3^2 + D_4^2 + D_5^2} \times 100$$

$$= \sqrt{(0.0833)^2 + (0.0333)^2 + (0.01667)^2 + (0.00833)^2} \times 100$$

$$= \mathbf{9.1624\ \%}$$

ii) When identical second transistor is used, then **all even harmonics get eliminated.** So only D_3 and D_5 will be present.

$$\therefore \quad \% D = \sqrt{D_3^2 + D_5^2} \times 100 = \sqrt{(0.033)^2 + (0.00833)^2} \times 100$$

$$= \mathbf{3.4326\ \%}$$

Example 6.27 : *The circuit shown in the Fig. 6.50 uses two identical and ideal transistors.*

i) Calculate the maximum a.c. power that can be delivered to the load.

ii) If it is desired to increase the power delivered to the load by 36 %, by what percent must the supply voltage be increased ? What should be the minimum breakdown voltage of the transistor used when the supply voltage is increased ?

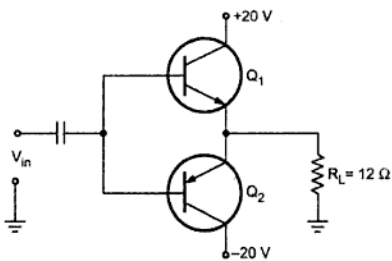


Fig. 6.50

Solution : From the Fig. 6.50 we can write,

$$V_{CC} = 20 \text{ V and } R_L = 12\ \Omega$$

i) The maximum a.c. power that can be delivered to the load is,

$$(P_{ac})_{max} = \frac{1}{2}\frac{V_{CC}^2}{R_L} = \frac{1}{2}\frac{(20)^2}{12} = \mathbf{16.67\ W}$$

ii) Let new power delivered to the load be $(P_{ac})'$.

The corresponding new supply voltage be V'_{CC}.

$$(P_{ac})' = 1.36\ (P_{ac})_{max} \quad \text{... 36 \% more}$$

$$= 1.36 \times 16.67 = 22.67 \text{ W}$$

And $$(P_{ac})' = \frac{1}{2}\frac{(V'_{CC})^2}{R_L}$$

$$\therefore \quad 22.67 = \frac{1}{2} \times \frac{(V'_{CC})^2}{12}$$

$$\therefore \quad (V'_{CC})^2 = 544.1088$$

$$\therefore \quad (V'_{CC}) = 23.326 \text{ V}$$

ii) A.C. power output

$$(P_{ac})_{max} = \frac{1}{2} \times \frac{V_{CC}^2}{R_L'} \text{ as } V_m = V_{CC} \text{ for maximum}$$

$$= \frac{1}{2} \times \frac{(30)^2}{8} = \mathbf{56.25\ W}$$

iii) Efficiency

$$\%\eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{8}{27} \times 100$$

$$= \mathbf{29.62\ \%}$$

iv) Power dissipation by both the transistors

$$P_d = P_{DC} - P_{ac} = 27 - 8$$

$$= \mathbf{19\ W}$$

Hence power dissipation per transistor is

$$= \frac{19}{2}$$

$$= \mathbf{9.5\ W}$$

Example 6.30 : *For a class A amplifier shown in the Fig. 6.51 transformer turns ratio 8 : 1. The transformer has an efficiency of 90 % and d.c resistance of 10 Ω for the primary. Transistor has β = 20 and V_{BE} = 0.5 V. Determine :*

i) Maximum power delivered to the load ii) Circuit efficiency

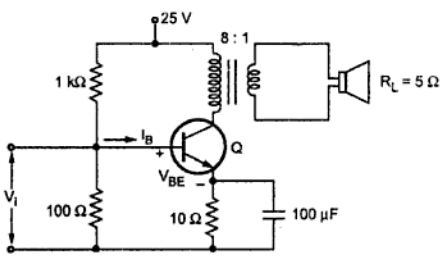


Fig. 6.51

Solution : The circuit used for providing proper biasing is self bias, for which the various currents can be shown as in the Fig. 6.52.

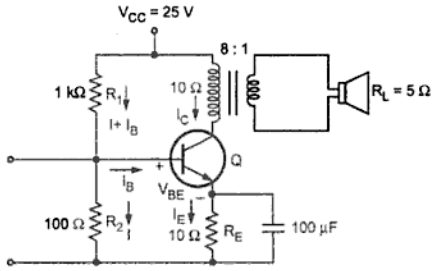


Fig. 6.52

Applying KVL to base-emitter loop,

$$-V_{BE} - I_E R_E + IR_2 = 0$$

$$\therefore \quad I \times 100 - (1 + \beta) I_B \times 10 = V_{BE}$$

$$\therefore \quad 100\, I - 210\, I_B = 0.5 \qquad \ldots (1)$$

Applying KVL through R_1 and R_2,

$$-R_1 (I + I_B) - R_2 I + V_{CC} = 0$$

$$\therefore \quad -1000 (I + I_B) - 100\, I = -V_{CC}$$

$$\therefore \quad 1100\, I + 1000\, I_B = 25 \qquad \ldots (2)$$

Multiplying equation (1) by (11) and subtracting from equation (2) we get,

$$3310\, I_B = 19.5$$

$$\therefore \quad I_B = 0.00589 \text{ A}$$

$$\therefore \quad I_C = \beta I_B = 117.82 \text{ mA} = I_{CQ}$$

Now $$n = \frac{N_2}{N_1} = \frac{1}{8}$$

$$\therefore \quad R'_L = \frac{R_L}{n^2} = \frac{5}{\left(\frac{1}{8}\right)^2} = 320\ \Omega$$

i) For maximum power delivered to load,

$$V_{1m} = V_{CEQ}$$

ii) Power delivered to load under maximum signal conditions.

iii) Conversion efficiency under maximum signal.

iv) Approximate value of C, if the circuit is used at signal frequency down to 30 Hz.

Solution : Apply KVL to V_{CC} to ground loop through 1 kΩ resistances and diodes.

$$\therefore \quad -I\,(1k\Omega) - 1.4 - I\,(1k\Omega) + 20 = 0$$

$$\therefore \quad 2\ k\Omega\ I = 18.6$$

$$\therefore \quad I = 9.3\ mA$$

Thus the voltages of bases of Q_1 and Q_2 can be calculated as,

i) Base of $Q_1 = 20 - I \times 1\ k\Omega = 20 - 9.3 = \mathbf{10.7\ V}$

Base of $Q_2 = I \times 1\ k\Omega = 9.3 \times 10^{-3} \times 1 \times 10^3 = \mathbf{9.3\ V}$

ii) This is single supply version hence while considering supply voltage V_{CC} for the amplifier calculations it should be considered as $V_{CC}/2$ i.e. 10 V and not 20 V.

Hence under maximum signal condition,

$$V_m = \frac{V_{CC}}{2} = 10\ V$$

$$\therefore \quad (P_{ac})_{max} = \frac{1}{2}\frac{V_{CC}^2}{R_L} = \frac{1}{2}\frac{(10)^2}{10}$$

$$= \mathbf{5\ W}$$

iii) $$P_{DC} = V_{CC}\ I_{CQ} \text{ where } I_{CQ} = I_{dc} = \frac{2I_m}{\pi}$$

and $$R_L = \frac{V_m}{I_m} \text{ hence } I_m = \frac{V_m}{R_L} = \frac{V_{CC}}{R_L}$$

$$\therefore \quad P_{DC} = V_{CC} \cdot \frac{2}{\pi} \cdot \frac{V_{CC}}{R_L} = \frac{2V_{CC}^2}{\pi R_L}$$

$$= \frac{2\times10^2}{\pi\times10} = 6.3661\ W$$

$$\therefore \quad \%\,\eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{5}{6.3661} \times 100 = \mathbf{78.54\ \%}$$

iv) The signal frequency $f = 30\ Hz$

Now $$f = \frac{1}{2\pi RC} \text{ and } R = R_L = 10\ \Omega$$

$$\therefore \quad C = \frac{1}{2\pi\times30\times10} = \mathbf{530.516\ \mu F}$$

Example 6.33 : *For a given input current $i_{in} = 50 \times 10^3 \sin 200t$, the output current given by a class A amplifier is*
$i_C = 2\times10^{-2} + 50\times10^{-2} \sin 200t + 10^{-4} \sin 400t + 3\times10^{-6} \cos 600t$.
Determine the distortion factor for it. (R.U. : May-2008)

Solution : $B_1 = 50 \times 10^{-2}$, $B_2 = 10^{-4}$, $B_3 = 3 \times 10^{-6}$

These are the amplitudes of various freuqency components.

$$\therefore \quad D_2 = \frac{|B_2|}{|B_1|} = \frac{10^{-4}}{50\times10^{-2}} = 2 \times 10^{-4}$$

$$\therefore \quad D_3 = \frac{|B_3|}{|B_1|} = \frac{3\times10^{-6}}{50\times10^{-2}} = 6 \times 10^{-6}$$

$$\therefore \quad \%\ D = \sqrt{D_2^2 + D_3^2} \times 100 = \sqrt{(2\times10^{-4})^2 + (6\times10^{-6})^2} \times 100$$

$$= \mathbf{0.02\ \%}$$

Example 6.34 : *A power transistor working in class A opertion is supplied from a 12 V battery. If the maximum collector current change is 100 mA, find the power transferred to a 5 Ω loudspeaker if it is,*

i) Directly connected in the collector
ii) Transformer coupled for maximum power transfer.
Find the turns ratio of the transformer in case (ii). (R.U. : 2003)

Solution : $V_{CC} = 12$ V, $I_{PP} = 100$ mA, $R_L = 5\ \Omega$

$$\therefore \quad I_m = \frac{I_{PP}}{2} = 50 \text{ mA}$$

i) $$P_{ac} = \frac{I_m^2 RL}{2} = \frac{(50\times10^{-3})^2 \times 5}{2} = \mathbf{6.25 \times 10^{-3}\ W}$$

ii) $$(P_{ac})_{max} = \frac{1}{2} \frac{V_{CC}^2}{R_L'} \qquad \ldots(1)$$

But $$P_{ac} = \frac{V_m I_m}{2} \text{ and } V_m = V_{CC} \text{ for maximum power}$$

$$\therefore \quad (P_{ac})_{max} = \frac{12\times50\times10^{-3}}{2} = 0.3 \text{ W}$$

$$\therefore \quad 0.3 = \frac{1}{2} \times \frac{(12)^2}{R_L'}$$

$$\therefore \quad R_L' = 240\ \Omega$$

But $$R_L' = \frac{R_L}{n^2} \quad \text{i.e. } 240 = \frac{5}{n^2}$$

$$\therefore \quad n^2 = 0.02083 \qquad \text{i.e. } n = 0.1443 = \frac{N_2}{N_1}$$

$$\therefore \quad \frac{N_1}{N_2} = \mathbf{6.928 : 1}$$

Example 6.35 : *For class A CE transistor amplifier, the operating point is located at $I_C = 250$ mA and $V_{CE} = 8$ V. Due to the input signal, the output collector current goes in between 450 mA and 40 mA while the V_{CE} swing between 15 V to 1 V. Find :*

i) The output power delivered *ii) The input power*

iii) The collector efficiency *iv) The power dissipated by transistor.*

(R.U. : 2002)

Solution : $I_{CQ} = 250$ mA, $V_{CEQ} = 8$ V

$V_{max} = 15$ V, $V_{min} = 1$ V, $I_{max} = 450$ mA, $I_{min} = 40$ mA

$\therefore \quad I_{PP} = I_{max} - I_{min} = 450 - 40 = 410$ mA

$\therefore \quad V_{pp} = V_{max} - V_{min} = 15 - 1 = 14$ V

$\therefore \quad V_m = \frac{V_{PP}}{2} = 7$ V and $I_m = \frac{I_{PP}}{2} = 205$ mA

i) $P_{ac} = \frac{V_m I_m}{2} = \frac{7 \times 205 \times 10^{-3}}{2} = \mathbf{0.7175\ W}$ ...Output power

ii) $P_{DC} = I_{CQ} V_{CEQ} = 250 \times 10^{-3} \times 8 = \mathbf{2\ W}$ ...Input power

iii) $\% \eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{0.7175}{2} \times 100 = \mathbf{35.875\ \%}$ ...Efficiency

iv) $P_d = P_{DC} - P_{ac} = 2 - 0.7175 = \mathbf{1.2825\ W}$ ... Power dissipation

Example 6.36 : *The signal power is to be delivered to a loudspeaker having a reistance of 4 Ω. The output transformer used in the power amplifier has a turns ratio of 20 : 1. The primary winding of transformer gets a.c. signal from a transistor which can be represented by a current source of 5 mA and shunt resistance of 8 k Ω. Calculate the power delivered to the loudspeaker when it is connected to the secondary of the transformer.* **(R.U. : 1998)**

Solution : The circuit diagram is shown in the Fig. 6.54.

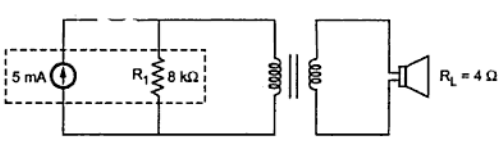


Fig. 6.54

$\therefore n = \frac{N_2}{N_1} = \frac{1}{20}$

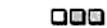
$\therefore R'_L = \frac{R_L}{n^2}$

$= \frac{4}{\left(\frac{1}{20}\right)^2}$

$= 1600\ \Omega$

11. *Explain with neat circuit diagram, the working of a transformer coupled class A power amplifier.*
12. *What is impedance transformation in case of a transformer ? Explain the procedure of calculating a reflected load on primary, for a step down transformer.*
13. *Prove that the maximum efficiency of a transformer coupled class A amplifier is 50 %.*
14. *Explain the advantages and disadvantages of directly coupled and transformer coupled class A amplifiers.*
15. *A power transistor operated in class A operation delivers a maximum of 6 W to a 8 Ω load with the supply voltage of 25 V. The Q point is adjusted for a symmetrical swing. Calculate,*
    a. Step down turns ratio b. Peak collector current c. Efficiency **(Ans. : 2.55 :1, 0.48 A, 50%)**
16. *What is harmonic distortion ? How the output signal gets distorted due to the harmonic distortion ?*
17. *What is the meaning of % harmonic distortion ? How the total harmonic distortion is calculated ?*
18. *Explain the three point method of calculating the second harmonic distortion.*
19. *What are the different possible distortions in an A.F. power amplifier ? Which is the most significant ? Why ?*
20. *A transistor used in A.F. power amplifier, working in class A operation supplies 0.8 W to 4 kΩ load. The zero signal d.c. collector current is 31 mA and the d.c. collector current with signal is 36 mA. Determine the % second harmonic distortion.* **(Ans. : 16.01 %)**
21. *Draw a neat circuit diagram of push pull class B amplifier. Explain its working.*
22. *Draw the circuit diagram of class B push pull amplifier and discuss*
    a. Its merits b. Cross-over distortion.
23. *Prove that the maximum power dissipation is approximately* $\frac{1}{5}$*th of the maximum a.c. output power, for a class B amplifier.*
24. *Show that the even harmonics are cancelled at the output of a push pull class B ideal amplifier.*
25. *A certain B amplifier delivers 10 W to the load. The output transformer efficiency is 85 %. A CRO connected across the load of 0.5 Ω in series with positive lead of the 24 V power supply shows a peak voltage of 500 mV. Determine the efficiency.* **(Ans. : 77 %)**
26. *Explain the working of complementary symmetry class B amplifier. What are its advantages?*
27. *Prove that the maximum efficiency of a class B amplifier is 78.5 %.*
28. *Derive the condition for maximum power dissipation for a class B amplifier. State the expression for maximum power dissipation.*
29. *A complementary symmetry class B amplifier supplied output to a load of 3 Ω from the supply voltage of 20 V. Calculate maximum power output, power output, power dissipation rating of each transistor.* **(Ans. :16.67 W, 3.38 W)**
30. *Compare complementary symmetry and push pull class B circuits.*

31. *What is cross-over distortion? Explain.*
32. *How the cross-over distortion in an A.F. power amplifier is eliminated ?*
33. *Draw and explain single supply version of complementary symmetry class B amplifier circuit*
34. *Draw and explain the complementary symmetry class B amplifier with a driver stage.*
35. *Draw and explain the operation of quasi-complementary push pull power amplifier.*
36. *Write a note on safe operating area for a transisor.*



A

Schmitt Trigger using Op-amp

A.1 Op-amp in Switching Circuits

The op-amp is basically a high gain differential amplifier. In open loop configuration, it has very high gain, of the order of 10^5. But op-amp has a saturable property, that it can produce maximum output equal to its supply voltages. Thus if supply voltages used for the op-amp, are $+ V_{CC}$ and $- V_{EE}$, then practically the output votlage saturates at the voltages $+ V_{sat}$ and $- V_{sat}$ given by,

$$+ V_{sat} \approx + V_{CC} - 1 \text{ V} \quad \text{and} \quad - V_{sat} \approx - V_{EE} + 1 \text{ V} \qquad \ldots(1)$$

Key Point : *Due to very high open loop gain, for very small change in input voltage, the op-amp output switches from* $+ V_{sat}$ *to* $- V_{sat}$ *or viceversa.*

Due to this property, the op-amp in open loop mode can be used as a basic comparator. When two inputs are applied to the open loop op-amp then it compares the two inputs. Depending on the comparison, it produces output voltage which is either $+ V_{sat}$ or $- V_{sat}$.

A.2 Basic Comparator using Op-amp

There are two types of op-amp comparator circuits namely,

1. Non-inverting comparator and 2. Inverting comparator

A.2.1 Basic Non-inverting Comparator

In this comparator, the input voltage is applied to the non-inverting terminal and no reference voltage is applied to other terminal. So inverting terminal is grounded. The input voltage is denoted as V_{in} while the voltage applied to other terminal with which V_{in} is compared is denoted as V_{ref}. In the basic comparator, $V_{ref} = 0$ V. The **basic non-inverting comparator** is shown in the Fig. A.1.

In the non-inverting comparator, if V_{in} is greater than V_{ref} then output is $+ V_{sat}$ i.e. almost equal to $+ V_{CC}$. While if V_{in} is less than V_{ref} then output is $- V_{sat}$ i.e. almost equal to $- V_{EE}$.

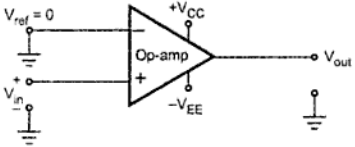


Fig. A.1 Basic non-inverting comparator

Thus for Fig. A.1, as $V_{ref} = 0$ V when V_{in} is positive then $V_o = + V_{sat} \approx + V_{CC}$ while when V_{in} is negative then $V_o = - V_{sat} \approx - V_{EE}$. This is because, as open loop gain op-amp (A_{OL}) is very very high even for very small V_{in} the op-amp output saturates.

Thus the two possible output levels of the comparator are $+ V_{sat}$ and $- V_{sat}$, indicating whether the input voltage is greater than or less than the reference voltage. Such type of the comparator, in which the operation is at saturation level is known as **saturating** type of comparator. Assuming symmetrical conditions, the two possible output levels of the saturating type comparator are $+ V_{sat}$ and $- V_{sat}$.

Note that no feedback is applied to the op-amp and it is operated in open loop conditions, because of which the op-amp is operating in saturating conditions.

The input and output waveforms for a basic non-inverting comparator, for sinusoidal input are shown in the Fig. A.2.

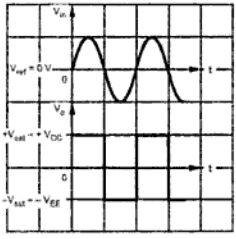


Fig. A.2 Waveforms of a basic non-inverting comparator

A.2.2 Basic Inverting Comparator

The Fig. A.3 shows the basic inverting comparator in which the input is applied to the inverting terminal while the reference voltage which is zero is applied to the non-inverting terminal. Thus if V_{in} is greater than V_{ref}, then the output is $-V_{sat}$, while if V_{in} is less than V_{ref} then the output $+V_{sat}$ due to inverting action.

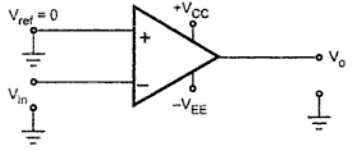


Fig. A.3 Inverting comparator

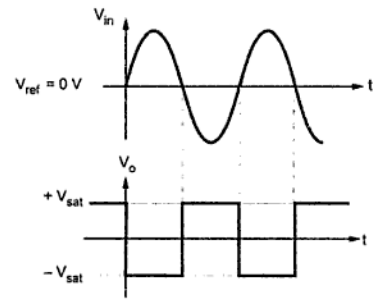


Fig. A.4 Waveforms of inverting comparator

The Fig. A.4 shows the waveforms of an inverting comparator.

In both the types of comparator, the output can be controlled as per the requirement by setting V_{ref} other than zero, by using a battery and potential divider circuit.

A.2.3 Limitations of Op-amp Comparator

In comparators, the op-amp is used in open loop mode. As open loop gain of op-amp is large, very small noise voltages also can cause triggering of the comparator, to change its state. Such a false triggering may cause lot of problems in the applications of comparator as zero crossing detector. This may give a wrong indication of zero crossing due to zero crossing of noise voltage rather than zero crossing of input wanted signal. Such unwanted noise causes the output to jump between high and low states. The comparator circuit used to avoid such unwanted triggering is called **regenerative comparator** or **Schmitt trigger**, which basically uses a positive feedback.

A.3 Inverting Schmitt Trigger

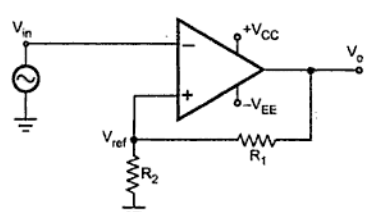


Fig. A.5 Inverting schmitt trigger

The Fig. A.5 shows the basic schmitt trigger circuit. As the input is applied to the inverting terminal, it is also called inverting schmitt trigger circuit. The inverting mode produces opposite polarity output. This is fedback to the non-inverting input which is of same polarity as that of output. This ensures positive feedback.

When V_{in} is slightly positive than V_{ref}, the output gets driven into negative saturation at $-V_{sat}$ level.

When V_{in} becomes more negative than $-V_{ref}$, then output gets driven into positive saturation at $+V_{sat}$ level.

Thus output voltage is always at $+V_{sat}$ or $-V_{sat}$ but the voltage at which it changes its state now can be controlled by the resistance R_1 and R_2. Thus V_{ref} can be obtained as per the requirement.

Now R_1 and R_2 forms a potential divider and we can write,

$$+V_{ref} = \frac{V_o}{R_1 + R_2} \times R_2 = \frac{+V_{sat}}{R_1 + R_2} \times R_2 \quad \text{.... positive saturation}$$

$$-V_{ref} = \frac{V_o}{R_1 + R_2} \times R_2 = \frac{-V_{sat}}{R_1 + R_2} \times R_2 \quad \text{.... negative saturation}$$

$+V_{ref}$ is for positive saturation when $V_o = +V_{sat}$ and is called upper threshold voltage denoted as V_{UT}. $-V_{ref}$ is for negative saturation when $V_o = -V_{sat}$ and is called lower threshold voltage denoted as V_{LT}. The values of these threshold voltage levels can be determined and adjusted by selecting proper values of R_1 and R_2.

Thus
$$V_{UT} = \frac{+V_{sat}\, R_2}{(R_1 + R_2)}$$

and
$$V_{LT} = \frac{-V_{sat}\, R_2}{(R_1 + R_2)}$$

The output voltage remains in a given state until the input voltage exceeds the threshold voltage level either positive or negative.

The Fig. A.6 shows the graph of output voltage against input voltage. This is called transfer characteristics of schmitt trigger.

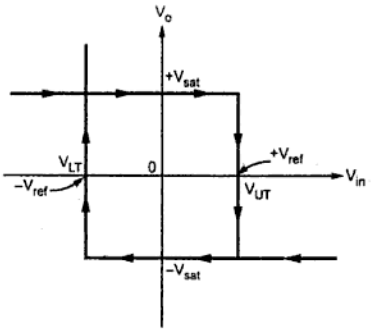


Fig. A.6 Hysteresis

A.4 Non-inverting Schmitt Trigger

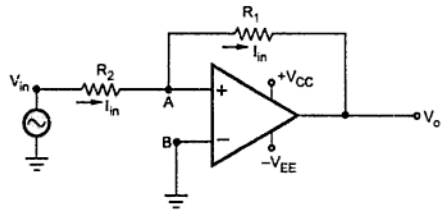


Fig. A.9 Non-inverting schmitt trigger

The Fig. A.9 shows the non-inverting schmitt trigger circuit. The input is applied to the non-inverting input terminal of the op-amp.

To understand the working of the circuit, let us assume that the output is positively saturated i.e. at $+V_{sat}$. This is fedback to the non-inverting input through R_1. This is a positive feedback.

Now though V_{in} is decreased, the output continues its positive saturation level unless and until the input becomes more negative than V_{LT}. At lower threshold, the output changes its state from positive saturation $+V_{sat}$ to negative saturation $-V_{sat}$. It remains in negative saturation till V_{in} increases beyond its upper threshold level V_{UT}. The transfer characteristics is shown in the Fig. A.10.

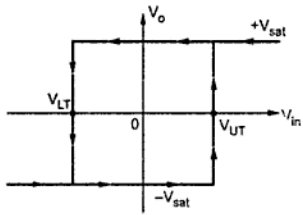


Fig. A.10 Hysteresis

Now V_A = Voltage at point A $= I_{in} R_2 = V_{UT}$

As op-amp input current is zero, I_{in} entirely passes through R_1.

$$\therefore \quad I_{in} = \frac{V_o}{R_1} = \frac{+V_{sat}}{R_1}$$

$$\therefore \quad V_{UT} = I_{in} R_2 = \frac{R_2}{R_1}(+V_{sat}) = V_{sat}\frac{R_2}{R_1}$$

and

$$V_{LT} = \frac{R_2}{R_1}(-V_{sat}) = -V_{sat}\frac{R_2}{R_1}$$

and

$$H = V_{UT} - V_{LT} = 2\,V_{sat}\frac{R_2}{R_1}$$

$$V_{UT} = \frac{+ V_{sat}\ R_2}{R_1 + R_2} = \frac{13.5 \times 120}{51 \times 10^3 + 120} = 0.03169 \text{ V}$$

$$V_{LT} = \frac{- V_{sat}\ R_2}{R_1 + R_2} = \frac{- 13.5 \times 120}{51 \times 10^3 + 120} = - 0.03169 \text{ V}$$

$$H = V_{UT} - V_{LT} = 0.03169 - (- 0.03169)$$

$$= 0.06338 \text{ V} = 63.38 \text{ mV}$$

Example A.3 : *For a non-inverting regenerative comparator shown in the Fig. A.13, calculate tripping voltages. Assume* $V_{sat} = \pm 13.5$ *V.*

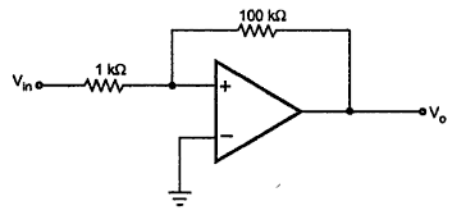


Fig. A.13

Solution : As input is applied to the non-inverting terminal, the circuit is non-inverting schmitt trigger.

$$R_1 = 100 \text{ k}\Omega, \qquad R_2 = 1 \text{ k}\Omega$$

$$\therefore \quad V_{UT} = + V_{sat} \frac{R_2}{R_1} = 13.5 \times \frac{1}{100} = 0.135 \text{ V}$$

$$V_{LT} = - V_{sat} \frac{R_2}{R_1} = \frac{- 13.5 \times 1}{100} = - 0.135 \text{ V}$$

A.5 Schmitt Trigger Applications

We have already seen one important application of Schmitt trigger as sine to square wave converter. It can be used to eliminate comparator chatter in signal shaping and in ON/OFF control. It is a building block of relaxation oscillators.

A.5.1 Schmitt Triggers for Eliminating Comparator Chatter

Chattering can be defined as production of multiple output transition as the input signal swings through the threshold region of a comparator. This happens due to the fact that a.c. noise is present in the practical circuits. Fig. A.14 shows input signal with a.c. noise and how comparator output chatters. Even if noise is very less, it takes a very small noise spike to cause chatter due to high comparator gains.

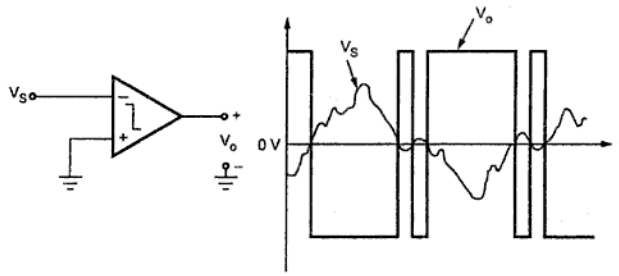


Fig. A.14

This problem can be solved by using schmitt trigger circuits. This is because they exhibit hysteresis. In case of hysteresis, as soon as the input signal crosses the present threshold level once, the output changes its state and activates the other threshold level, so that the input signal must swing back to the new threshold in order to make the output of the circuit to change its state again. Refer Fig. A.15. By making hysteresis width greater than the maximum peak amplitude of noise, a dead zone is created such that noise within this zone no longer causes multiple output transitions.

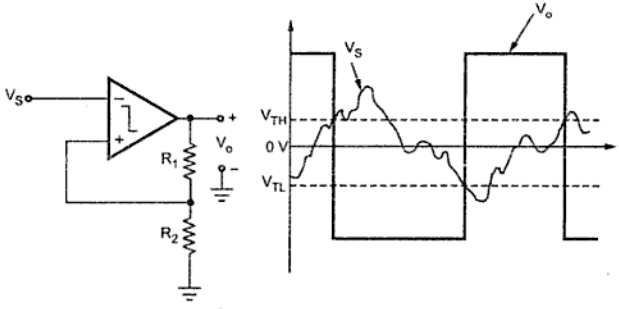


Fig. A.15

A.5.2 Schmitt Triggers in ON/OFF Controllers

In ON/OFF controller, such as temperature controller, when temperature is below setpoint heater is made ON and when it is above setpoint heater is made OFF. Now consider that temperature is just below the setpoint, and heater is ON. As soon as the temperature reaches the setpoint, the comparator which is controlling the heater makes it OFF. The smallest temperature drop following the heater OFF will make comparator to go in its activate state and switch on the heater. As a result, the heater will be cycled ON and OFF by the comparator at a rapid pace. This is not desirable.

two different values of V_1 can be obtained. Thus the circuit acts as a Schmitt trigger with different UTP and LTP levels. For designing such circuit, apply KVL to the output circuit, neglecting op-amp input current.

$$-IR_2 - IR_1 - x + V_o = 0$$

$$\therefore \quad I = \frac{V_o - x}{R_1 + R_2} \quad \ldots (1)$$

And $$V_1 = IR_1 + x \quad \ldots (2)$$

$$\therefore \quad V_1 = \frac{(V_o - x) R_1}{R_1 + R_2} + x \quad \ldots (3)$$

For $V_1 = V_{UT}$, $V_o = +V_{sat}$

$$\therefore \quad \boxed{V_{UT} = \frac{(+V_{sat} - x) R_1}{R_1 + R_2} + x} \quad \ldots (4)$$

For $V_1 = V_{LT}$, $V_o = -V_{sat}$

$$\therefore \quad \boxed{V_{LT} = \frac{(-V_{sat} - x) R_1}{R_1 + R_2} + x} \quad \ldots (5)$$

Subtracting equation (5) from (4),

$$\boxed{(V_{UT} - V_{LT}) = \frac{2V_{sat} R_1}{R_1 + R_2}} \quad \ldots (6)$$

This gives the relation between R_1 and R_2. Substituting $(R_1 + R_2)$ interms of R_1 in equation (4), the value of x can be obtained. Then by choosing R_1, the value of R_2 can be obtained.

Finally $$R_{comp} = R_1 || R_2$$

If value of 'x' is negative, it should be connected with opposite polarity in the circuit, compared to what is shown in the Fig. A.16.

Example A.4 : *Design an op-amp Schmitt trigger with the following specifications : UTP = 2 V, LTP = – 4 V and the output swings between ± 10 V. If input is 5 sin ωt, plot the waveforms of input and output.*

Solution : For the Schmitt trigger

$V_{UT} = 2$ V, $V_{LT} = -4$ V, $\pm V_{sat} = \pm 10$ V

For unequal UTP and LTP values, a modified circuit is required as shown in the Fig. A.17.

The voltage V_1 decides the UTP and LTP levels. Applying KVL to the output circuit and neglecting op-amp input current we can write,

$$-IR_2 - IR_1 - x + V_0 = 0$$

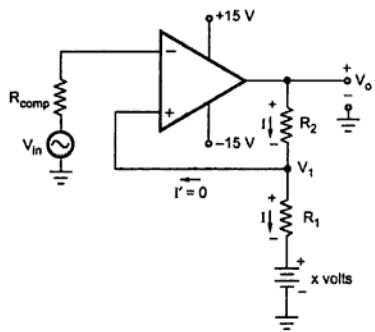


Fig. A.17

$$\therefore \quad I = \frac{V_0 - x}{R_1 + R_2} \qquad \ldots (7)$$

And $$V_1 = IR_1 + x \qquad \ldots (8)$$

$$\therefore \quad V_1 = \frac{V_0 - x}{R_1 + R_2} \cdot R_1 + x \qquad \ldots (9)$$

For $+V_{sat} = 10$ V,

$V_1 = V_{UT} = 2$V,

$V_0 = 10$ V

$$\therefore \quad 2 = \frac{10 - x}{R_1 + R_2} \cdot R_1 + x \qquad \ldots (10)$$

For $-V_{sat} = -10$ V,

$V_1 = V_{LT} = -4$V,

$V_0 = -10$ V

$$\therefore \quad -4 = \frac{-10 - x}{R_1 + R_2} \cdot R_1 + x \qquad \ldots (11)$$

Subtracting equation (11) and (10),

$$[2 - (-4)] = \frac{R_1}{R_1 + R_2}[10 - x + 10 + x]$$

$$\therefore \quad 6 = \frac{20\,R_1}{R_1 + R_2}$$

$$\therefore \quad R_1 + R_2 = 3.333 R_1 \qquad \ldots (12)$$

$$\therefore \quad R_2 = 2.333\,R_1 \qquad \ldots (13)$$

Substituting equation (13) in (10),

$$2 = \frac{(10 - x)\,R_1}{3.333\,R_1} + x$$

$$\therefore \quad 2 \times 3.333 = 10 - x + 3.333\,x$$

$$\therefore \quad 2.333\,x = -3.3334$$

$$\therefore \quad x = -1.4286$$

So actually polarity of the voltage source 'x' must be opposite to what is assumed earlier as shown in the Fig. A.17.

Choose $R_1 = 1\ k\Omega$ hence $R_2 = 2.333\ k\Omega$

$$\therefore \quad R_{comp} = R_1 \| R_2 = 0.7\ k\Omega$$

When the output is positive, D_1 gets forward biased and V_{UT} is the drop across R_2. When the output is negative, D_1 is reverse biased and only op-amp input current flows through R_2. Hence V_{LT} is almost zero.

The diode D_1 must be selected to have reverse breakdown voltage more than the supply voltage. Its reverse recovery time must be smaller than the minimum pulse width of the input signal.

$$t_{rr}(\text{for diode}) \leq \frac{\text{Minimum pulse width}}{10} \quad \ldots (14)$$

Using two diodes and two resistors as shown in the Fig. A.19 (b) different UTP and LTP levels can be selected. When the output is positive D_1 is forward biased while when the output is negative D_2 is forward biased.

$$\therefore \quad \text{UTP} = V_{UT} = \frac{[|V_o| - V_F] \times R_2}{R_1 + R_2} \quad \ldots (15)$$

$$\text{And} \quad \text{LTP} = V_{LT} = \frac{[|V_o| - V_F] \times R_2}{R_2 + R_3} \quad \ldots (16)$$

Where V_F is the forward voltage drop of D_1.

Review Questions

1. *In what mode op-amp is used as comparator ? Why ?*
2. *Explain the operation of inverting comparator using op-amp.*
3. *Explain the operation of non-inverting comparator using op-amp.*
4. *What is the need of op-amp Schmitt trigger circuit over comparator ?*
5. *Compare Schmitt trigger circuit with comparator.*
6. *Draw and explain the operation of op-amp inverting Schmitt trigger circuit.*
7. *Draw and explain the operation of op-amp non-inverting Schmitt trigger circuit.*
8. *Design an inverting Schmitt trigger to have trigger voltages ± 3 V. Use op-amp 741 with ± 12 V supply.*
9. *Explain the Schmitt trigger applications.*
10. *Draw and explain the operation of op-amp Schmitt trigger with different UTP and LTP levels.*

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Analog Electronics

✎ **Chapterwise University Questions with Answer**

1 Feedback Amplifiers

Q.1 *Draw the equivalent circuit of the following amplifier and show that the output resistance with load resistance, R_L with feedback is :*

$$R'_{of} = \frac{R_L[r_d + (\mu + 1)R]}{r_d + R_L(\mu + 1)R}$$

(2007)

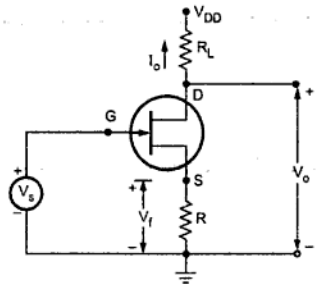

Fig. 1

Ans. : Refer section 1.12.2.

Q.2 *Define the following :*

i) Amount of feedback (in dB) ii) Desensitivity iii) Loop gain. **(2007)**

Ans. : Refer section 1.6.

Q.3 *The circuit of given Fig. 2 has the following parameters*

$R_c = 4\ K,\ h_{ie} = 1.1\ K,\ R' = 40\ K,\ h_{fe} = 50$

$R_s = 10\ K,\ h_{re} = h_{oe} = 0$

Find : a) A_{Vf} b) R_{if} c) R'_{of} **(2007)**

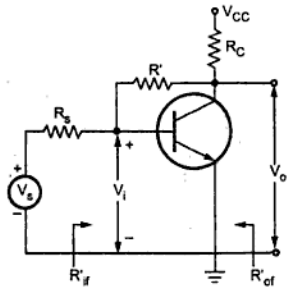

Fig. 2

Ans. : Refer section 1.12.4.

Q.4 *Write short note on topologies of negative feedback amplifier.* **(2002, 2003, 2007)**

Ans. : Refer section 1.5.

Q.5 *Calculate the input resistance and output resistance for a current-shunt feedback amplifier.* **(2006)**

Ans. : Refer section 1.9.

Q.6 *List major advantages of negative feedback. What are the four possible topologies of a feedback amplifier ? Identify the output signal X_o and feedback signal X_f for each topology (either as current or voltage). Also give dimensions of transfer given for each topology.* **(2006)**

Ans. : Refer sections 1.4 and 1.5.

Q.7 *An amplifier with an open loop voltage gain of 1,000 delivers 10 W of output power at 10 percent harmonic distortion when the input signal is 10 mV. If 40 dB negative voltage series feedback is applied and the output power is to remain at 10 W. Determine required input signal.* **(2006)**

As. : Refer example 1.5.

Q.8 *The transistor in the feedback amplifiers are identical and their h parameters are assumed to be standard. Calculate*

$R_{if} = V_s / I_i$, $A_{if} = I_o / I_i$, $A_{of} = V_o / V_i$, $A_{of} = V_o / V_s$ *and* R'_{of} **(2005)**

Q.11 *List the merits and demerits of negative feedback amplifiers.* **(2004)**

Ans. : Refer section 1.4.

Q.12 *Explain the effect of negative feedback on gain and frequency response of an amplifier with the help of suitable diagram.* **(2003)**

Ans. : Refer sections 1.6 and 1.7.

Q.13 *An amplifier has a voltage gain of 40. The amplifier is now modified to provide a 10 % negative feedback in series with the input. Calculate : i) Voltage gain with feedback ii) Amount of feedback in dB iii) Loop gain.* **(2003)**

Ans. : Given $A_v = 40$, $\beta = 10\ \% = 0.1$

i) $$A_{vf} = \frac{A_v}{1 + A_v \beta} = \frac{40}{1 + (40 \times 0.1)} = 8$$

ii) Amount of feedback in dB $= 20 \log \left| \frac{1}{1 + A\beta} \right|$

$$= 20 \log \left| \frac{1}{1 + (40 \times 0.1)} \right|$$

$$= -13.98 \text{ dB}$$

iii) Loop gain $= -A\beta = -40 \times 0.1 = -4$

Q.14 *Calculate the voltage gain with and without feedback for the given circuit with values of $g_m = 5$ ms, $R_D = 5.1$ kΩ, $R_s = 1$ kΩ and $R_f = 20$ kΩ.* **(1995, 2002)**

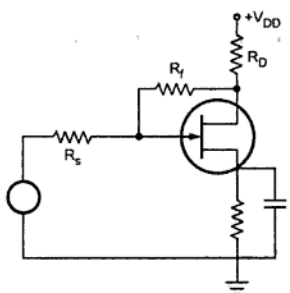

Fig. 5

Ans. : i) Voltage gain without feedback $= -g_m R_D$

$$= -5 \times 10^{-3} \times 5.1 \times 10^3$$

$$= -25.5$$

ii) Voltage gain with feedback

Step 1 : Identify topology

By making $V_o = 0$, feedback current becomes zero. Hence it is a voltage sampling. The feedback is fed in shunt with the input signal and thus the topology is voltage shunt feedback.

Step 2 and Step 3 : Find input and output circuit.

To find input circuit, set $V_o = 0$. This places resistor R_f across the input. To find output circuit, set $V_i = 0$. This places resistor R_f across output. The resultant circuit is shown in Fig. 6.

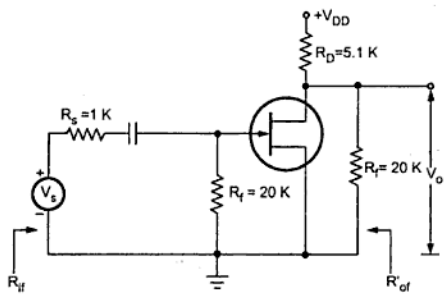

Fig. 6

Step 4 : Replace FET with its equivalent circuit

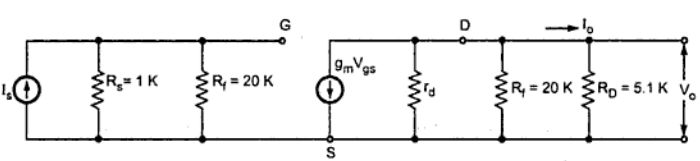

Fig. 7

Step 5 : Find open loop transresistance

$$R_M = \frac{V_o}{I_s} = \frac{-g_m V_{gs} R_{eff}}{I_s}$$

$$R_{eff} = r_d \parallel R_f \parallel R_D \quad \text{assuming } r_d = 40 \text{ K}$$

$$= 40 \text{ K} \parallel 20 \text{ K} \parallel 5.1 \text{ K}$$

$$= 3.689 \text{ K}$$

$$V_{gs} = I_s R_i = I_s \times R_s \parallel R_f$$

$$= I_s \times 1 \text{ K} \parallel 20 \text{ K}$$

$$= 952.38 \, I_s$$

$$\therefore \quad R_M = \frac{-5\times10^{-3} \times 952.38 \, I_s \times 3.689\times10^3}{I_s}$$

$$= -17.567 \text{ K}$$

Step 6 : Calculate β

$$\beta = -\frac{1}{R}$$

$$= -\frac{1}{20\times10^3} = -5 \times 10^{-5}$$

Step 7 : Calculate D, R_{Mf} and A_{Vf}

$$D = 1 + \beta R_M$$

$$= 1 + (-5 \times 10^{-5})(-17.567 \times 10^3)$$

$$= 1.878$$

$$R_{Mf} = \frac{R_M}{D} = \frac{-17.567\times10^3}{1.878}$$

$$= -9.354 \text{ K}$$

$$A_{Vf} = \frac{R_{Mf}}{R_s} = \frac{9.354\times10^3}{1\times10^3}$$

$$= -9.354$$

Q.15 *Derive expression for output resistance in voltage series feedback amplifier.* **(2002)**

Ans. : Refer section 1.9.

Q.16 *An amplifier has a gain of 60 dB (voltage gain). It has an output impedance of $Z_o = 12\,k\Omega$. It is required to modify its output impedance to 600 Ω by applying negative feedback. Calculate the value of feedback factor β. Also find the percentage change in overall gain $\frac{dA_f}{A_f}$ for 10 % change in the gain of internal amplifier $\frac{dA}{A}$.* **(2002)**

2 Oscillators

Q.1 *Draw the circuit diagram of a Colpitt oscillator and obtain the expression for frequency of oscillation and minimum gain of the transistor.* **(1994)**

Ans. : Refer section 2.10.

Q.2 *It is desired to design phase shift oscillator using FET having $g_m = 5000\ \mu S$, $r_d = 40\ k\Omega$ and feedback circuit value of $R = 10\ k\Omega$. Select the value of C and R_D to have the frequency of operation as 1 kHz and $A > 29$.* **(1995)**

Ans. : Refer example 2.33.

Q.3 *Draw the circuit and explain the working of series operated crystal oscillator.* **(1995)**

Ans. : Refer section 2.14.

Q.4 *Draw the circuit equivalent of a crystal and obtain expression for the reactance, prove that -*

$$\omega_\phi = 1 + \frac{1}{2}\frac{C_s}{C_\phi}$$

where ω_ϕ = Parallel resonant frequency

ω_s = Series resonant frequency

C_s = Series capacitance

C_ϕ = Parallel capacitance **(1995, 1997)**

Ans. : Refer example 2.30.

Q.5 *For the FET oscillator shown below, find -*

i) $\frac{V_f}{V_0}$ ii) The frequency of oscillations

iii) The minimum gain of the source follower required for oscillator.

(1997, 2001, 2002)

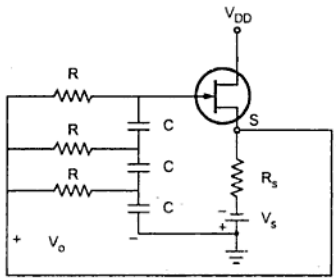

Fig. 1

Ans. : Refer section 2.5.8.

Q.6 *The oscillator circuit is shown in the Fig. 2.*

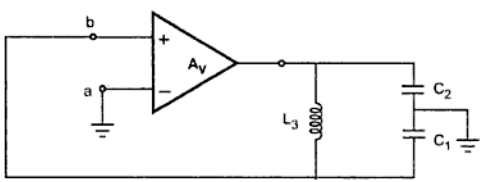

Fig. 2

a) If the inductance coil L_3 has the internal resistance r_3 and is taken into account, show that the frequency of oscillations is given by,

$$\omega^2 = \frac{1}{L_3}\left[\frac{1}{C_1}+\frac{1}{C_2}\left(1+\frac{r_3}{R_o}\right)\right]$$

b) If $\frac{r_3}{R_o} << 1$, show that the minimum amplifier gain required for the oscillations is,

$$A_V = \frac{C_1}{C_2}+\frac{C_2+C_1}{L_3}r_3R_o$$

(1998)

Ans. : Refer example 2.35.

Q.7 *Explain a generalised resonant circuit oscillator. How is its resonant frequency controlled by external circuit element ? Under what conditions is such an oscillator called Colpitts oscillator ?* **(2000)**

Ans. : Refer sections 2.8 and 2.10.

Q.8 *Explain how amplitude and frequency stability are improved in an oscillator ?* **(2001)**

Ans. : Refer sections 2.13 and 2.15.

Q.9 *Give the two Barkhausen conditions required in order for sinusoidal oscillations to be sustained and state the frequency stability criterion for a sinusoidal oscillator.* **(2001, 2002)**

Ans. : Refer sections 2.3 and 2.13.

Q.10 *Write short note on RC phase shift oscillator.* **(2001, 2005)**

Ans. : Refer section 2.5

Q.11 *Draw the circuit BJT Wien-bridge oscillator and explain the working.* **(2002)**

Ans. : Refer section 2.6.2.

Q.12 *Write short note on "Crystal oscillators".* **(2002, 2007)**

Ans. : Refer section 2.14.

Q.13 *Calculate the :*

i) Operating frequency; and

ii) Feedback fraction for the oscillator as shown below and the mutual inductance of the coils is 20 μH. **(2003, 6 Marks)**

Also mention the name of oscillator.

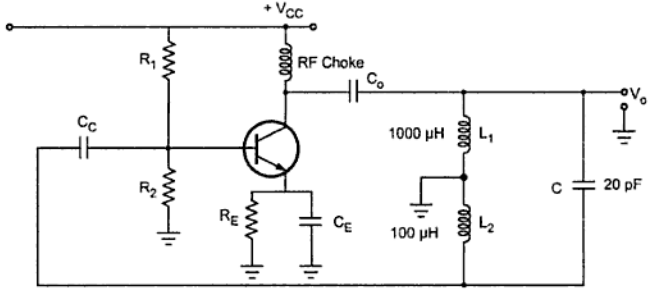

Fig. 3

Ans. : Refer example 2.32.

Q.14 *Prove that the ratio of the parallel to series resonant frequencies of crystal is approximately given by,*

$$\frac{f_p}{f_s} \cong \left(1 + \frac{C}{2C_M}\right) \text{ where } C_M = \text{Mounting capacitance.}$$

(2004)

Ans. : Refer example 2.30.

Q.15 *If C = 0.04 pF and C_M = 2 pF then by what percent does the parallel resonant frequency exceed the series resonant frequency ?* **(2003)**

Ans. : Refer example 2.31.

Q.16 *Write a short note on Wien bridge oscillator.* **(2004, 2005)**

Ans. : Refer section 2.6.

Q.17 *Prove that for a Wien bridge oscillator the gain of amplifier should equal to δ i.e. deviation where δ > 3. Also derive expression for frequency of oscillation with suitable diagrams.* **(2005)**

Ans. : Refer section 2.6.1.

Q.18 *A Hartley oscillator having the following parameters, L_1 = 500 μH, L_2 = 5000 μH, M = 300 μH, C = 150 pF. Find the frequency of oscillations.* **(2006)**

Ans. : Refer section 2.28.

Q.19 *The parameters of a crystal oscillator equivalent circuit are L_s = 0.8 H, C_s = 0.08 pF, R_s = 5 kΩ and C_M = 1 pF. Determine the resonating frequencies f_s and f_p.* **(2007)**

Ans. : Refer example 2.29.

Q.20 *Design a phase shift oscillator using FET of op-amp., to work with 2 kHz frequency. Assume that input resistance without feedback is very high.* **(May-2008, 8 Marks)**

Ans. : Refer example 2.36.

Q.21 *What is name of following oscillator, explain its working and calculate the value of inductance (L) offered by the crystal at oscillation frequency f_s = 1 MHz.*

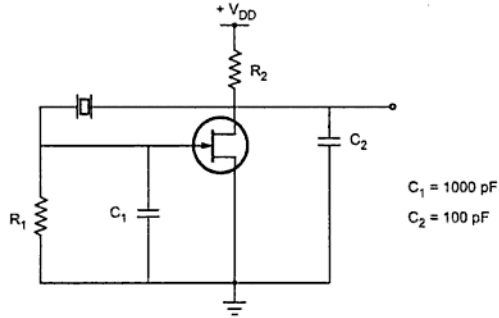

Fig. 4

If crystal has bulk resistance R_s = 700 Ω then draw its electrical equivalent circuit with component values. **(May-2008, 8 Marks)**

Ans. : Refer example 2.34.

Q.22 *Explain frequency response of crystal and give formulas for f_s and f_p.* **(2003, 2005; 6 Marks)**

Ans. : Refer section 2.14.

Q.25 *Verify the following inequality :*

$h_{fe} > 4K + 23 + 29K$

where $K = R_C/R$

R_C = *Collector resistance*

R = *Resistance of frequency selective network in a RC phase shift oscillator.* **(2005)**

Ans. : Refer section 2.5.4.

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3 Multivibrators and Blocking Oscillators

Q.1 *Discuss the working of a transistorized (BJT) biastable multivibrator.* **(1999)**

Ans. : Refer section 3.3.

Q.2 *Write short note on Schmitt trigger.* **(1999, 2002, 2005, 2007)**

Ans. : Refer section 3.9.

Q.3 *Draw the circuit for the astable multivibrator and explain its operation.* **(2001, 2002)**

Ans. : Refer section 3.7.

Q.4 *Write short note on blocking oscillator.* **(2003, 2006, 2007)**

Ans. : Refer section 3.12.

Q.5 *Explain the working of monostable multivibrator with required waveform, also derive expression for gate width.* **(2006)**

Ans. : Refer section 3.4.

Q.6 *Calculate the stable state voltages and currents I_{C1}, I_{C2}, I_{B1}, I_{B2}, V_{B1}, V_{B2}, V_{C1} and V_{C2} for the following circuit of bistable multivibrator where $V_{BE(sat)} = 0.7$ V, $V_{CE(sat)} = 0.15$ V.* **(2007)**

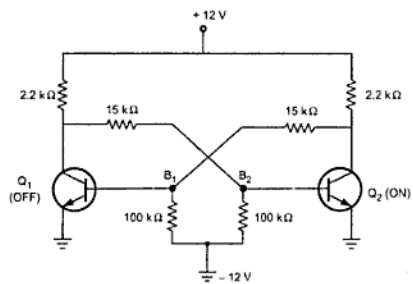

Fig. 1

Ans. : Refer example 3.16.

Q.7 *Describe the working of a monostable multibrator with the help of suitable circuit diagram using BJT and also show the waveforms at various points and expression for time width.* **(2008)**

Ans. : Refer section 3.5.

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4 High Frequency Amplifiers

Q.1 *Draw the hybrid-π model for a transistor in CE configuration and briefly describe origin of components. Comment on the validity of model.* **(1994,** 1995, 1998, 2000, 2003)

Ans. : Refer sections 4.2 and 4.5.

Q.2 *Given the following transistor measurements made at I_c = 5 mA, V_{CE} = 10 V and at room temperature h_{fe} = 100, h_{ie} = 600 Ω, A_{ie} = 10 at 10 MHz, C_c = 3 pF.*

Find f_β, f_T, C_e, $r_{b'e}$ and $r_{bb'}$. (1995, 2005)

Ans. : Refer example 4.21.

Q.3 *Draw a small signal high frequency emitter follower model of a transistor and derive an expression for its high frequency voltage gain.* (1999, 2002, 2005, 2007)

Ans. : Refer section 4.9.2.

Q.4 *Derive the expressions for hybrid-π parameters of transistor interms of CE h-parameters.*

(2001, 2002)

Ans. : Refer section 4.3.

Q.5 *Consider of CE stage with a resistive load R_L, using Miller's theorem, what is the midband input capacitance and high 3 dB frequency f_H for the current gain.*

(2001, 2002)

Ans. : Refer section 4.7.2.

Q.6 *Given that h_{fe} = 50, h_{oe} = 24 μA/V. Find out g_m and $g_{b'e}$ at I_c = 1.3 mA and room temperature.* (2002)

Ans. : Refer example 4.22.

Q.7 *Write short note on gain-bandwidth product.* (2002)

Ans. : Refer section 4.8.

Q.8 *In a hybrid-π model, prove that diffusion capacitance at emitter junction -*

$$C_{de} = g_m \frac{W^2}{2D_B}$$

where g_m = *Transistor transconductance*

W = *Base width*

D_B = *Diffusion constant for minorities in base.* **(2003, 2007)**

Ans. : Refer section 4.4.

Q.9 *Draw the high frequency equivalent circuit of an emitter follower and derive the expression of upper cut-off frequency, f_H for the same.* **(2003, 2006)**

Ans. : Refer section 4.9.

Q.10 *Derive the expression for CE short circuit current gain as a function of frequency. Define f_β and f_T. Also find relation between f_β and f_T.* **(2004)**

Ans. : Refer section 4.7.1.

Q.11 *Derive the expression of the CE short circuit current gain A_i as a function of frequency. Define f_β and f_T. What is the relationship between f_β and f_T ?* **(2005, 2007)**

Ans. : Refer section 4.7.

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6 Power Amplifiers [Large Signal Amplifiers]

Q.1 *Find an expression for the second harmonic distribution factor of the collector current of a BJT (Bipolar junction transistor) amplifier interms of experimentally measured values I_{Cmax}, I_{Cmin} and I_{CQ} for an amplifier driven by a base current $i_b = i_{bm} \cos \omega t$.* **(1994)**

Ans. : Refer section 6.9.

Q.2 *Why is tuned amplifier operated in class C operation ?* **(1995)**

Ans. : Refer section 6.3.3.

Q.3 *Discuss the advnatages of a push pull amplifier in class B operation.* **(1998)**

Ans. : Refer section 6.11.9.

Q.4 *Signal power is to be delivered to a loudspeaker having a resistance of 4 Ω. The output transformer used in the power amplifier has a turns ratio of 20 : 1. The primary winding of transformer gets a.c. signal from a transistor which can be represented by a current source of 5 mA and shunt resistance of 8 kΩ. Calcualte the power delivered to the loudspeaker when it is connected to the secondary of the transformer.* **(1998)**

Ans. : Refer example 6.36.

Q.5 *Give the circuit of a transformer coupled single transistor output stage and explain the need of matching the impedance.* **(2000)**

Ans. : Refer section 6.8.

Q.6 *What is meant by cross-over distortion in class B amplifier ? Explain how it is overcome in class AB operation ?* **(2002)**

Ans. : Refer section 6.16.

Q.7 *For class A CE transistor amplifier, the operating point is located at I_c = 250 mA and V_{CE} = 8 V. Due to input signal the output collector current goes in between 450 mA and 40 mA. The V_{CE} swings between 15 V and 1 V. Find :*

i) The output power delivered, ii) The input power, iii) Collector efficiency

iv) Power dissipated by the transistor. **(2002)**

Ans. : Refer example 6.35.

Q.8 *Draw the diagram of a class A amplifier, find the expression for the power. What is the cause of harmonic distortion ?* **(2002)**

Ans. : Refer section 6.7.

Q.9 *Write short note on push pull amplifier.* **(2002)**

Ans. : Refer section 6.11.

Q.10 *For a series fed class A large signal amplifier. Draw the output characteristics and the current and votlage waveforms. Derive expression for output power.* **(2002, 2004)**

Ans. : Refer section 6.7.

Q.11 *Define conversion efficiency, compare maximum efficiency of a series fed and transformer coupled class A signal transistor power stage.* **(2002, 2004)**

Ans. : Refer section 6.7.

Q.12 *Explain the operation of a class B push pull power amplifier with a neat circuit diagram and waveforms. Determine its collector efficiency. What is cross-over distortion and how do you eliminate it in the above power amplifier ?* **(2002, 2005)**

Ans. : Refer section 6.11.

Q.13 *Show that optimum conversion efficiency possible in calss B push pull amplifier is 78.5 % and also explain the main drawback of class B configuration in power amplifier.* **(2003)**

Ans. : Refer section 6.11.

Q.14 *A power transistor working in class A opertion is supplied from a 12 V battery. If the maximum collector current change is 100 mA, find the power transferred to a 5 Ω loudspeaker if it is,*

i) Directly connected in the collector
ii) Transformer coupled for maximum power transfer.
Find the turns ratio of the transformer in case (ii). **(2003)**

Ans. : Refer example 6.34.

Q.15 *List major difference between small signal and large signal amplifiers.* **(2004)**

Ans. : Refer section 6.2.

Q.16 *Prove that the maximum efficiency of transformer feed class A power amplifier will be 50 %.* **(2004)**

Ans. : Refer section 6.8.

Q.17 *Draw only circuit diagram of transformer less class B push pull amplifier.* **(2004)**

Ans. : Refer section 6.12.

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