ΤΕΧΝΙΚΕΣ ΑΥΞΗΣΗΣ ΤΗΣ ΑΠΟΔΟΣΗΣ ΤΩΝ ΥΠΟΛΟΓΙΣΤΩΝ ΙΙ

Multiprogramming

In a multiprogramming system there are one or more programs loaded in main memory which are ready to execute. Only one program at a time is able to get the CPU for executing its instructions (i.e., there is at most one process running on the system) while all the others are waiting their turn.

The main idea of multiprogramming is to maximize the use of CPU time. Indeed, suppose the currently running process is performing an I/O task Then, the OS may interrupt that process and give the control to one of the other in-main-memory programs that are ready to execute (i.e. *process context switching*).

Multiprocessing

Multiprocessing sometimes refers to executing multiple processes (programs) at the same time. In fact, multiprocessing refers to the *hardware* (i.e., the CPU units) rather than the *software* (i.e., running processes). If the underlying hardware provides more than one processor then that is multiprocessing. Several variations on the basic scheme exist, e.g., multiple cores on one die or multiple dies in one package or multiple packages in one system.

Anyway, a system can be both multiprogrammed by having multiple programs running at the same time and multiprocessing by having more than one physical processor.

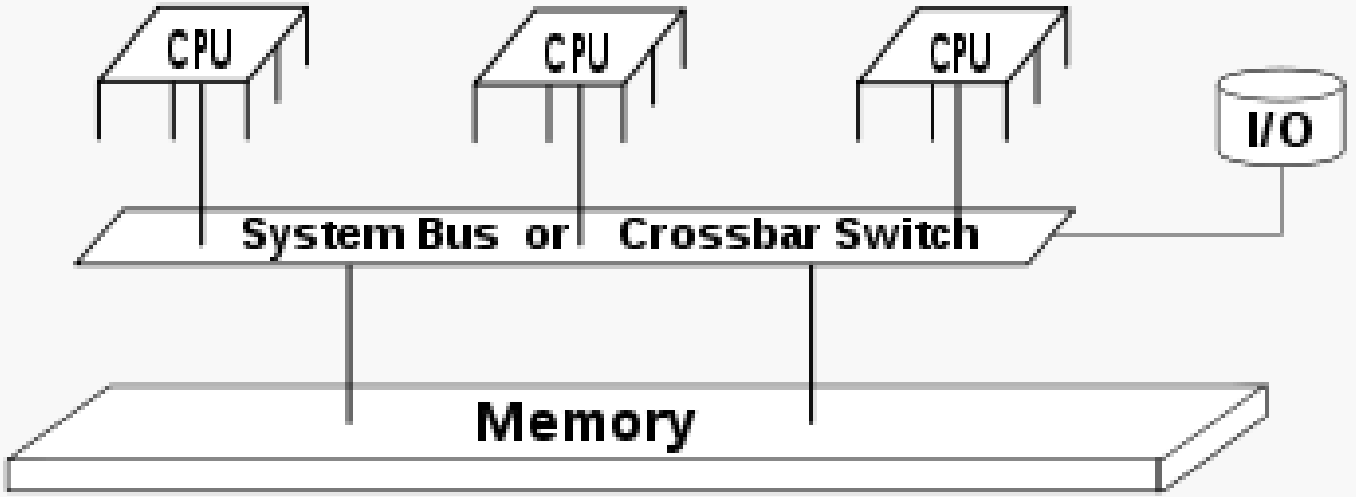
context switching

In computing, a **context switch** is the process of storing the state of a process or of a thread, so that it can be restored and execution resumed from the same point later. This allows multiple processes to share a single CPU, and is an essential feature of a multitasking operating system.

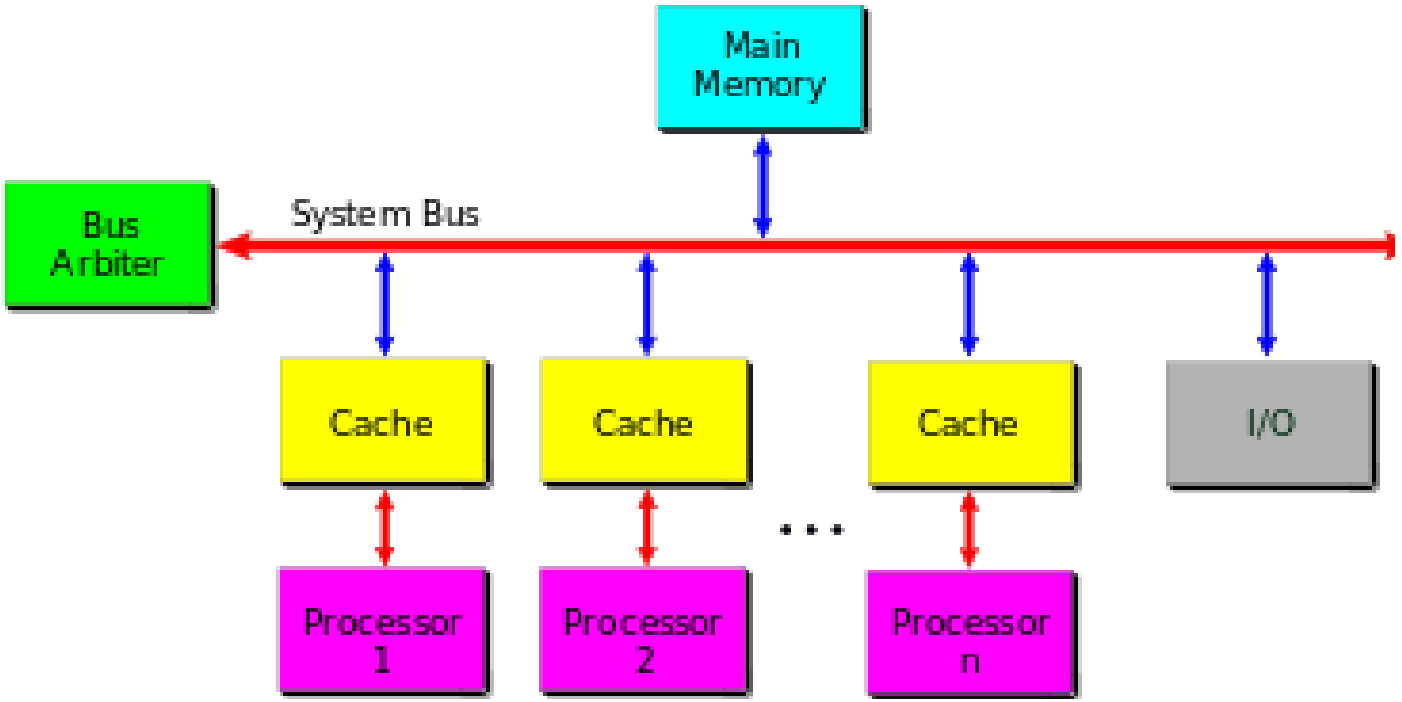
Συστήματα SMP

Ένα υπολογιστικό σύστημα με *αρχιτεκτονική συμμετρικής πολυεπεξεργασίας* (*symmetric multiprocessing* ή SMP) μπορεί να ορισθεί σαν ένα αυτοδύναμο υπολογιστικό σύστημα που περιλαμβάνει δύο ή περισσότερους όμοιους επεξεργαστές που μοιράζονται την ίδια κύρια μνήμη.
Το σύστημα λειτουργεί κάτω από ένα ενιαίο λειτουργικό σύστημα που εξασφαλίζει την συνεργασία των επεξεργαστών.
Σαν *σύστημα διασύνδεσης* χρησιμοποιούνται δίαυλοι (buses), crossbar switches. Στα συστήματα SMP υπάρχουν περιορισμοί στην επεκτασιμότητα που οφείλονται στο bandwidth και την κατανάλωση ισχύος του συστήματος διασύνδεσης μεταξύ των επεξεργαστών, της μνήμης, των διατάξεων δίσκων και των μονάδων εισόδου/εξόδου.

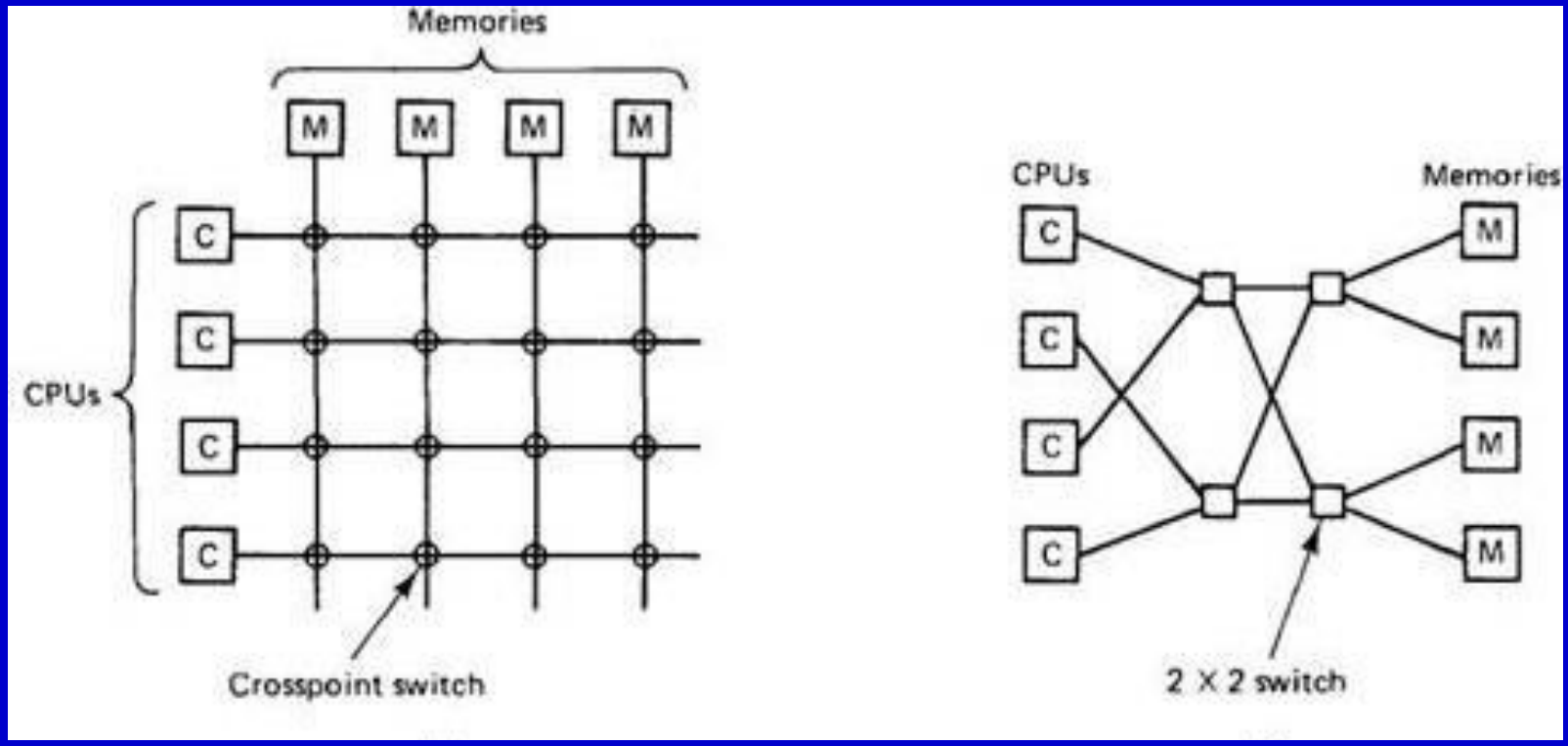
Αρχιτεκτονική συστημάτων SMP

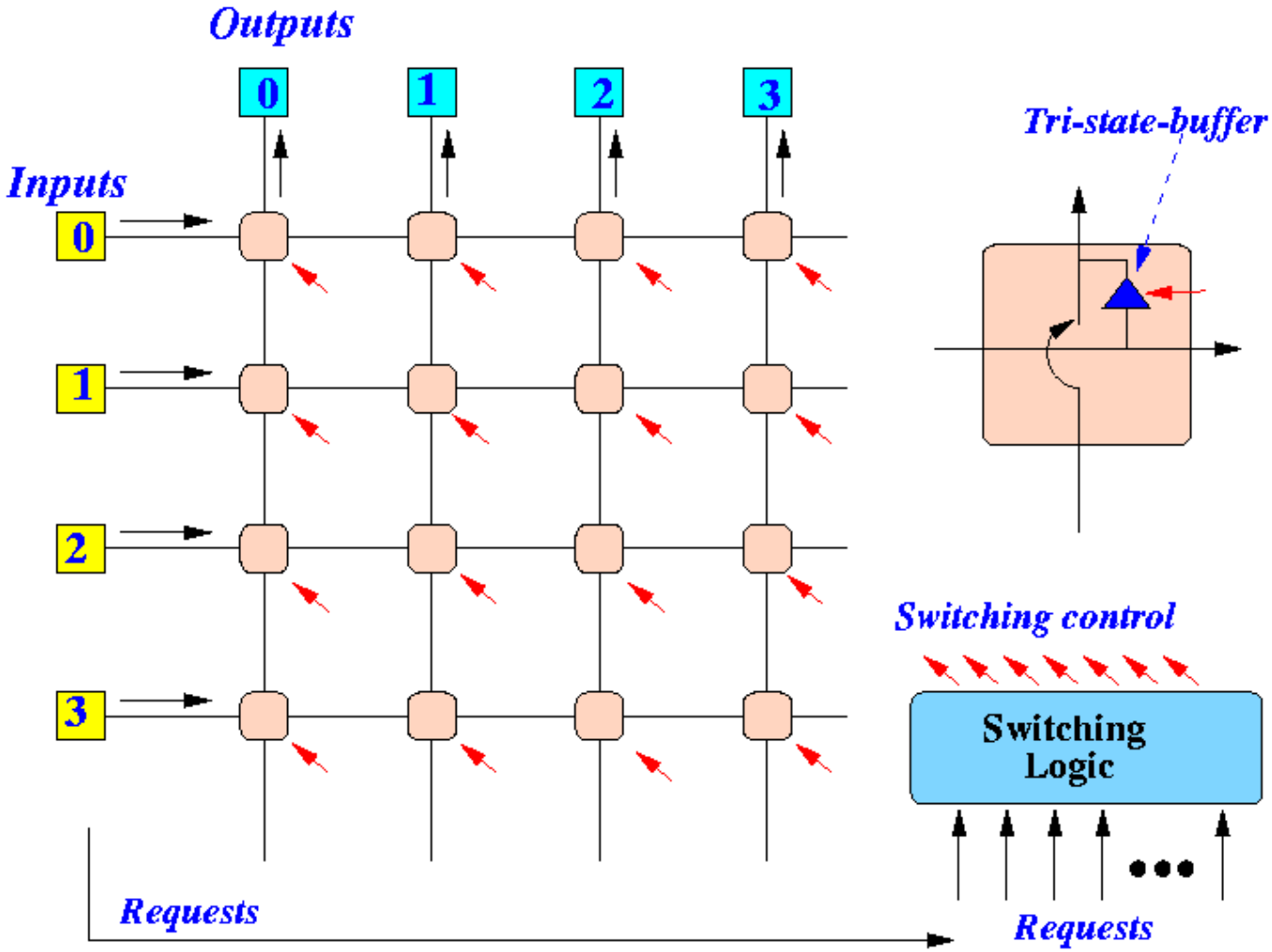


Σύστημα SMP με κοινό δίαυλο



Σύστημα SMP με crossbar switch



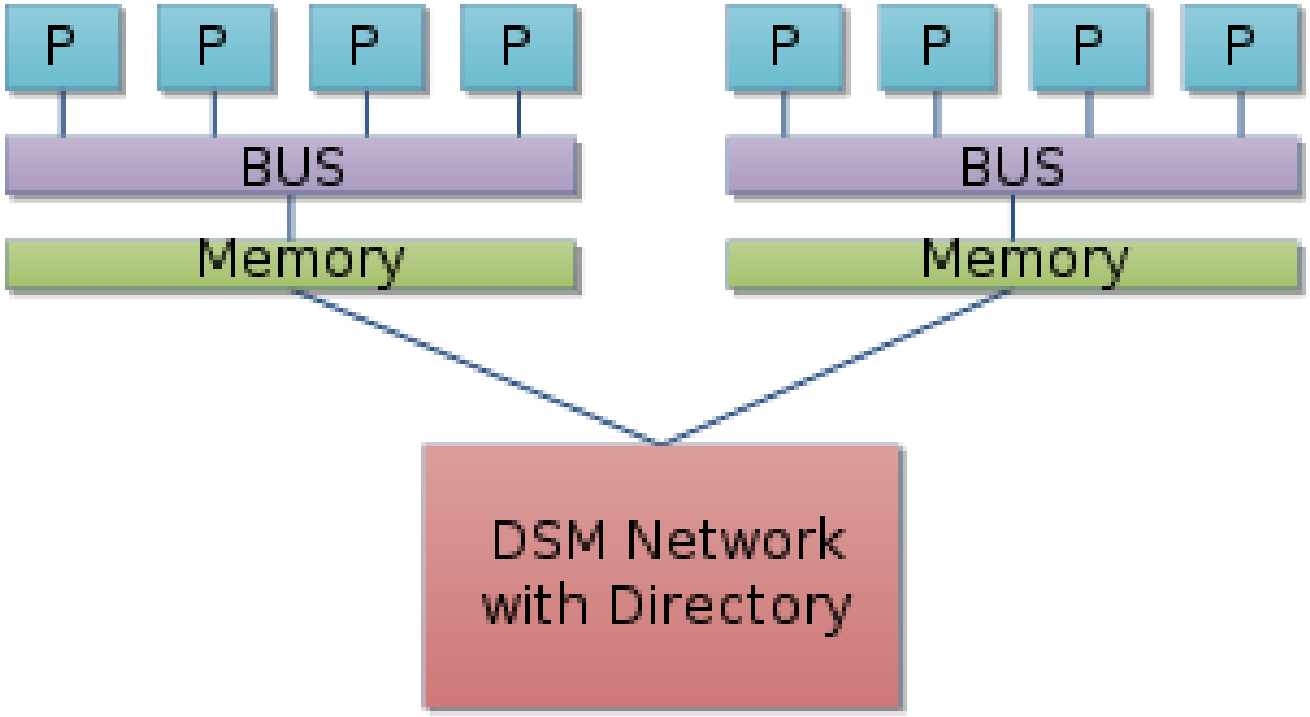

Outputs
0
1
2
3
Inputs
0
1
2
3
Requests
Tri-state-buffer
Switching control
Switching
Logic
Requests

Αρχιτεκτονική NUMA

Στα συστήματα SMP υπάρχει περιορισμός στον αριθμό των επεξεργαστών που μπορεί να διαθέτει το κάθε υπολογιστικό σύστημα. Μια προσέγγιση στο να επιτευχθεί μεγάλης κλίμακας πολυεπεξεργασία και να διατηρηθούν τα χαρακτηριστικά της αρχιτεκτονικής SMP είναι η NUMA (Non Uniform Memory Architecture).

Τα συστήματα με αρχιτεκτονική NUMA είναι αυτόνομα υπολογιστικά συστήματα στα οποία οι επεξεργαστές έχουν προσπέλαση σε όλα τα τμήματα της κύριας μνήμης χρησιμοποιώντας απλές εντολές γλώσσας μηχανής (load, store, move, …). Ο χρόνος προσπέλασης της μνήμης όμως εξαρτάται από το τμήμα της μνήμης στο οποίο γίνεται η προσπέλαση.

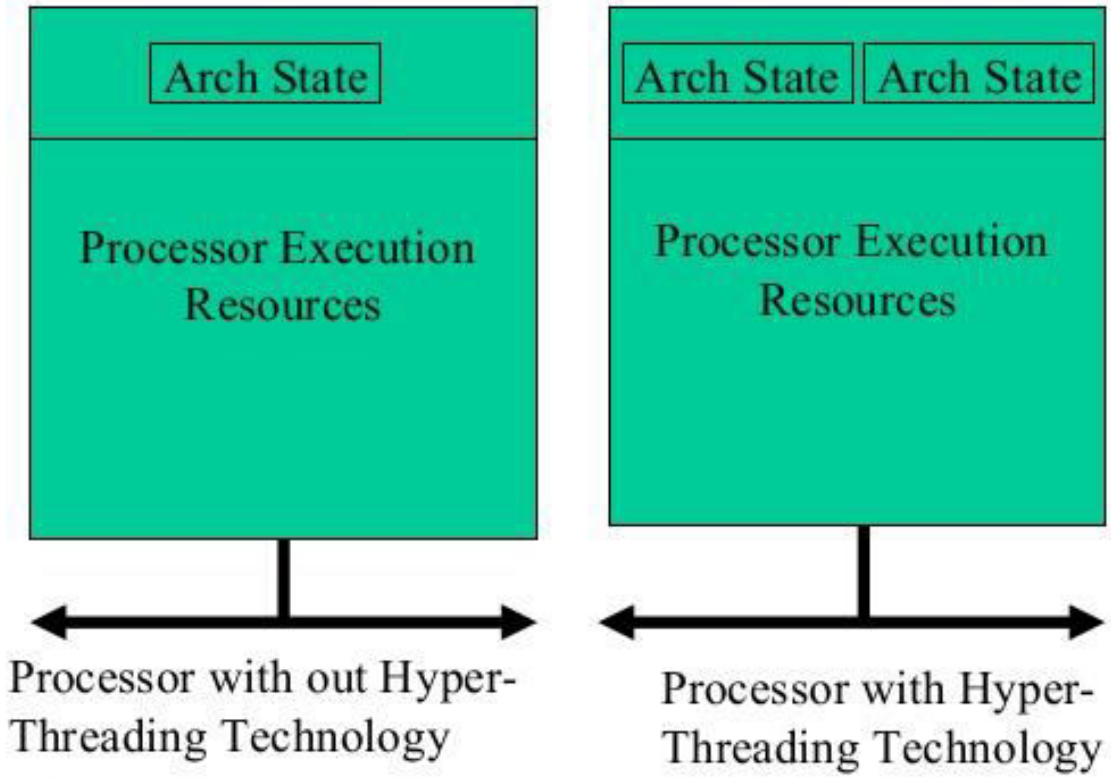
Αρχιτεκτονική NUMA



Hyper-threading technology

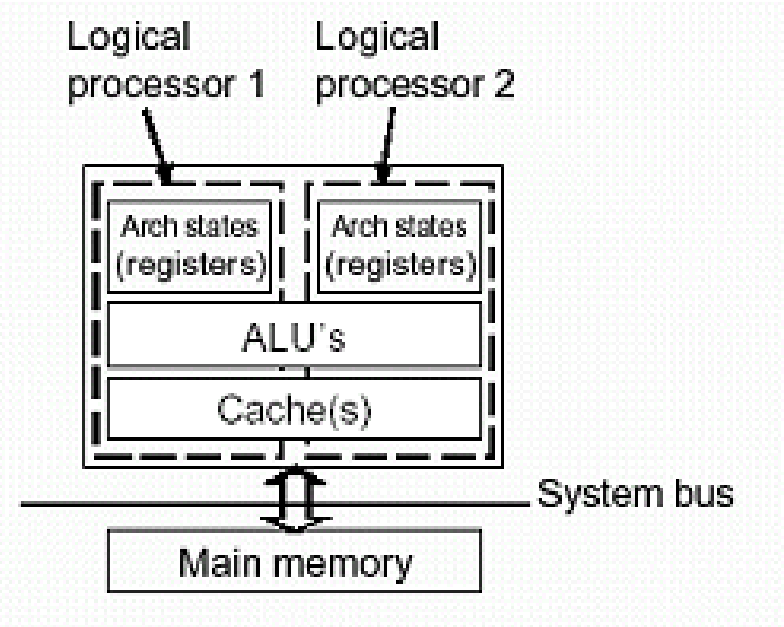
Hyper-threading (HT) technology, is Intel's proprietary simultaneous multithreading (SMT) implementation used to improve parallelization of computations (doing multiple tasks at once) performed on x86 microprocessors. It first appeared in February 2002 on Xeon server processors and in November 2002 on Pentium 4 desktop CPUs. Later, Intel included this technology in Atom, and Core 'i' Series CPUs, among others.

Hyper-Threading Technology Architecture

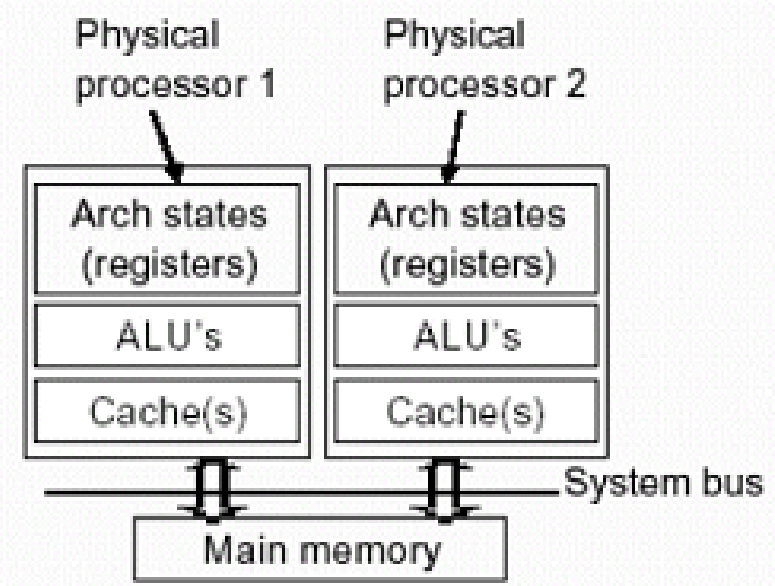


Αρχιτεκτονικές multithread και multicore

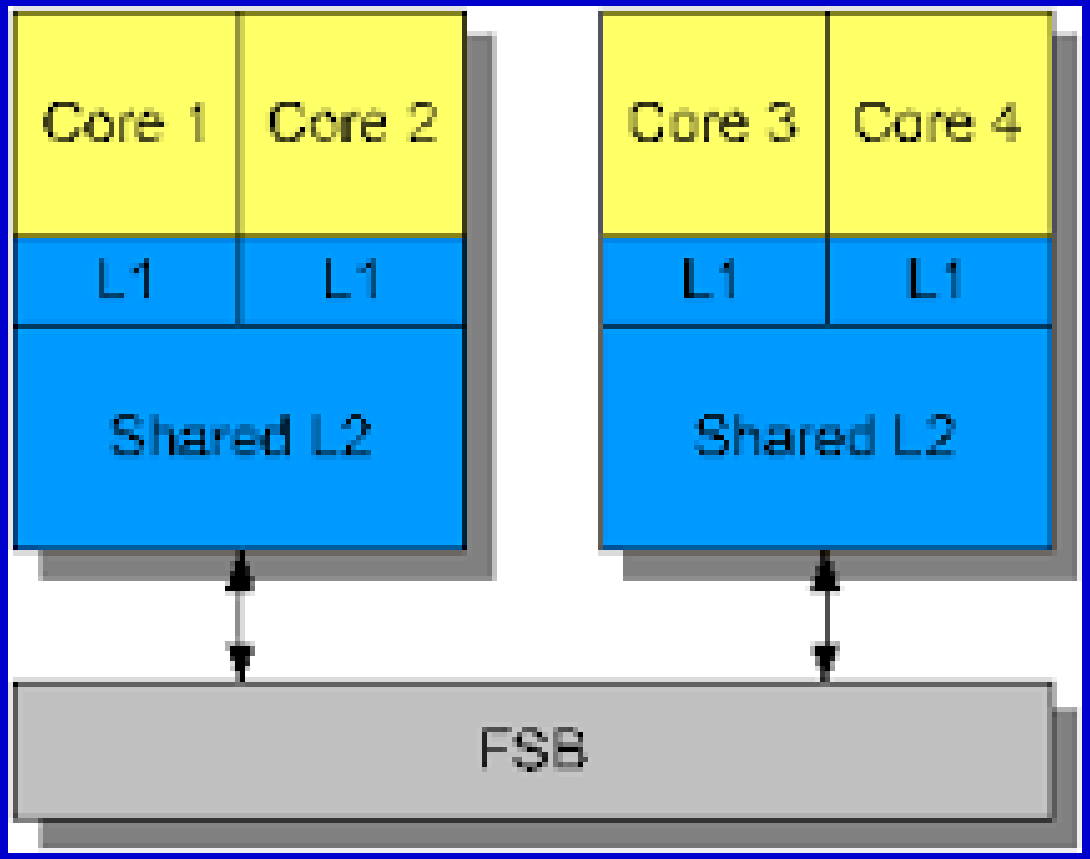
Multithread



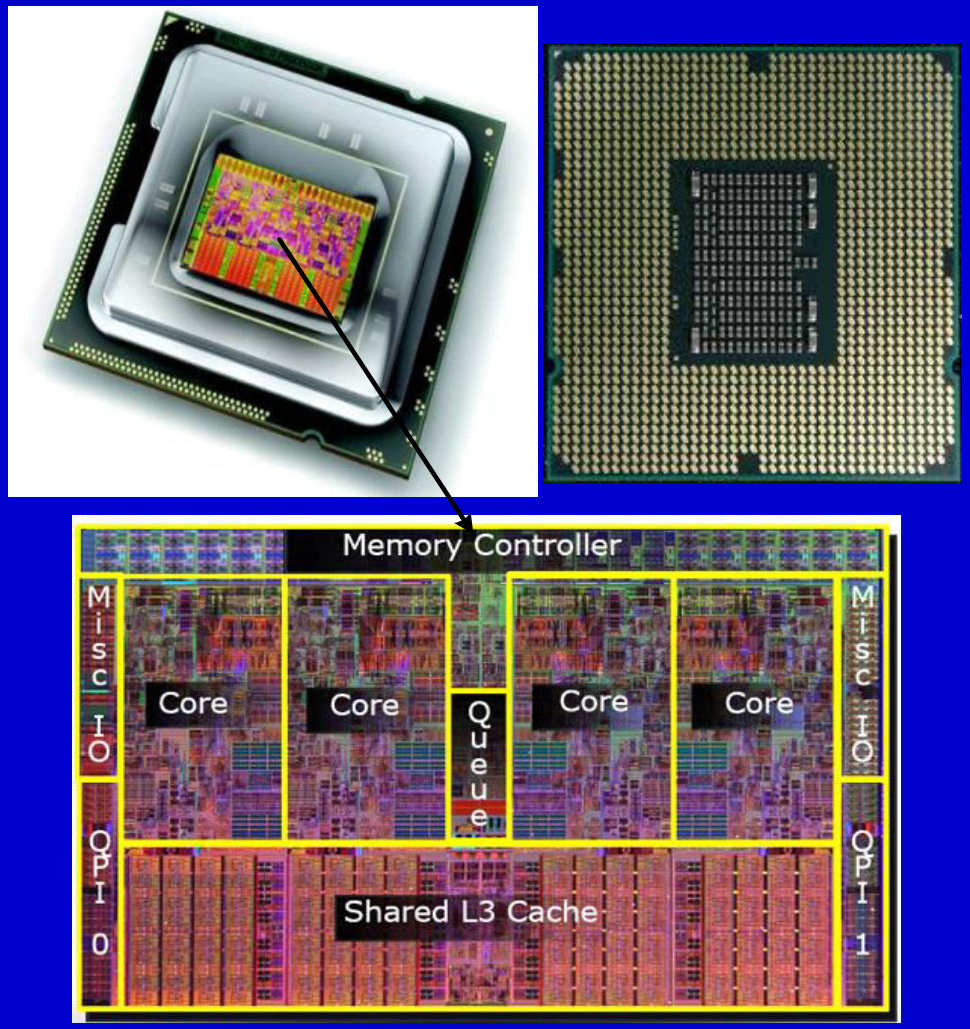
Multicore



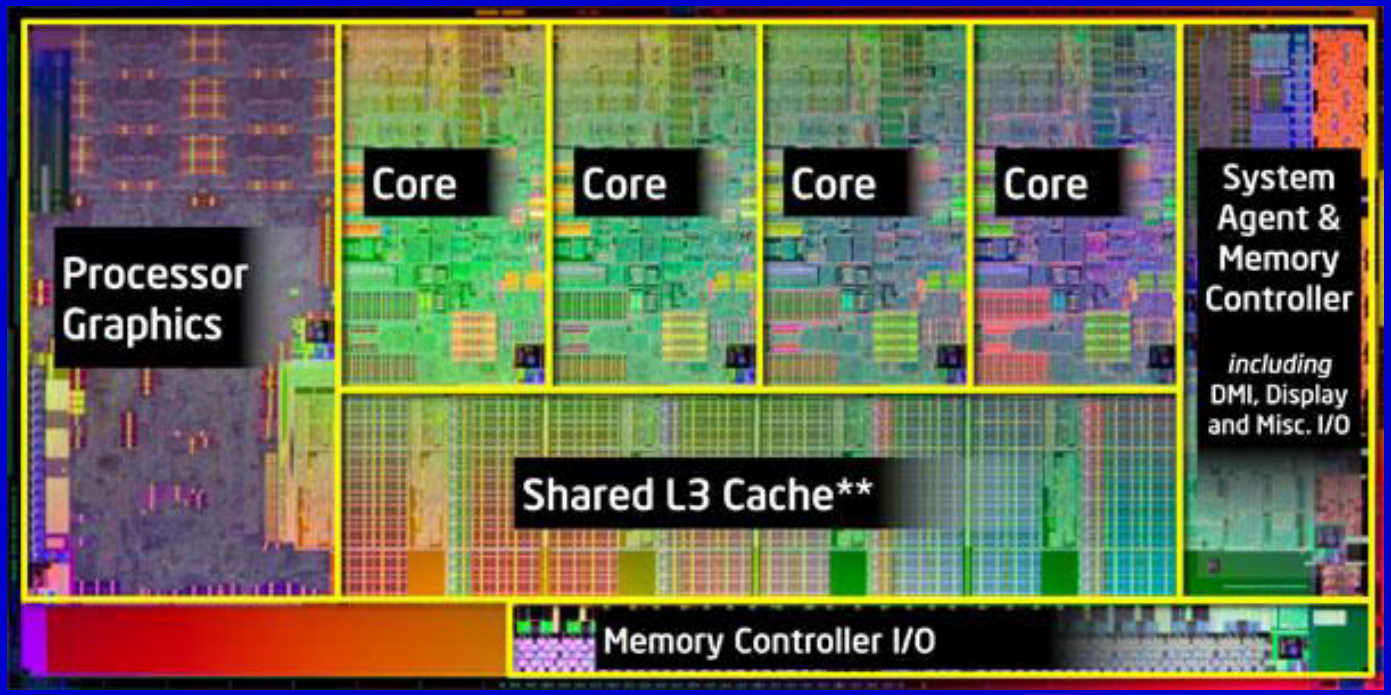
Multi Core Architecture



Intel Multi Core Architecture



Σύγχρονος τετραπύρηνος επεξεργαστής με ενσωματωμένη GPU

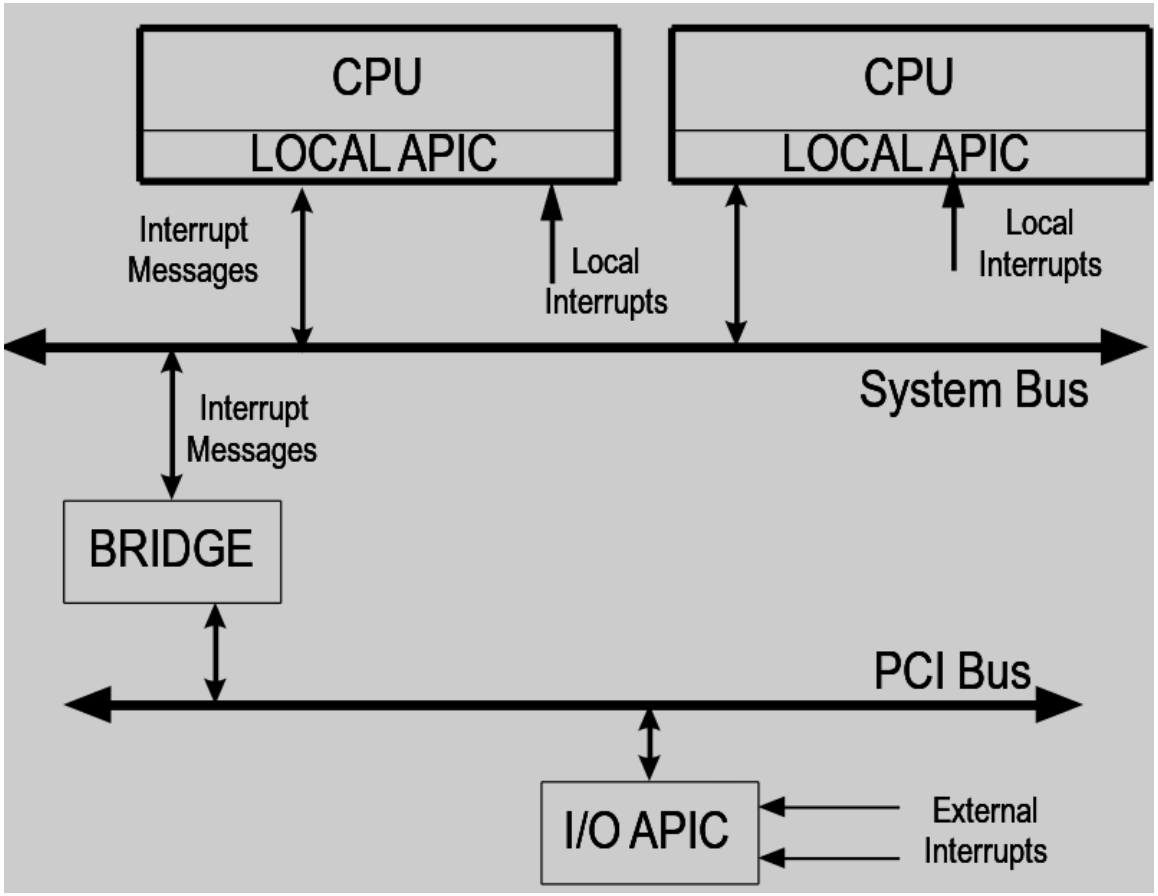


Σύστημα διακοπών APIC

In computing, Intel's **Advanced Programmable Interrupt Controller** (APIC) is a family of interrupt controllers. The APIC is more advanced than Intel's 8259 Programmable Interrupt Controller (PIC), particularly enabling the construction of multiprocessor systems. It is one of several architectural designs intended to solve interrupt routing efficiency issues in multiprocessor computer systems.

The APIC is a split architecture design, with a local component (LAPIC) usually integrated into the processor itself, and an optional I/O APIC on a system bus.

Σύστημα διακοπών APIC



SoC

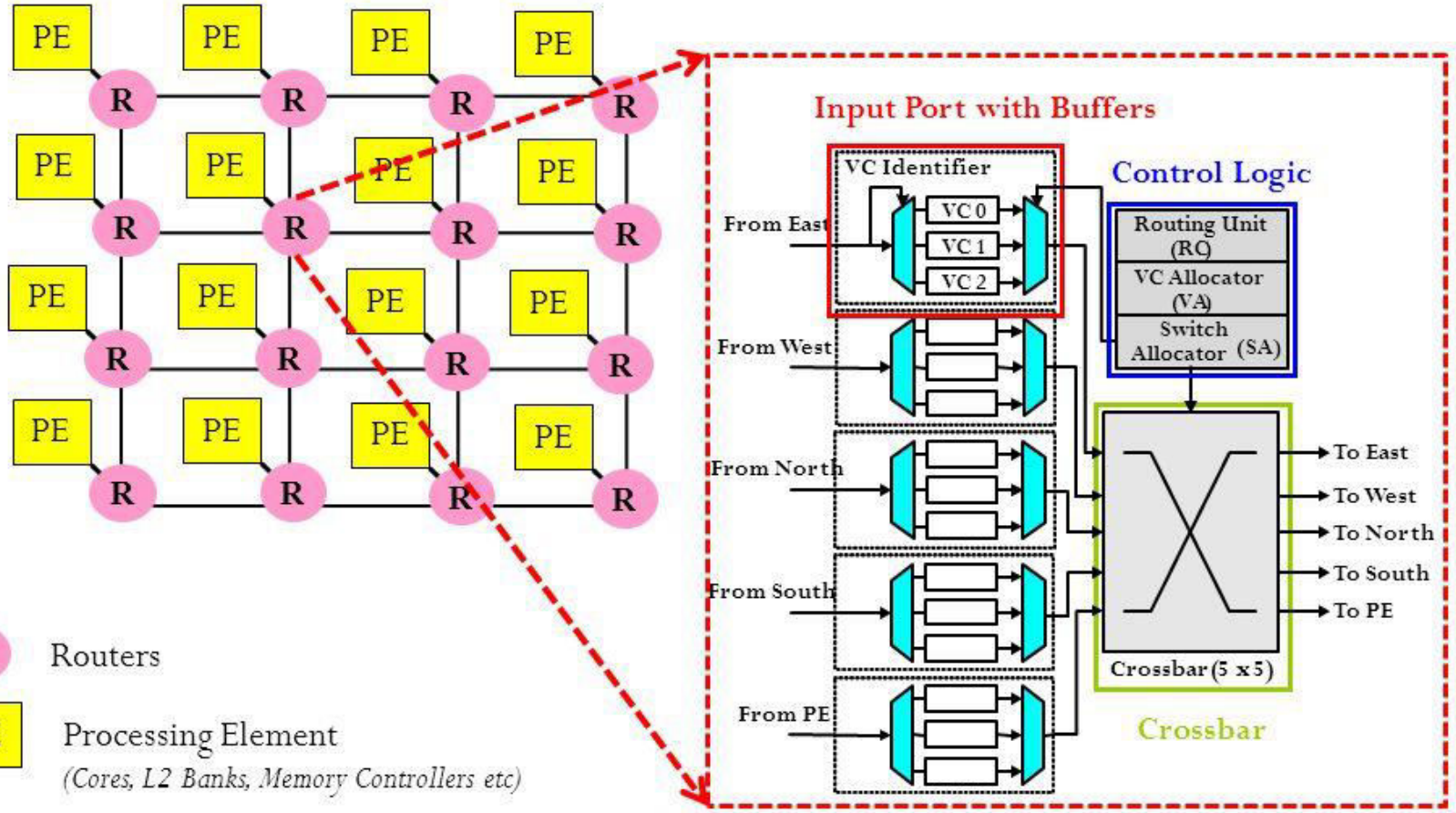
A **system on chip** (**SoC**) is an integrated circuit that integrates all components of a computer or other electronic system. It may contain digital, analog, mixed-signal, and often radio-frequency functions—all on a single substrate. SoCs are very common in the mobile computing market because of their low power consumption. A typical application is in the area of embedded systems.

SoC integrates a microcontroller or microprocessor with advanced peripherals like graphics processing unit (GPU), Wi-Fi module. SoC does not necessarily contain built-in memory.

Network on a Chip

Network on a chip (**NoC**) is a communication subsystem on an integrated circuit (chip), typically between cores in a system on a chip (SoC). NoCs can span synchronous and asynchronous clock domains or use unclocked asynchronous logic. NoC technology applies networking theory and methods to on-chip communication and brings notable improvements over conventional bus and crossbar interconnections. NoC improves the scalability of SoCs, and the power efficiency of complex SoCs compared to other designs.

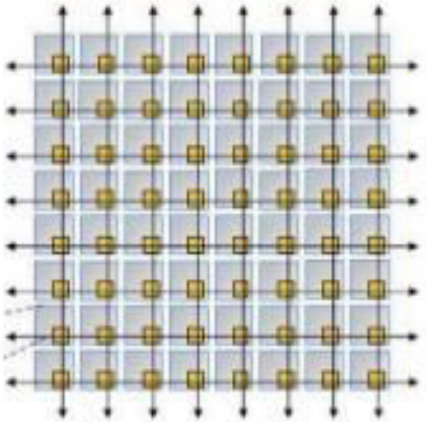
Network-on-Chip

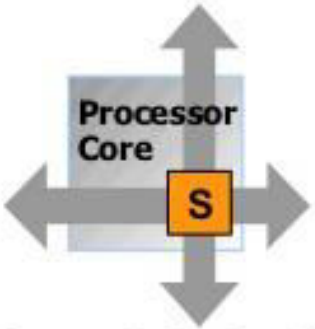


iMesh on-chip inter-core network

Sanctum Networks

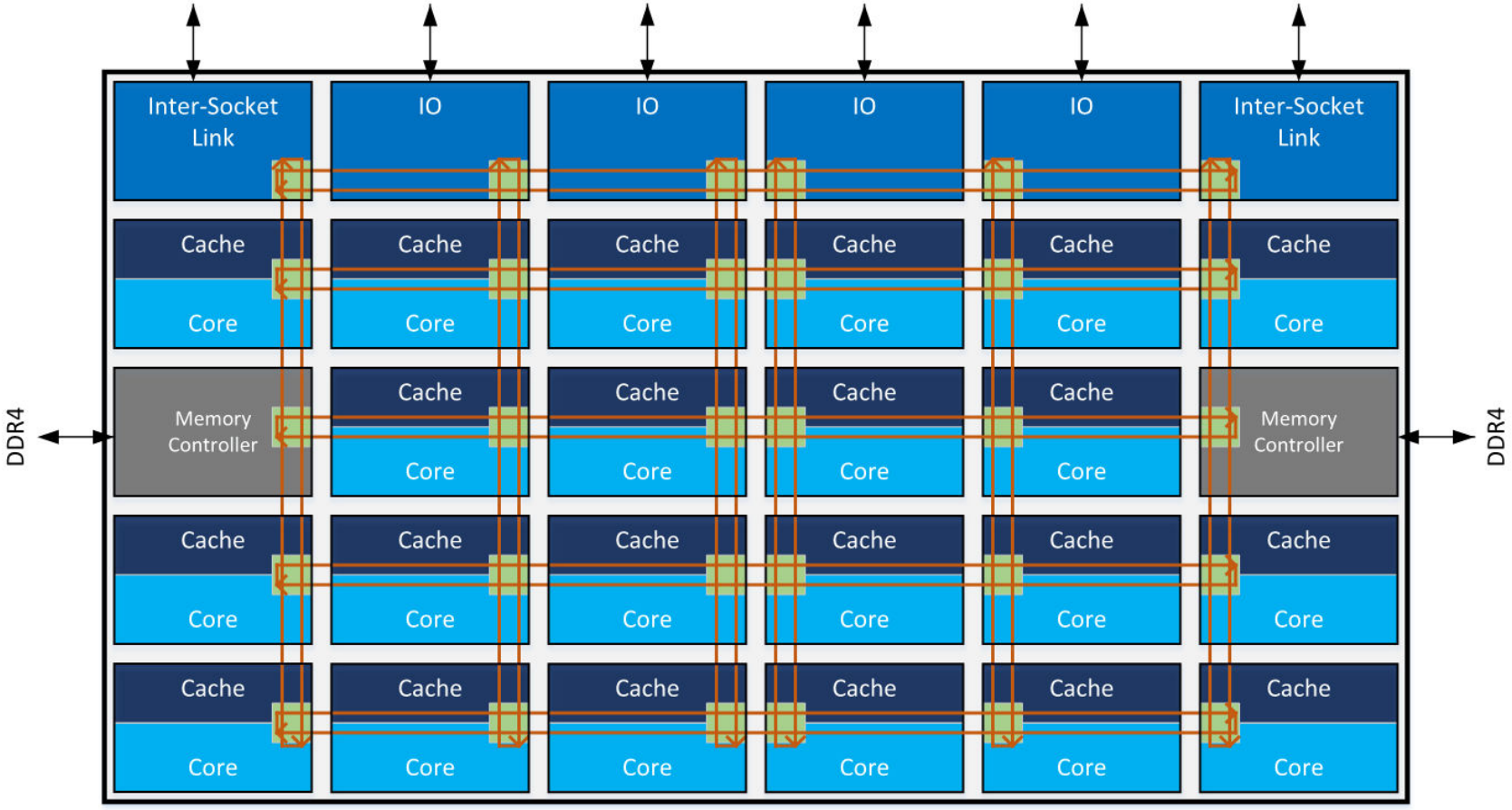
- laid out in tile with mesh shape inter-connect.
- an independent switch processor at each crossing
  - switch ties computing node with the entire on-chip network
- 38Tbps performance
- ensure global cache coherency
  - watches and manages each of L2 cache simultaneously.
- I/O interrupts travel across inter-connect.
  - uniform communication in IPI mechanism.





Core+ Switch = Tile

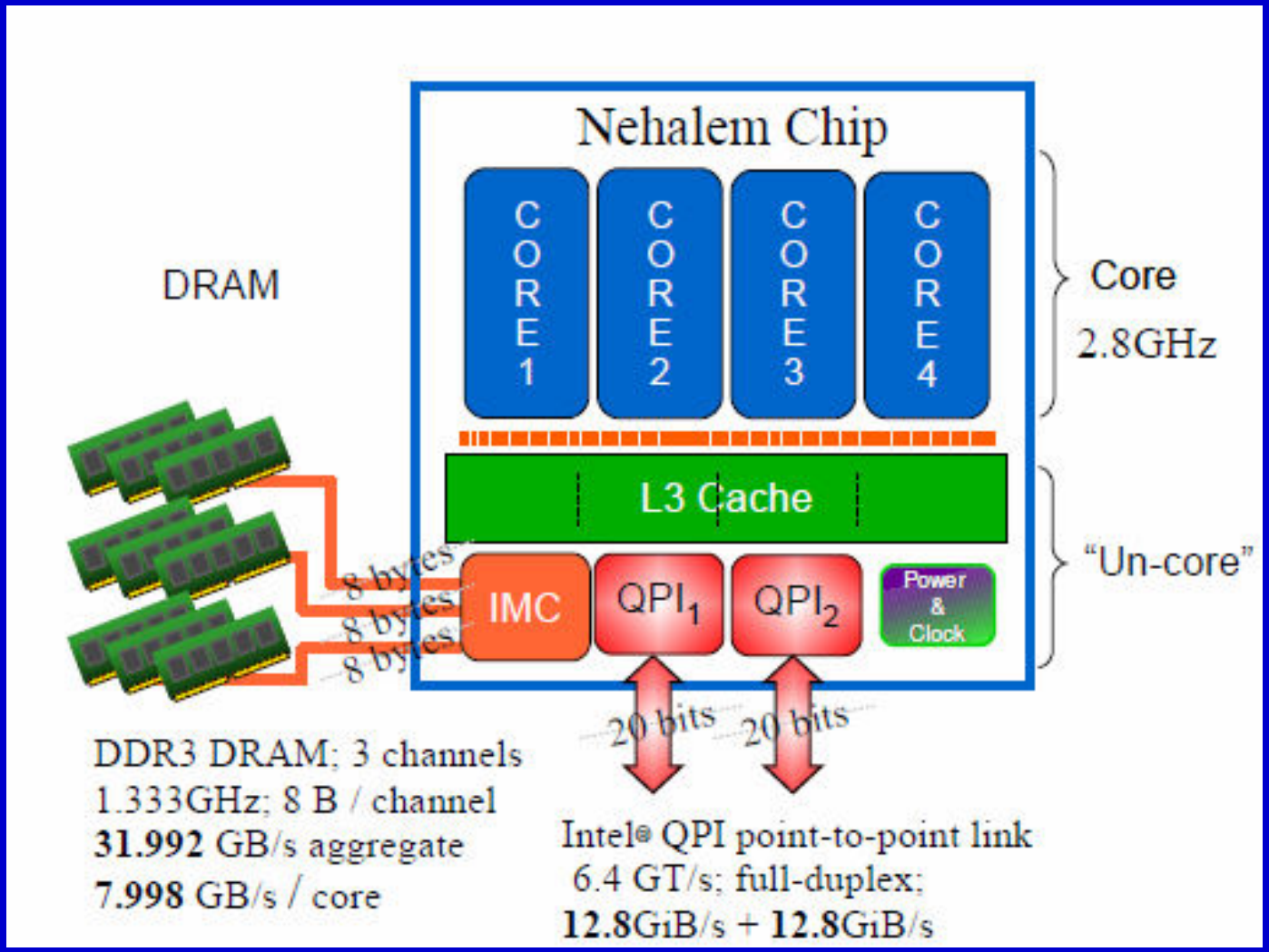
Intel mesh network architecture



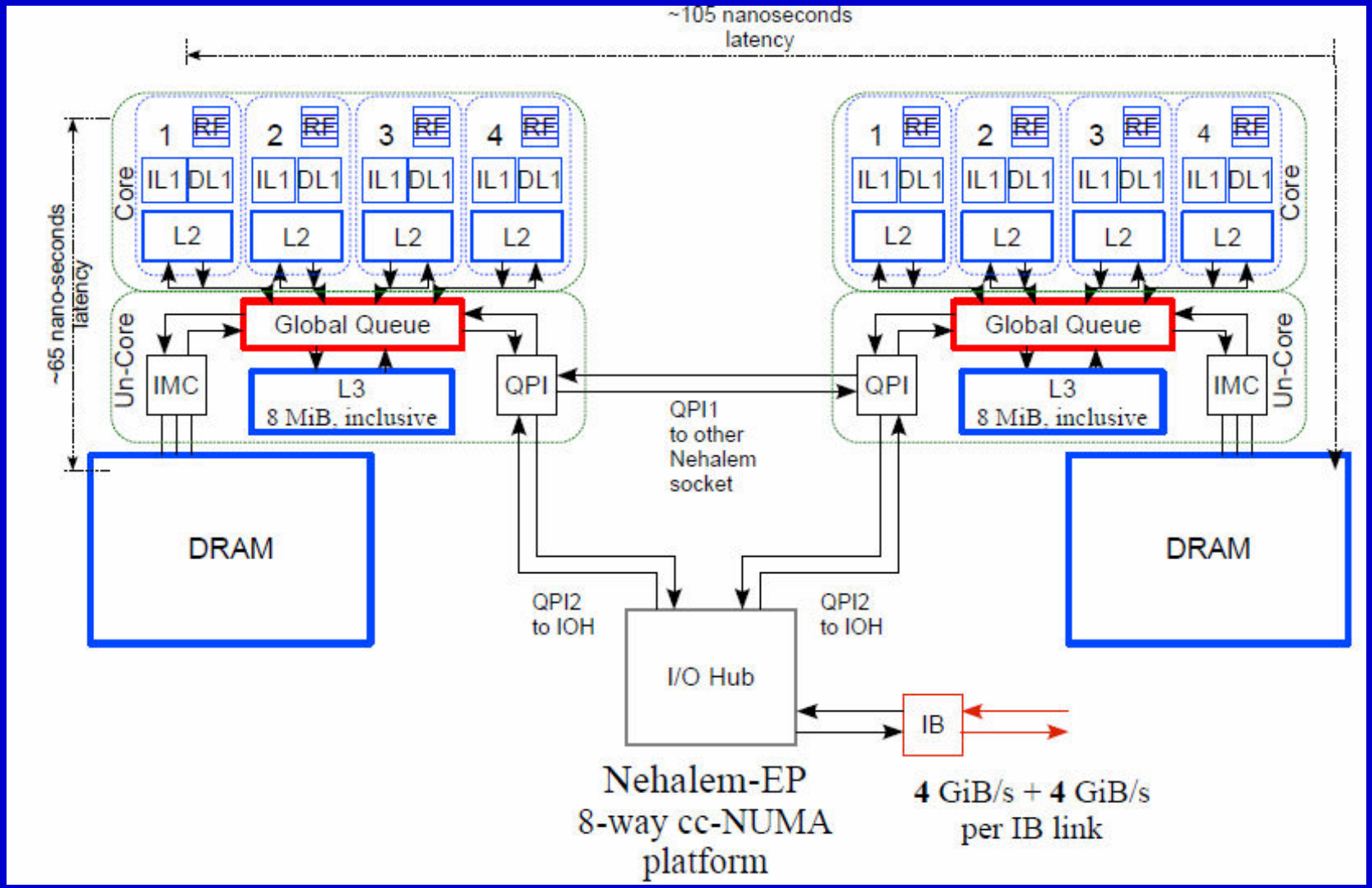
Intel Xeon

The **Xeon** is a brand of x86 microprocessors designed, manufactured, and marketed by Intel, targeted at the non-consumer workstation, and server markets. It was introduced in June 1998. **Xeon** processors are based on normal desktop-grade CPUs, but have some advanced features such as support for ECC memory, higher core counts, support for larger amounts of RAM, and larger cache memory. Some also support multi-socket systems with 2, 4, or 8 sockets.

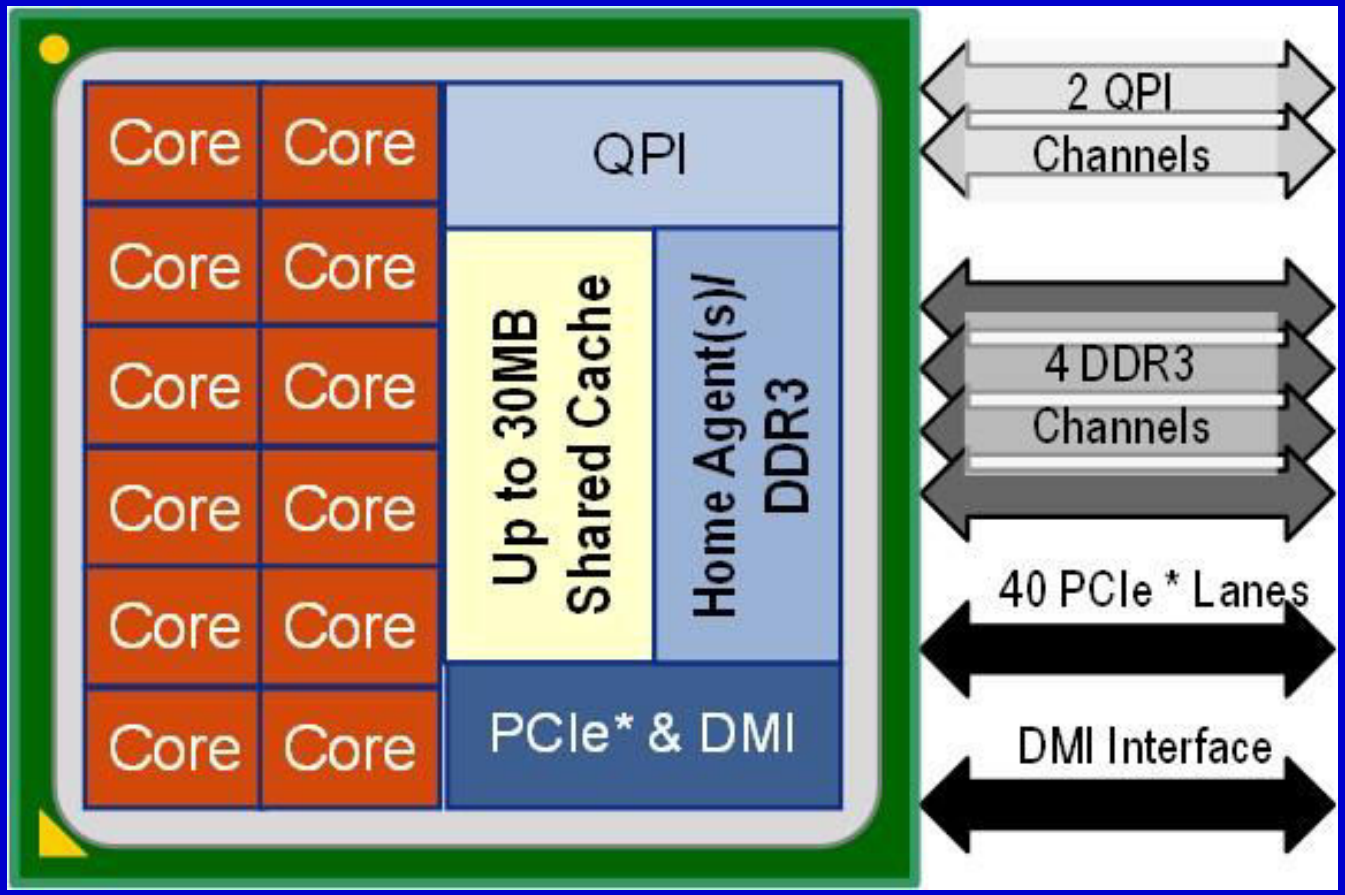
Επεξεργαστής Nehalem Xeon



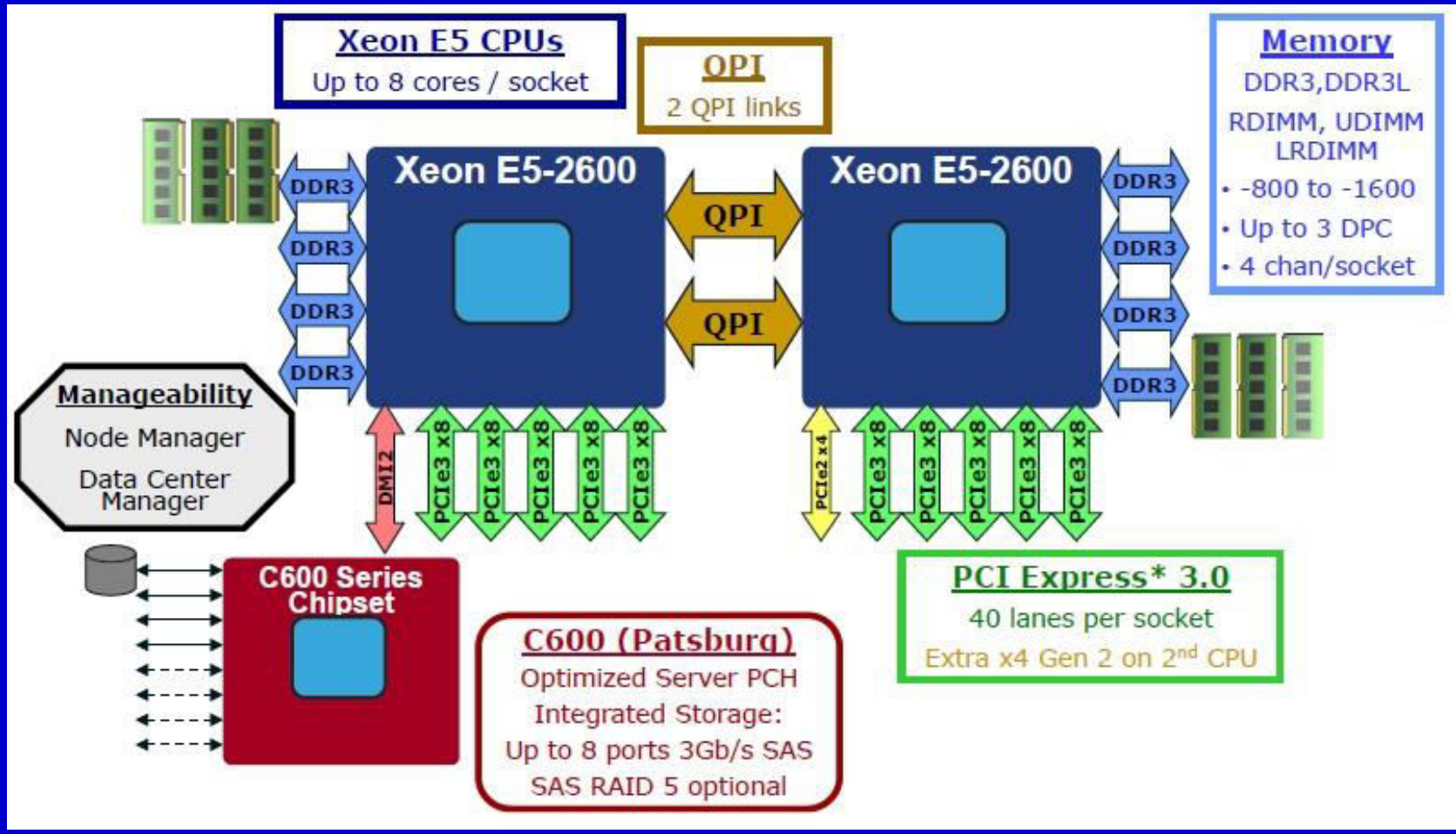
Σύστημα με αρχιτεκτονική NUMA βασισμένη σε Xeon



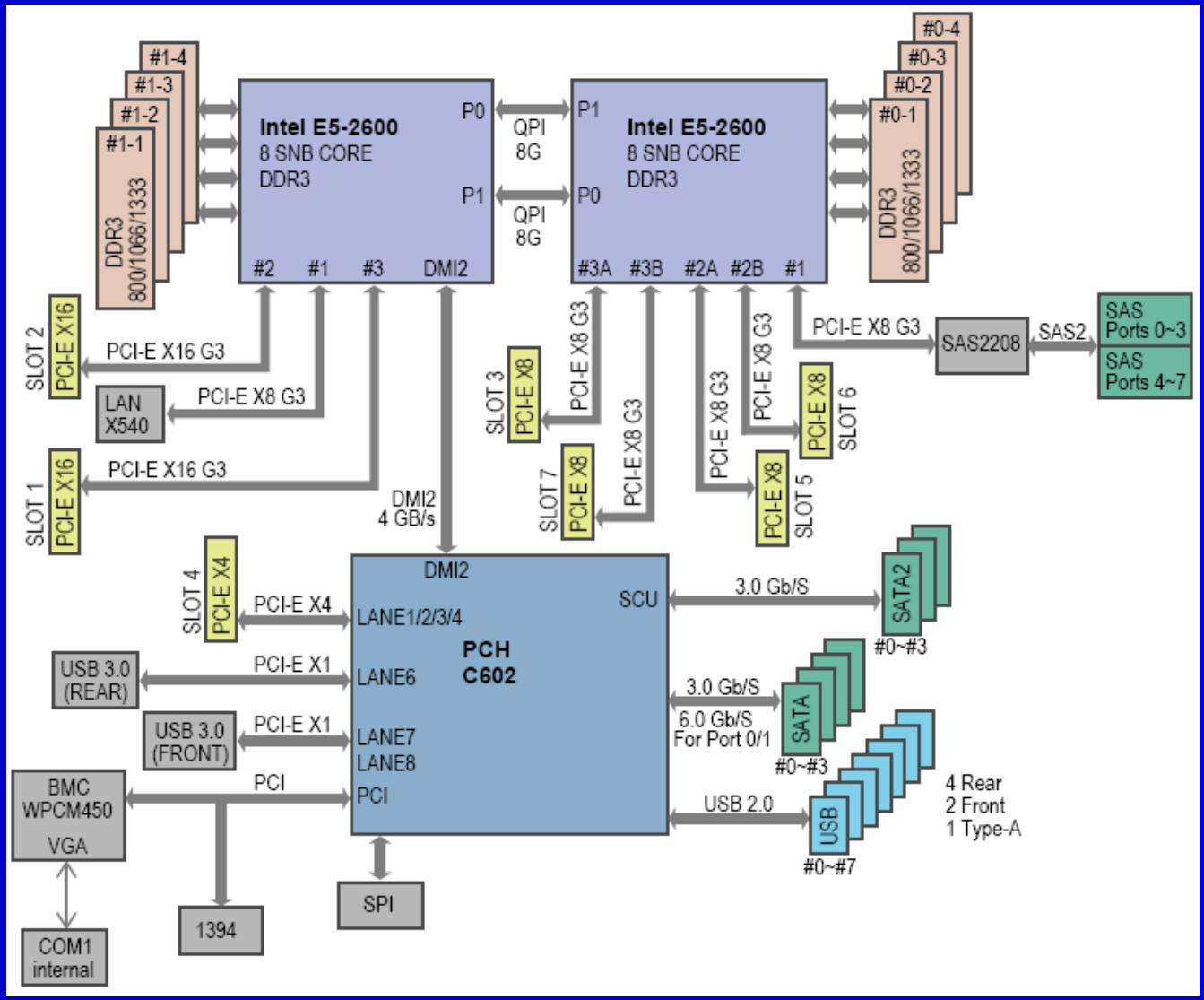
Xeon E5-2600 architecture



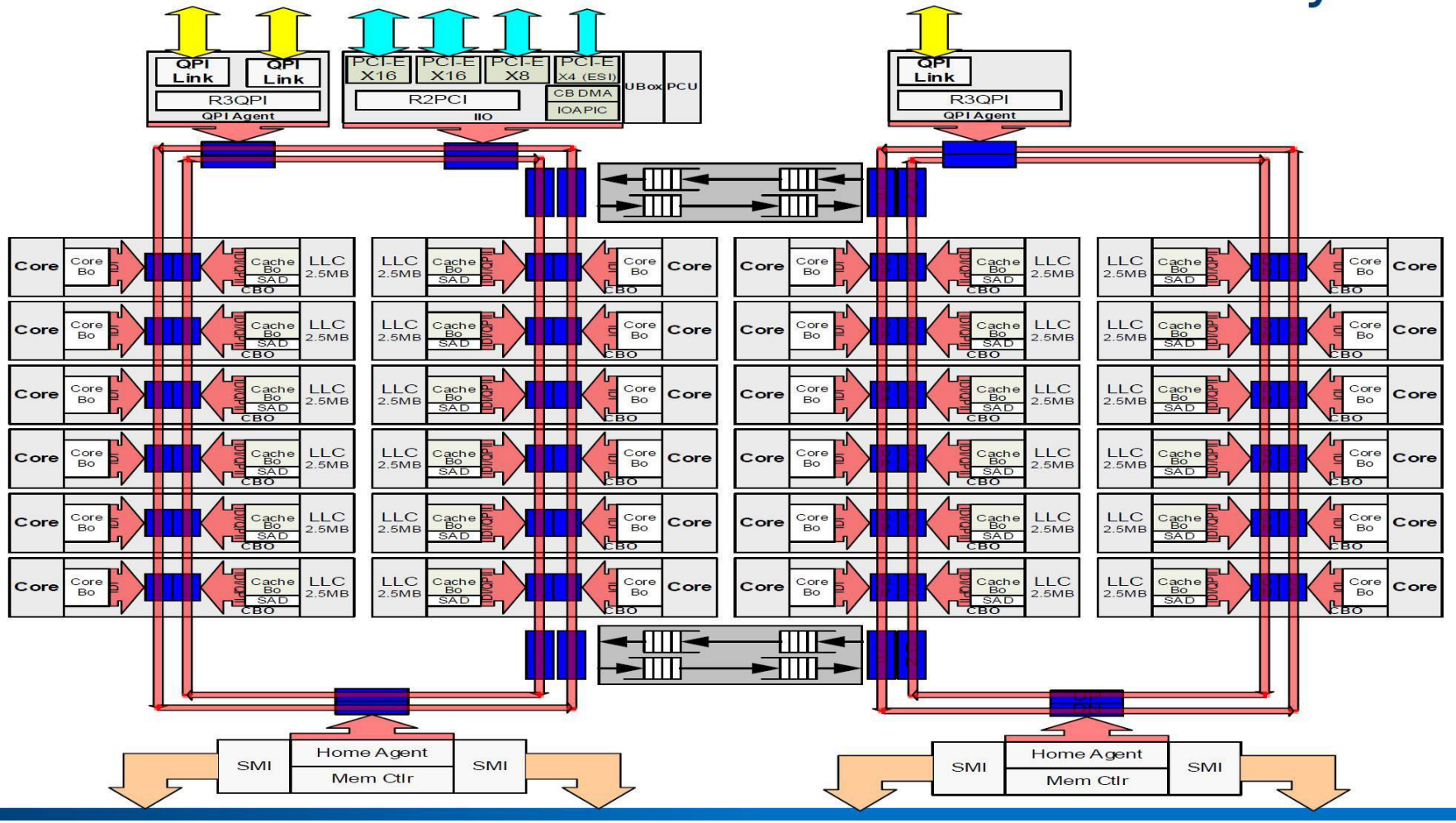
Σ **Διάγραμμα βαθμίδων συστήματος αρχιτεκτονικής NUMA με δύο Xeon**

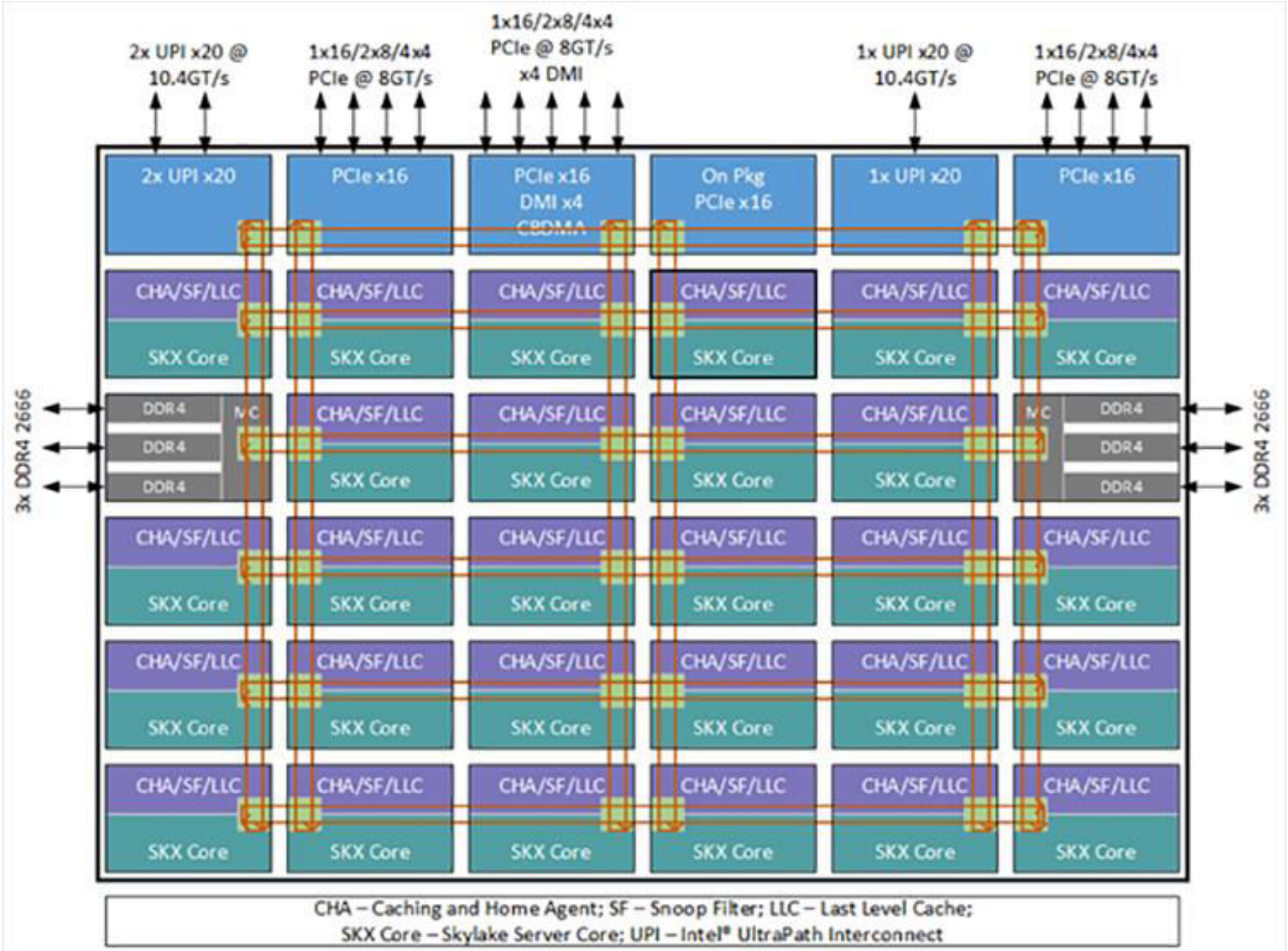


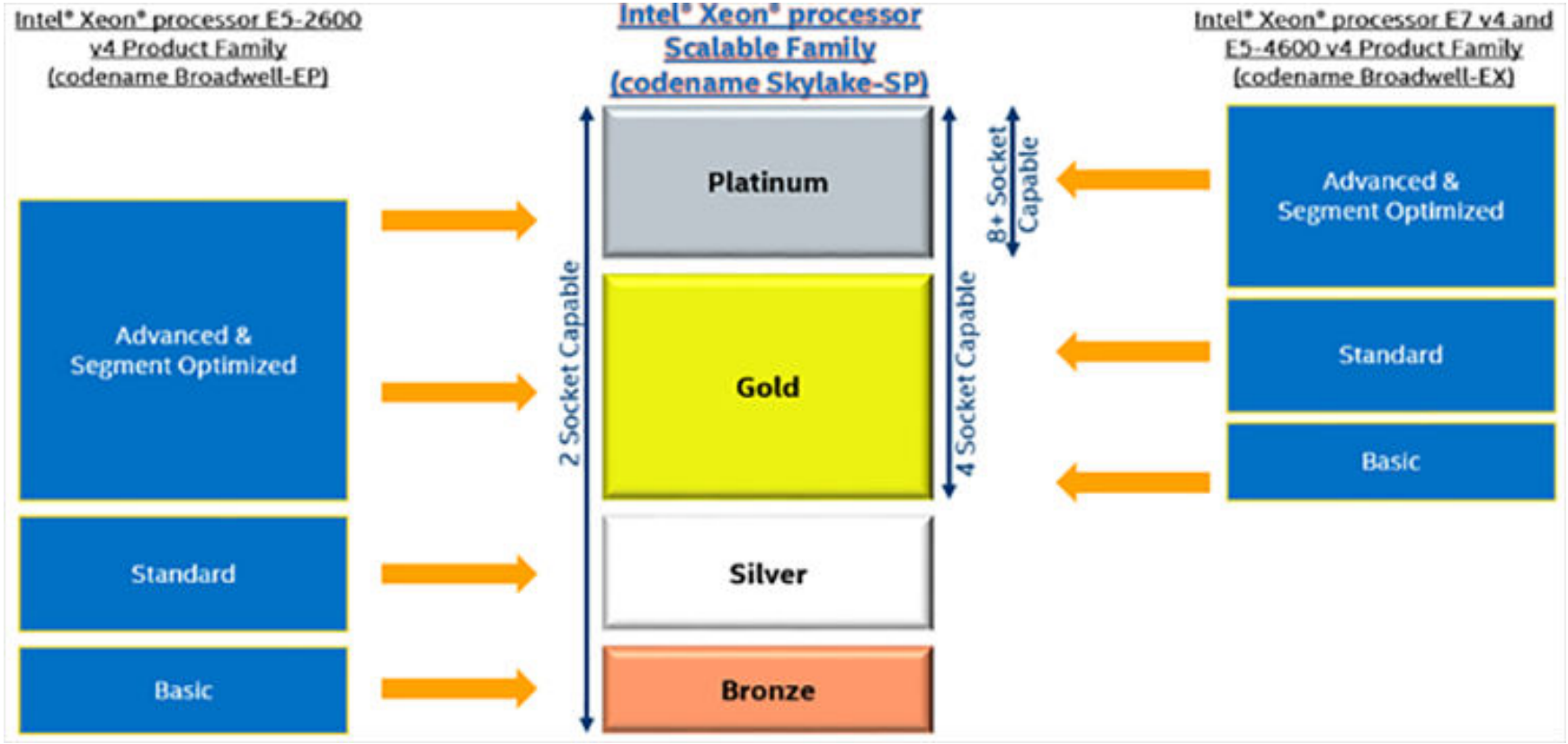
Διάγραμμα βαθμίδων motherboard με δύο Xeon



Intel® Xeon® Processor E7 v4 Product Family

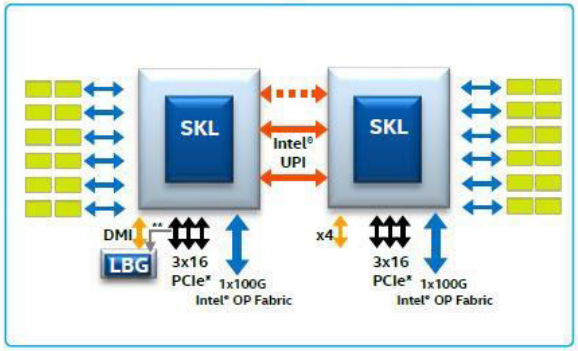



2x UPI x20 @ 10.4GT/s
1x16/2x8/4x4 PCIe @ 8GT/s
1x16/2x8/4x4 PCIe @ 8GT/s x4 DMI
1x UPI x20 @ 10.4GT/s
1x16/2x8/4x4 PCIe @ 8GT/s
2x UPI x20
PCIe x16
PCIe x16 DMI x4 CBDMA
On Pkg PCIe x16
1x UPI x20
PCIe x16
CHA/SF/LLC
SKX Core
IMC
DDR4
3x DDR4 2666
CHA – Caching and Home Agent; SF – Snoop Filter; LLC – Last Level Cache;
SKX Core – Skylake Server Core; UPI – Intel® UltraPath Interconnect


Intel® Xeon® processor E5-2600 v4 Product Family (codename Broadwell-EP)
Intel® Xeon® processor Scalable Family (codename Skylake-SP)
Intel® Xeon® processor E7 v4 and E5-4600 v4 Product Family (codename Broadwell-EX)
Advanced & Segment Optimized
Standard
Basic
Platinum
Gold
Silver
Bronze
2 Socket Capable
4 Socket Capable
8+ Socket Capable
Advanced & Segment Optimized
Standard
Basic

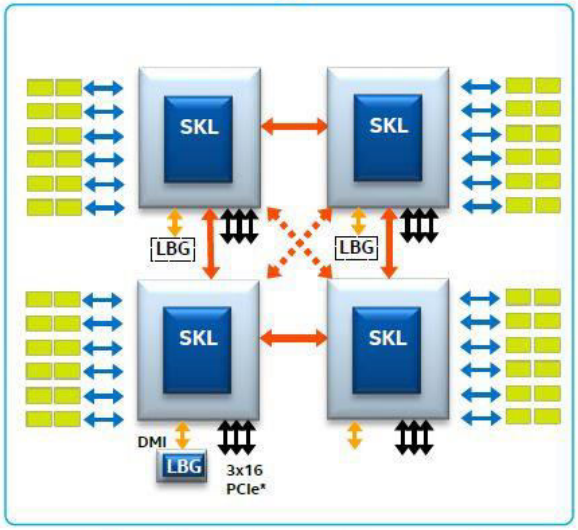
Platform Topologies

2S Configurations



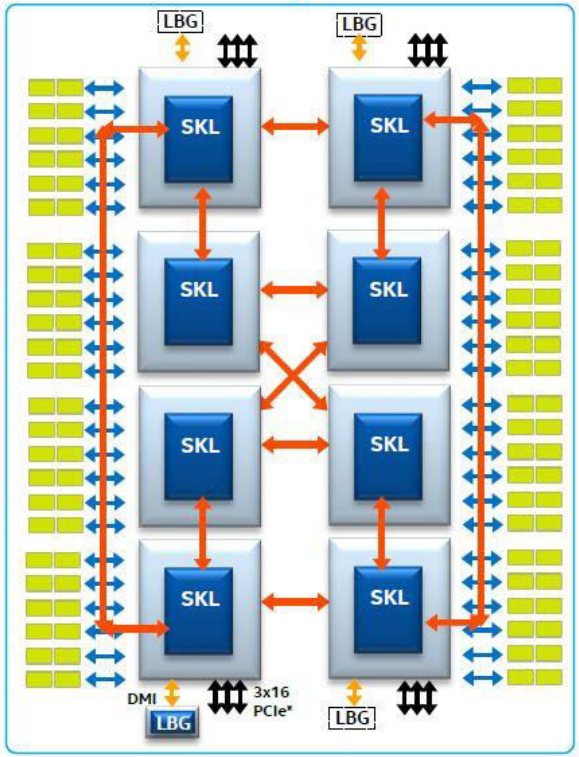
(2S-2UPI & 2S-3UPI shown)

4S Configurations



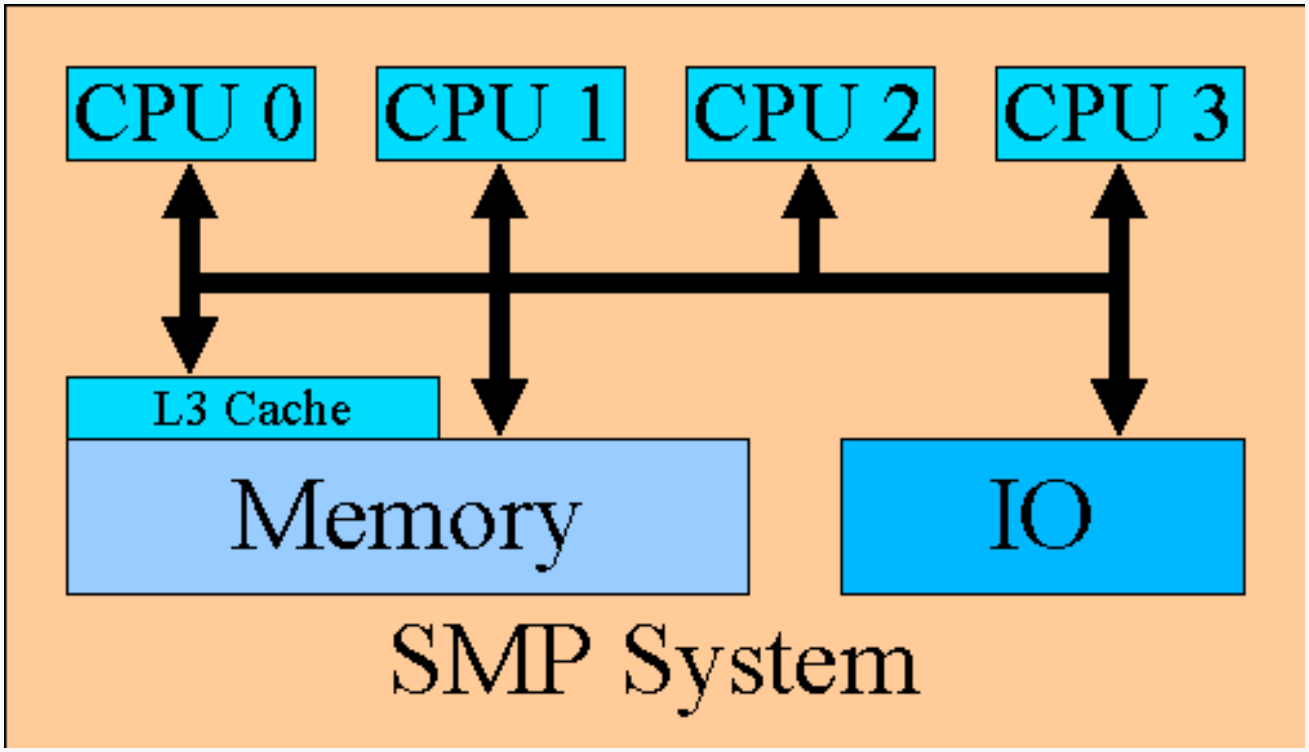
(4S-2UPI & 4S-3UPI shown)

8S Configuration

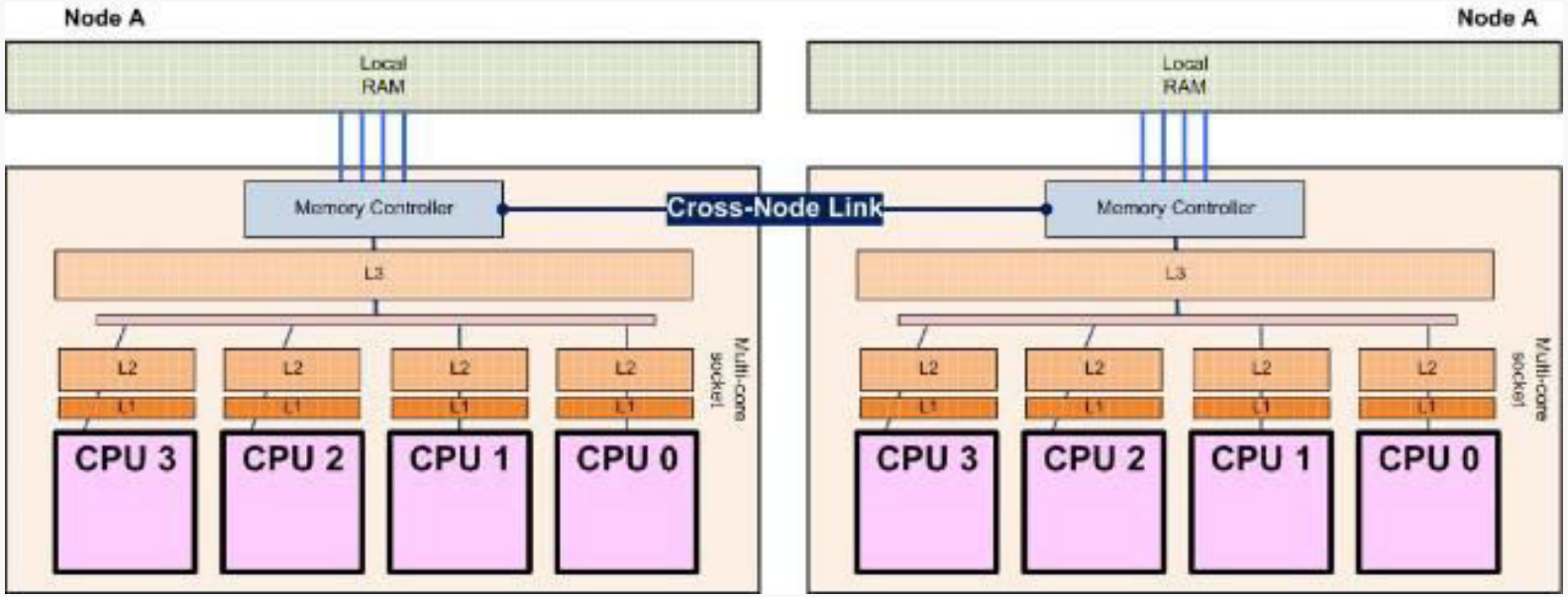


INTEL® XEON® SCALABLE PROCESSOR SUPPORTS CONFIGURATIONS RANGING FROM 2S-2UPI TO 8S

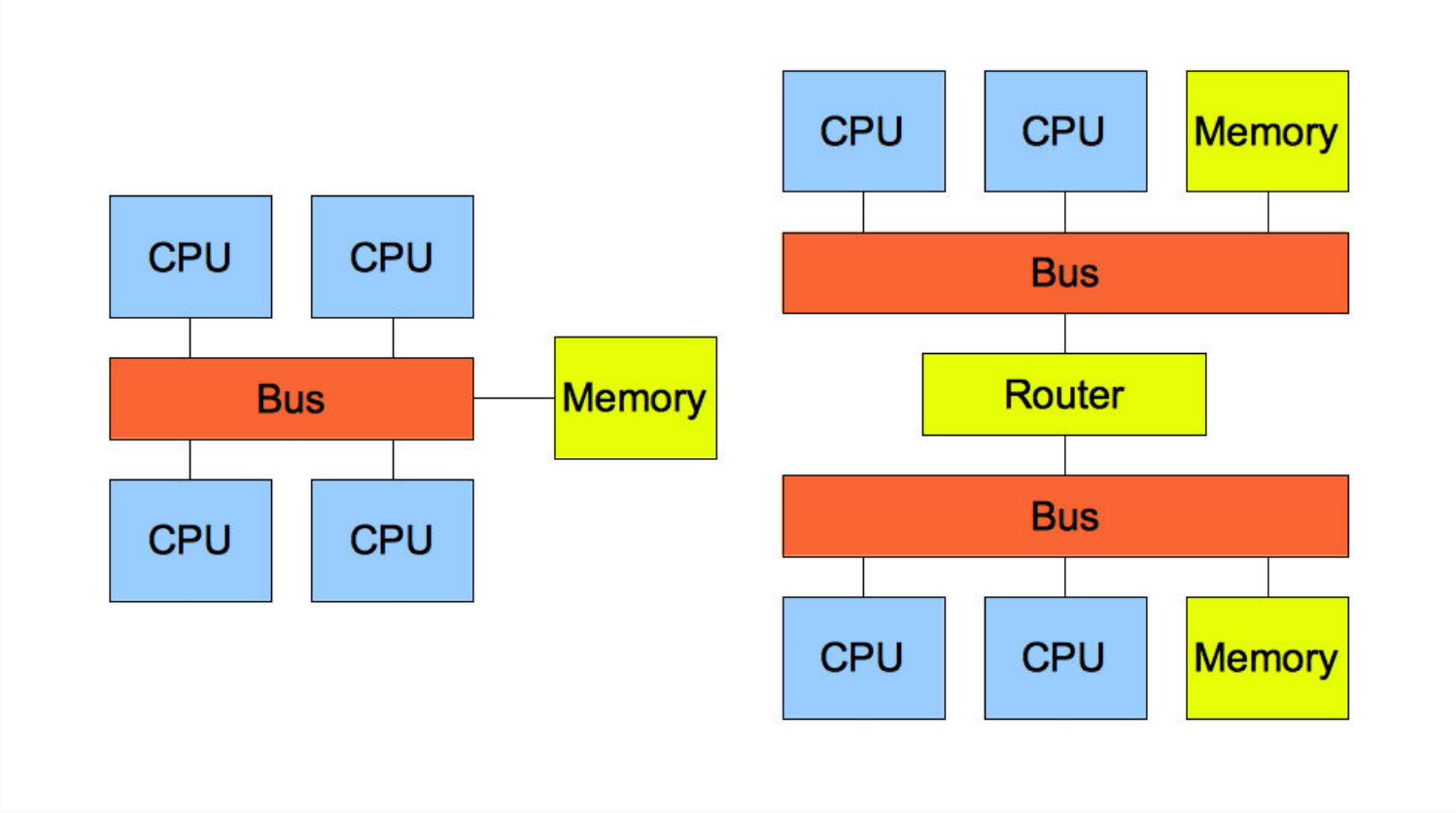
11.1. Τι αρχιτεκτονική είναι αυτή που περιγράφεται στην συνέχεια



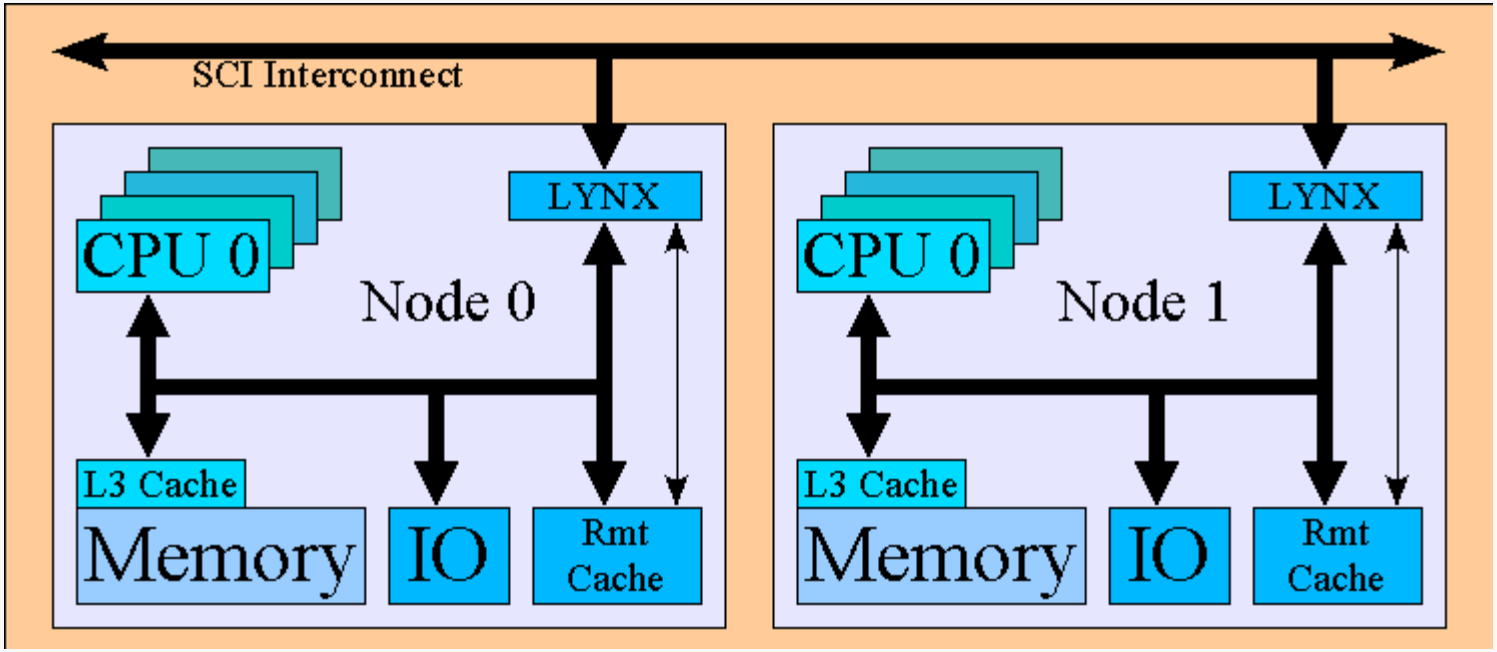
11.2. Αναφέρατε τον τύπο της αρχιτεκτονικής που περιγράφεται στην συνέχεια καθώς και των επί μέρους τμημάτων.



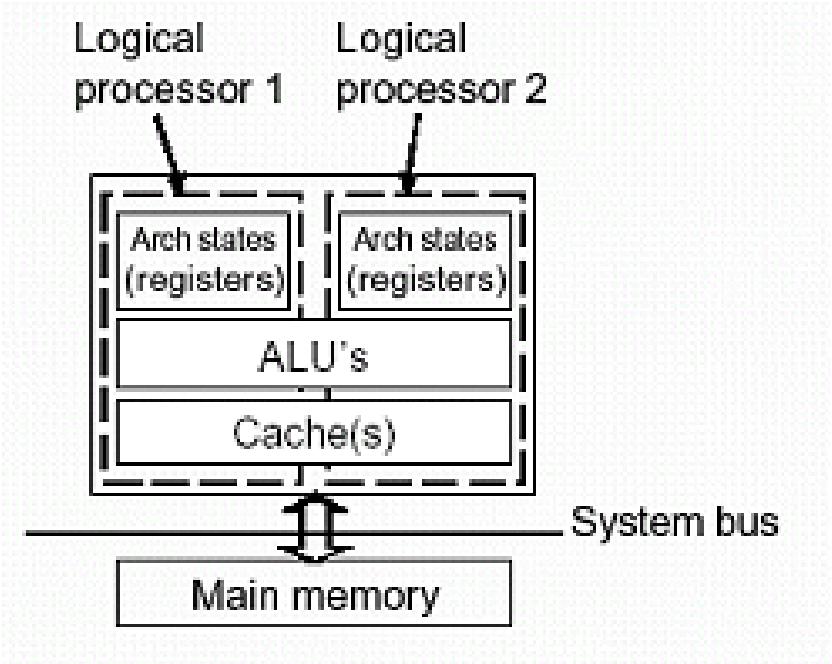
11.3. Από τις αρχιτεκτονικές που περιγράφονται στην συνέχεια είναι NUMA και ποια SMP.

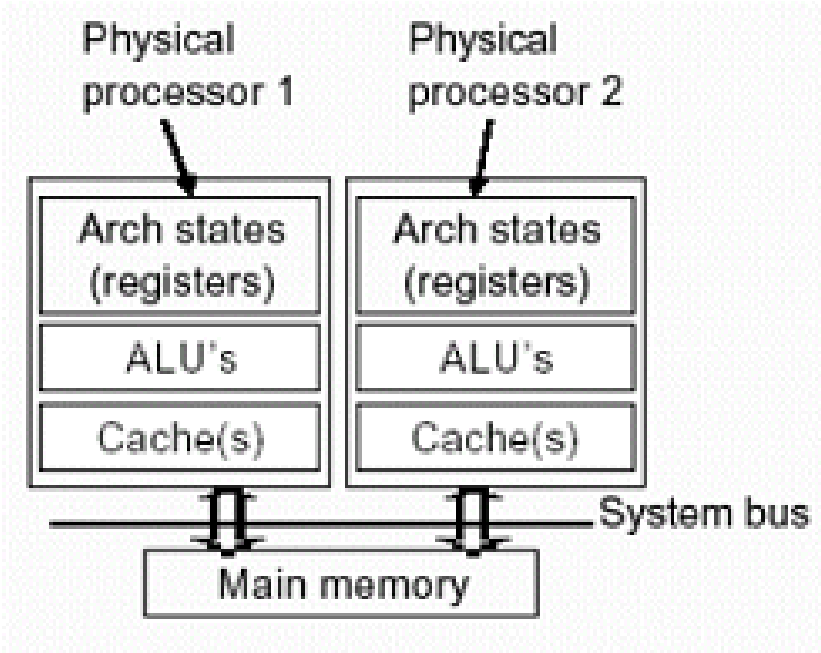


11.4. Τι είδους αρχιτεκτονική συνολικά είναι αυτή που περιγράφεται στην συνέχεια και ποια είναι η αρχιτεκτονική κάθε κόμβου.

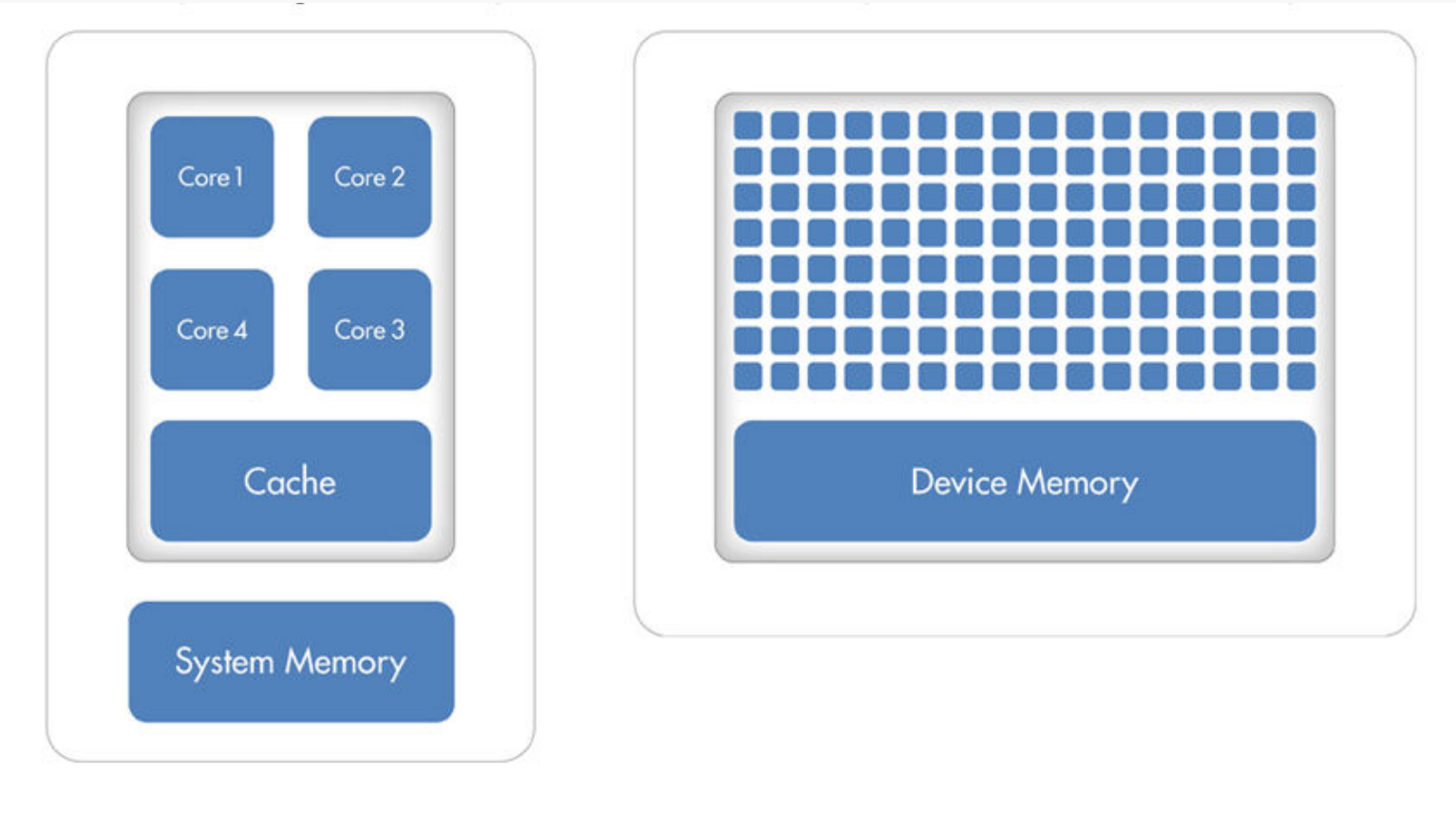


11.5. Από τις αρχιτεκτονικές που περιγράφονται στην συνέχεια ποια είναι hyperthread και ποια multicore.





11.6. Από τις multicore αρχιτεκτονικές που δίδονται στην συνέχεια ποια αντιστοιχεί σε CPU και ποια σε GPU.



11.7. Τι είδους αρχιτεκτονική είναι αυτή που περιγράφεται στην συνέχεια.